A Study of Metal-Semiconductor Contacts for Use as Detectors of Nuclear Radiation

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by

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Summary

An outline of current metal-semiconductor junction theories is given with particular attention being paid to the parameters which affect the performance of surface barrier nuclear radiation detectors. An evaluation of evaporated aluminium as a means of obtaining a low resistance, non-injecting ohmic back contact to silicon is made and the stability of the contact is shown to be dependent on the surface treatment of the silicon prior to the evaporation process. The structure of evaporated gold films deposited on silicon held at room temperature is investigated and the influence of substrate preparation and crystallographic orientation are shown to be the important parameters which determine the type of film deposited. Resistance-thickness plots for well oriented, hole-free annealed gold films indicate that their imperfection scattering mean free path is about 300 Å and this small value is supported by the low yield of photoexcited carriers across gold-silicon junctions. Photo-threshold measurements give a value of 0.79 ± 0.01 eV for the metal-semiconductor barrier height in the case of gold-silicon devices. Finally an assessment of the noise of an alloyed back radiation detector (pulse height spread equivalent to about 90 KeV FWHM at 100 V) indicates that such a device may prove useful for alpha particle detection.

Contents

GLOSSARY OF SYMBOLS

A^*	modified Richardson constant for emission of electrons over a metal-semiconductor barrier.
C_{dep}	depletion layer capacitance.
C_{inc}	incremental or differential capacitance.
E	energy.
E_c	conduction band edge energy.
E_F	Fermi level energy.
E_v	valence band edge energy.
E_i	intrinsic energy level.
F	Fano factor. (Chapter 3)
F	electric field. (Chapter 2)
G	generation rate.
I	current density.
I_S	saturation current density.
J_D	diffusion current density due to holes.
J_g	generation current density in space charge region.
L	diffusion length of carriers in semiconductor.
L(E)	hot electron attenuation length.
N	number of ion pairs generated by an energetic particle.
N_c	number of charge carriers in the depletion region.
N'	number of charge carriers in transit in counter.
N_D	donor density.
N_{ge}	number of electrons in depletion layer due to thermal generation.

N_{gh}	number of holes in depletion layer due to thermal generation.
Q_M	charge on metal surface.
Q_{SC}	charge in depletion region.
Q_{SS}	charge in surface states.
R	resolution of counter.
R_D	dynamic resistance of diode.
S	surface recombination velocity.
T	absolute temperature.
U_S	defined as $(E_F - E_i/kT)$ at the surface of a semiconductor.
U_B	defined as $(E_F - E_i/kT)$ in the bulk of a semiconductor.
V	potential.
V_A	applied reverse bias.
V_D	diffusion potential.
W	energy of particle.
X_S	electron affinity of semiconductor.
Y	photocurrent per absorbed photon.
e	charge on electron.
h	Planck's constant.
j_D	current density in a Schottky barrier from diffusion theory
j_S	saturation current density for a Schottky barrier from diode theory.
k	Boltzmann's constant.
l	mean free path.
m*	effective mass of electron in semiconductor.

n_i	intrinsic carrier concentration.
p_n	equilibrium density of holes in n-type semiconductor.
S_1	entrance slit width of monochromator.
S_2	exit slit width of monochromator.
v	electron velocity.
w	mean energy required to form ion pair.
α	photon absorption constant.
δ	thickness of separation between metal and semiconductor.
ϵ	relative dielectric constant.
ϵ_o	permittivity of free space.
ϵ_d	image force dielectric constant.
ϕ_M	work function of metal.
ϕ_S	work function of semiconductor.
ϕ_o	energy interval over which the surface states of an n-type semiconductor are filled.
ϕ_F	energy difference between Fermi level and conduction band edge.
ϕ_{MS}	metal-semiconductor barrier energy measured from Fermi level.
λ	depletion layer thickness under non-equilibrium conditions.
λ_o	depletion layer thickness under equilibrium conditions.
$\delta\lambda'$	spectral resolution of monochromator.
Δ_o	potential drop across oxide due to distribution of charge in slow states.
ρ	resistivity

τ	circuit time constant.
τ_o	dielectric relaxation time.
τ_c	charge collection time.
τ'	mean free time of carrier.
τ_r	recombination time.
τ_{eff}	effective lifetime.
τ_F	relaxation time associated with electrons at the Fermi level.
γ	frequency of radiation.
γ_o	threshold frequency.
μ_n	electron mobility in semiconductor.
μ_p	hole mobility in semiconductor.
σ	standard deviation.
χ	conductivity.

Biography

In July 1963 the author graduated in Physics (B.Sc. Tech. Hons.) at U.M.I.S.T.. The following October he began the one year M.Sc. course in Solid State Electronics by examination and dissertation, graduating in July 1965. The work for the Ph.D. degree commenced in January 1965.

All the work referred to in this thesis was done by the author himself during the past two years at U.M.I.S.T.. None of the contents of the thesis has been submitted in support of another degree either at U.M.I.S.T. or any other institute of learning.

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I would like to express my gratitude to Professor E. H. Rhoderick for accepting me as a research student and providing research facilities for the Solid State Electronics group. I would also like to thank my supervisor, Dr. D. C. Northrop, for his guidance and for discussions during this project and also Mr. A. J. Wright and Mr. H. D. McKell, who as staff of the S.S.E. group have always been of assistance.

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Chapter 1

Introduction

There are many inherent advantages in using semiconducting solids to detect nuclear particles compared with the more conventional ionization chamber and scintillation counter. In the first place a solid possesses a greater density and stopping power than a gas. For instance, about one millimetre of germanium or silicon would completely absorb 10 MeV protons, 0.9 MeV beta particles or 40 MeV alpha particles (Fig. 1.1 and Fig. 1.2.). Detectors made of such materials would be compact and so thin counters can be realised in order to measure the specific ionization of a particle, $\frac{dE}{dx}$. Hence the particle can be identified by subsequently absorbing it completely and thereby measuring its total energy E. Secondly, the ionization energy of semiconductors is very much less than that of gases and so E may be determined with greater accuracy. In the case of silicon and germanium w, the mean energy absorbed per electron-hole pair released in the ionization process, is 3.6 eV and 2.9 eV respectively, compared with about 30 eV for gases and 300 eV per photoelectron in a scintillator photomultiplier combination. Hence the statistical fluctuations from silicon or germanium counters (proportional to $\sqrt{n}$, where n is the number of ionization events, see 3.3.1) will be reduced by a factor of $2\sqrt{2}$.

The action of a simple homogeneous counter can be explained with reference to Fig. 1.3. The incident radiation creates electron-hole pairs in the semiconductor and these are swept to the respective

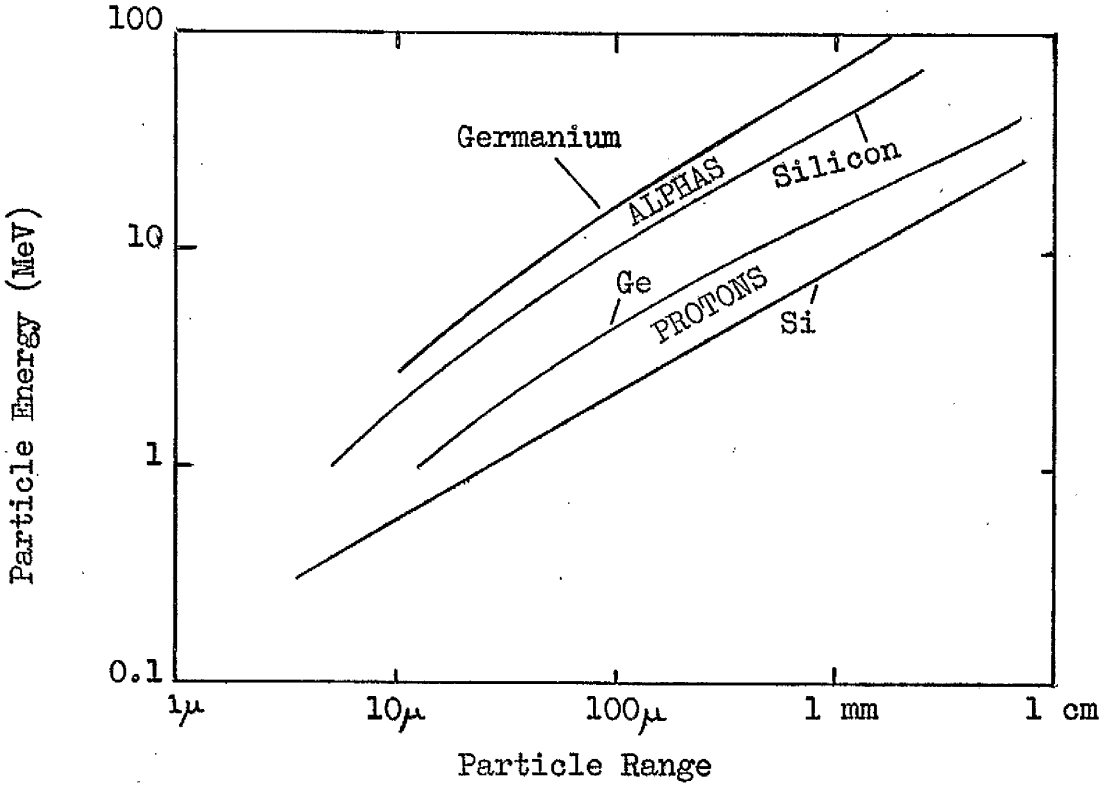

Fig. 1.1. Energy-range Relationship for Alphas and Protons in Silicon and Germanium. (Ref. 1, p. 7.)

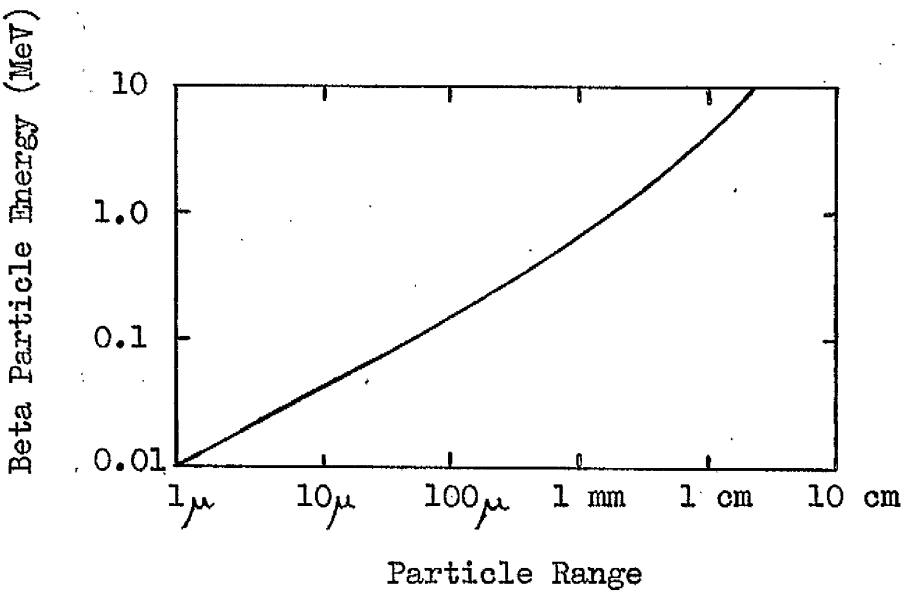

Fig. 1.2. Energy-range Relationship for Beta Particles in Silicon. (Ref. 1, p. 12.)

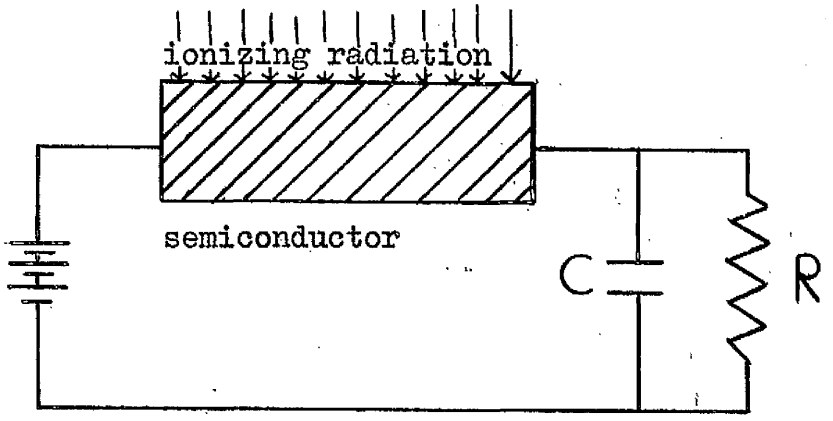

Fig. 1.3. Simple Homogeneous Counter.

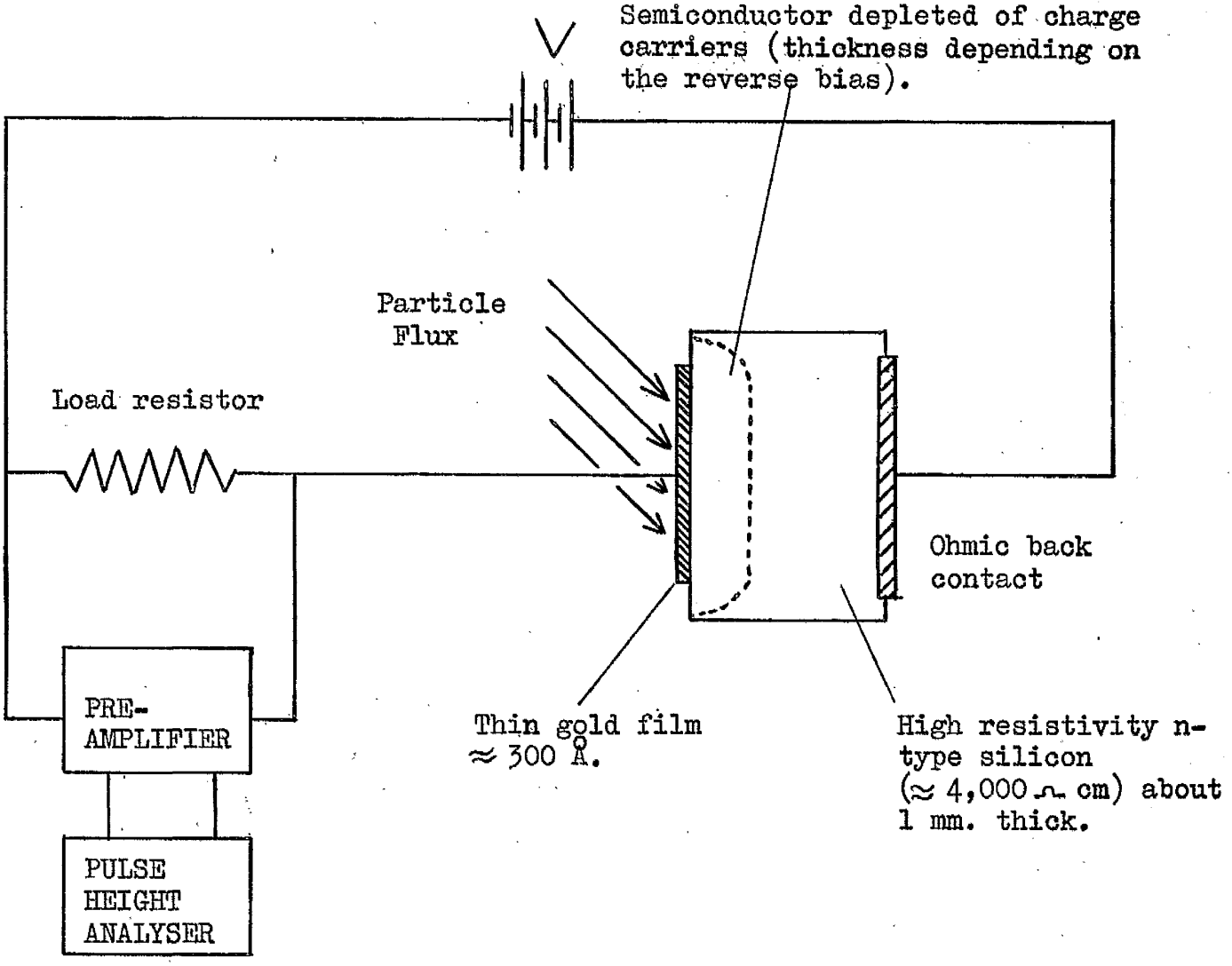

Fig. 1.4. Illustrating the Basic Structure and Operation of the Simplest Surface Barrier Detector.

electrodes by the applied field. Each electron-hole pair completely collected puts a charge $\pm e$ on the plates of the capacitor (assuming the mobility of the carriers is such that the transit time across the counter is less than the circuit integration time). In fact it is very difficult to achieve this situation in practice because both the resistivity of the solid and its dielectric relaxation time have finite values, thereby imposing many restrictions on the ideal case.

In particular thermally generated carriers may interfere with the charge collection and so reduce the signal to noise ratio. Also trapping centres or other localised sites may exist in the forbidden gap of the semiconductor and these will impede the movements of the holes and electrons. The criteria which govern whether a semiconducting material is suitable for a counter and the relative merits of various semiconductors are discussed fully elsewhere[1]. The chief parameters of the more familiar semiconductors which have been considered for use as counters are indicated in Table 1.1. The technology of silicon and germanium is highly developed and they are the only semiconductors which can be produced as single crystals of sufficiently high quality and size for use as counters. They possess long minority carrier lifetimes and large mobilities, but they are not suitable for use as homogeneous counters because their conductivities are too high and one has to resort to utilising the high field of the depleted region of a p-n junction in order to collect electron-hole pairs created by an ionizing event. However, the range of 5 MeV alpha particles in silicon is only about 20μ (Fig.1.1) and so if good resolution is to be obtained the p-n junction would have to be very near to the surface. This difficulty may be overcome by means of a

Semiconductor	Energy Gap (eV)	Electron Mobility ($cm^2 volt^{-1} sec^{-1}$)	Hole Mobility ($cm^2 volt^{-1} sec^{-1}$)	Electron Lifetime in p-type (sec)	Hole Lifetime in n-type (sec)	Atomic Number
Silicon	1.08	1500	500	3×10^{-3}	3×10^{-3}	14
Germanium	0.67	3800	1800	10^{-3}	10^{-3}	32
Diamond	$\sim$ 6	1800	1200			6
Gallium Arsenide	1.43	8500	420	10^{-7}	10^{-7}	31,33
Gallium Phosphide	2.25	140	150	10^{-8}	10^{-8}	31,15
Cadmium Sulphide	2.4	300	10	$\sim 10^{-3}$	$<10^{-8}$ limited by traps	48,16
Cadmium Telluride	1.5	$\sim$ 100	$\sim$ 100	4×10^{-5}	$>10^{-5}$	48,34
Indium Antimonide	0.17	78000	750	$\sim 10^{-7}$	$\sim 10^{-7}$	49,51
Gallium Antimonide	0.67	4000	1400	$\sim 10^{-8}$	$\sim 10^{-8}$	31,51

Table 1.1. Parameters of the more familiar semiconductors which have been considered for use as detectors. (Taken from ref. 1). All data is for 300°K.

suitable metal-semiconductor contact in which the semiconductor adjacent to the metal is fully depleted - this device is called a surface barrier detector. Actually the first semiconductor detector was neither of these devices but was a point contact diode.

In 1949 McKay[2] reported a novel method of detecting alpha particles. He used a point contact diode made by placing a phosphor bronze contact on a piece of n-type germanium. The output signal from the device was small because the sensitive area was only about 10^{-3}-10^{-2} cm diameter. In the same paper he suggested that if one utilised the built in field associated with a p-n junction then the sensitive area would be increased. Accordingly, in 1952[3] he used a germanium melt-grown p-n junction to measure w, the mean energy absorbed per electron-hole released in the ionisation process. He found w = 3.0 eV for germanium. At the same time Orman[4] was using germanium photovoltaic cells for the detection of alpha particles at Purdue University. Later, McKay[5] increased the signals from both germanium and silicon p-n junctions with controlled amplification by impact ionisation and found that for silicon, w = 3.6 eV.

These devices were small area detectors but in 1956 Mayer and Gossick[6] reported the use of a gold coated germanium detector as an alpha particle spectrometer. Experiments with cooled germanium devices were reported in 1958[7] and in 1959 Mayer[8] published data on a gold-germanium detector which could be operated at room temperature. This device consisted of a 500 Å gold film sputtered on a small piece of n-type germanium encapsulated in an epoxy resin. These so-called 'surface barrier' counters attracted much attention because of the good resolution and rise times reported and a simple model

based on a Schottky-type barrier was proposed to explain their behaviour.(9)

In 1959 McKenzie and Bromley(10), at Chalk River Laboratories, reported the use of silicon surface barrier counters for the first time. These exhibited comparable resolutions to the germanium detectors and could be operated satisfactorily at room temperature. (This was not surprising since Eg for silicon is 1.1 eV compared with 0.7 eV for germanium). They also claimed that phosphorus diffused p-n junction radiation detectors showed comparable resolution.

The silicon surface barrier diodes were attractive for three reasons. First, the charge depletion layer (which is the sensitive volume of the device) began essentially at the gold electrode so that relatively short range particles (e.g. alphas) could be easily detected. Secondly, if pure, high resistivity silicon was utilised then the depletion region would extend further into the semiconductor at reasonable reverse voltages and so more energetic particles could be counted. Thirdly, they operated at room temperature. Much of the effort since 1960 has been devoted to improving the performance of such devices.

The basic construction of a surface barrier counter is shown in Fig. 1.4. A thin gold layer (about 300 Å) is evaporated onto a chemically etched slice of n-type silicon which has an ohmic back contact. A high field depletion region is formed in the silicon, the thickness of which depends on the reverse bias applied to the device. An energetic particle enters this region (preferably through the gold electrode) and is arrested instantaneously (10^{-12} sec). The hole-

electron pairs liberated in the ionisation processes are collected by the electrodes in a time less than the dielectric relaxation time of the depleted silicon. If the time constants of the associated electronic equipment are correctly set then rise times of at most 10n sec are usual.

Semiconductor counters of the highest performance are surface barrier devices in which evaporated metal films are used to make ohmic and rectifying contacts to semiconductor surfaces. The correct physical description of these counters has never been determined, and perhaps because of this the yield of the process and the reliability and life of the devices falls far short of p-n junction counters of slightly inferior performances.

The purpose of the present work is to investigate in detail the structure and properties of evaporated metal films on silicon and the properties and ageing characteristic of the contacts so formed, paying particular attention to the materials used conventionally in semiconductor counter technology.

Metal-semiconductor contact theories are discussed more fully in Chapter 2 and the specific problems encountered with operational surface barrier detectors are summarised in Chapter 3.

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(3) K. G. McKay. Phys. Rev., 84, p. 829 (1951).

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Chapter 2

Metal-semiconductor junction theory, recent research and real semiconductor surfaces

2.1 Introduction

A considerable amount of literature has appeared on metal-semiconductor junctions over the last seventy years and this was excellently reviewed up to 1955 by Henisch[1]. Recently both Turner[2] and Mead[3] have covered the period 1955-67.

2.1.1 Historical development of devices

Metal point contacts on natural crystals were investigated in 1874[4] but it was not until 1904 that point contact rectifiers were used in radio telephony[5]. Silicon and germanium detectors were developed rapidly during the period 1940-45 but the advent of the transistor in 1950 tended to retard their development. However, transistor action has been obtained using metal-semiconductor surface barriers formed by electro-plating metals on semiconductors[6]. Since 1950 much effort has been concentrated into obtaining reproducible semiconductor surfaces (using single crystal materials) and subsequently metal-semiconductor junctions have been developed for nuclear particle detectors, field effect transistors, hot electron diodes and metal base transistors.

2.1.2 Development of modern rectification theories

In 1931 Wilson[7] explained the behaviour of semiconductors

in terms of the band theory of solids and this paved the way to a general understanding of metal-semiconductor contacts. At first specific problems were attacked, notably that of the cuprous oxide rectifier by Mott[8] in 1939 and later Schottky[9] put forward a more general theory suggesting that a potential barrier could arise from the stable space charges within the semiconductor due to the presence of a metal. Basically his idea was that if a semiconductor material, whose work function was less than that of a metal, was brought into contact with the metal then the electrons in the conduction band of the semiconductor, being at a higher energy level, would flow into the metal. Thus the semiconductor would be depleted of electrons and a positive space charge would build up in the semiconductor. Hence two space charge regions, one on either side of the interface, would be built up and this electric field would oppose any further flow of electrons. The magnitude of the potential barrier so formed was just equal to the difference in work functions of the two materials. For an n-type semiconductor the carrier concentration is very much less than that in the metal and so the space charge region extends much deeper into the semiconductor. (Fig. 2.5). This space charge region is called the depletion region. In 1942 Schottky[10] pointed out that such a model predicted a voltage-dependent capacitance for the metal-semiconductor contact, which was in agreement with experimental results.

Current-voltage characteristics were explained by a majority carrier diffusion process within the depletion region, but in 1942

Bethe[11] noted that this applies only when the depletion region is very thick compared with the mean free path of the carriers concerned. His diode theory assumes that carrier collisions within the barrier region can be neglected.

Results published by Meyerhof[12] in 1947 concerning metal point contacts on silicon and germanium did not agree with the predictions of the Schottky model and this led Bardeen[13] to propose that this lack of correlation was due to the presence of surface states within the forbidden energy band of the semiconductor.

Tamm[14] and Shockley[15] had both shown the theoretical validity of these discrete surface states a decade earlier and Bardeen proposed a new mechanism of barrier formation. This involved a charge double layer at the free surface of a semiconductor formed by a net charge from electrons in surface states and a space charge of opposite sign extending into the semiconductor. Brattain and Bardeen[16] confirmed this theory with experiments on surfaces of germanium and silicon. This idea enunciated by Bardeen is still the basis of modern metal-semiconductor junction theory.

2.2 Metal-semiconductor junction theory

2.2.1 Free metal surface

Although we define the thermionic work function of a metal, ϕ_M, to be the difference in energy between an electron at rest in a vacuum just outside the metal and an electron at the Fermi level (Fig. 2.1), this does not imply an abrupt change in potential at the

interface - in fact an electron outside the metal induces a positive charge on the metal surface and is thus attracted to it. This image force is equal to $\frac{e^2}{16\epsilon\epsilon_o\pi x^2}$ for an electron a distance x from the metal surface.

It is well known that the potential energy of the electron (Fig. 2.2) is given by

$$V_{image} = -\frac{e^2}{16\pi\epsilon_o x} \qquad (2.1)$$

(See Glossary of Symbols.)

When x is very small, i.e. comparable to atomic distances, this relationship is obviously not valid and for values of $x < x_o$ a constant force is assumed (region A - B) in Fig. 2.2(a).

If an electric field, F, is applied to the metal surface in order to draw electrons from the metal (Schottky Effect) then the effective work junction of the metal is reduced by an amount

$$\Delta \phi_M = -e\left[\frac{eF}{4\pi\epsilon_o}\right]^{\frac{1}{2}} \qquad (2.2)$$

This is shown in Fig. 2.2(b).

Moreover, if a monatomic layer of a foreign metal is adsorbed on the metal surface a charged double layer is established, resulting in a further lowering of the work function. The transmission of electrons through such barriers is well documented.[17]

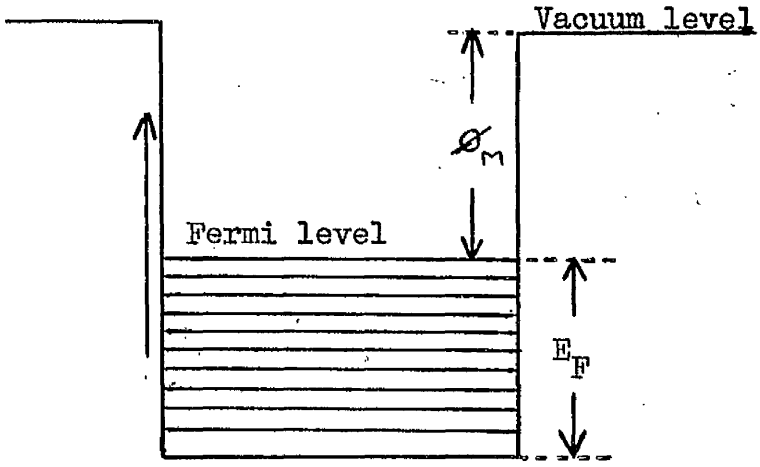


Fig. 2.1. Free Metal Surface.

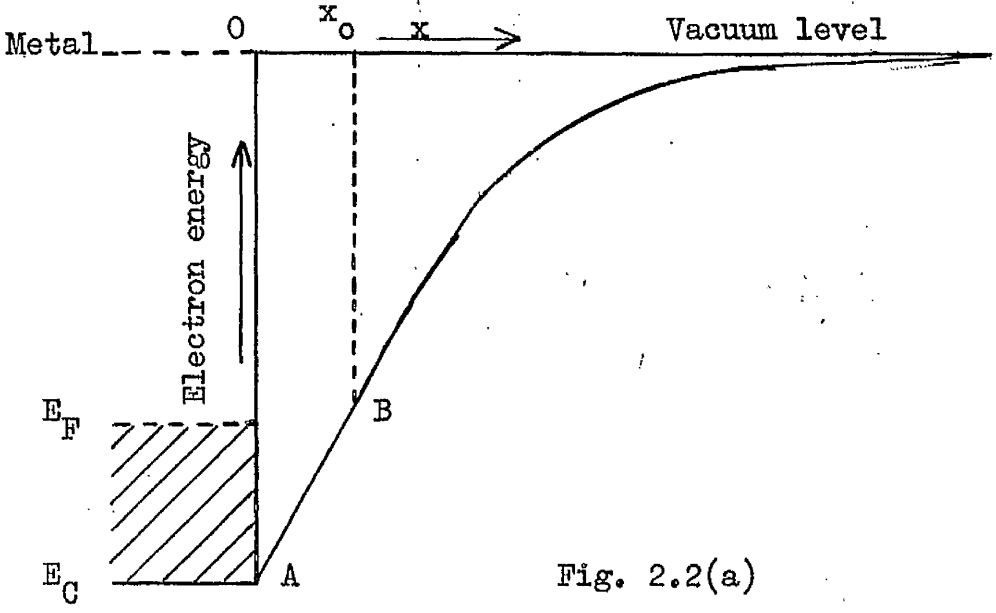


Fig. 2.2(a)

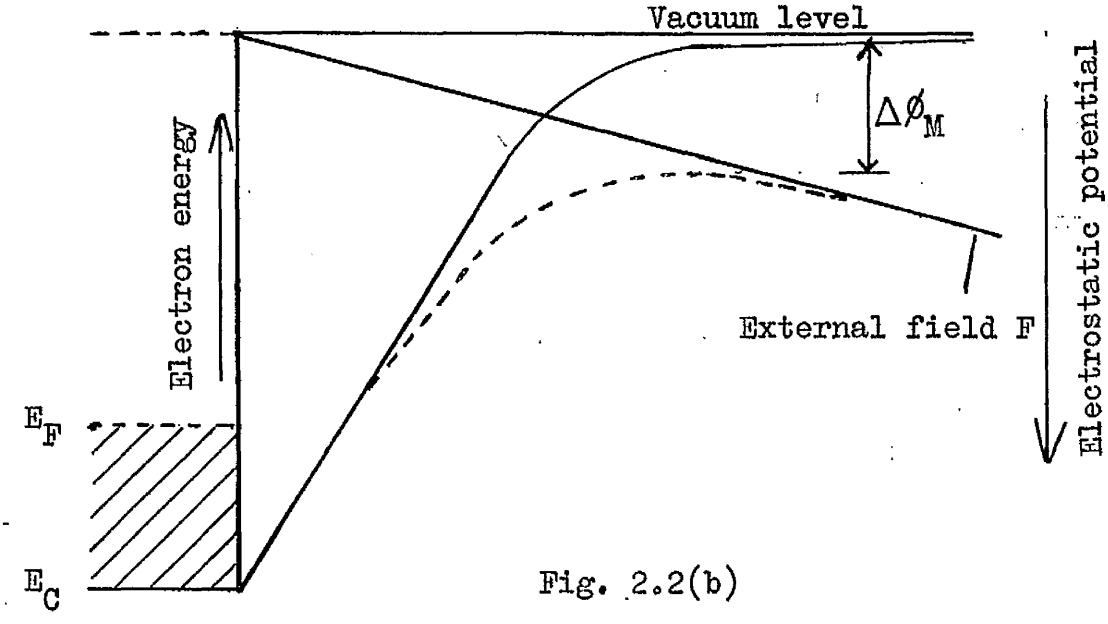


Fig. 2.2(b)

Fig. 2.2(a). Potential Energy of Electron near Metal Surface.
2.2(b). Schottky Effect on Work Function Lowering.

2.2.2 Free semiconductor surface (n-type)

2.2.2.1 No surface states

Fig. 2.3 defines the work function, ϕ_s, of a semiconductor. However, the Fermi level is a variable level in the semiconductor band gap and so it is more usual to refer to the electron affinity, X_s, which is the difference in energy between the bottom of the conduction band and free space.

2.2.2.2 With acceptor-like surface states

The effect of the termination of the crystal lattice on the solutions of the Schrödinger wave equation led both Tamm[14] and Schockley[15] to postulate the existence of allowed energy levels within the forbidden band for a semiconductor. These levels would be localised at the surface. According to Shockley if the lattice spacing is small then one discrete surface state should arise for each surface atom, i.e. about 10^{15} states cm^{-2}. The actual surface charge density will be influenced by adsorbed impurities which can either act as energy states or affect their occupancy. Recently, Many et al.[18] have given a full theoretical treatment of semiconductor surface states and their occupation statistics.

Fig. 2.4(a) shows the non-equilibrium situation with the surface states filled up to some value ϕ_o above the valence band with the remaining empty ones distributed over the energy gap. Since there are states empty below the Fermi level some conduction electrons fall into them, thereby charging the surface negative. Thus a positive

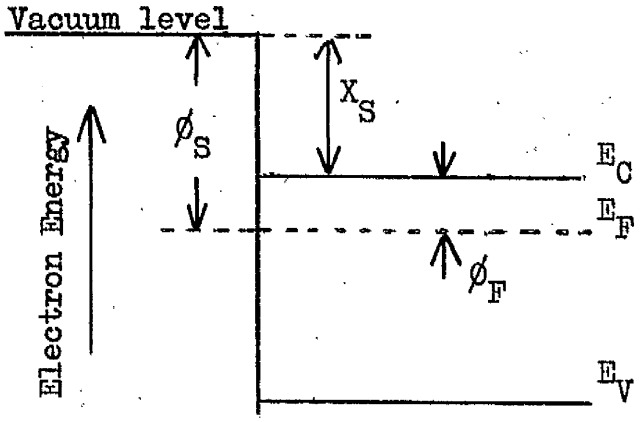


Fig. 2.3. Free surface of an n-type semiconductor with no surface states.

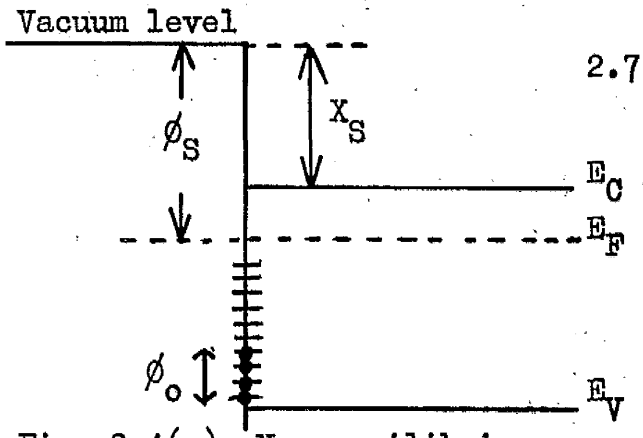


Fig. 2.4(a). Non equilibrium.

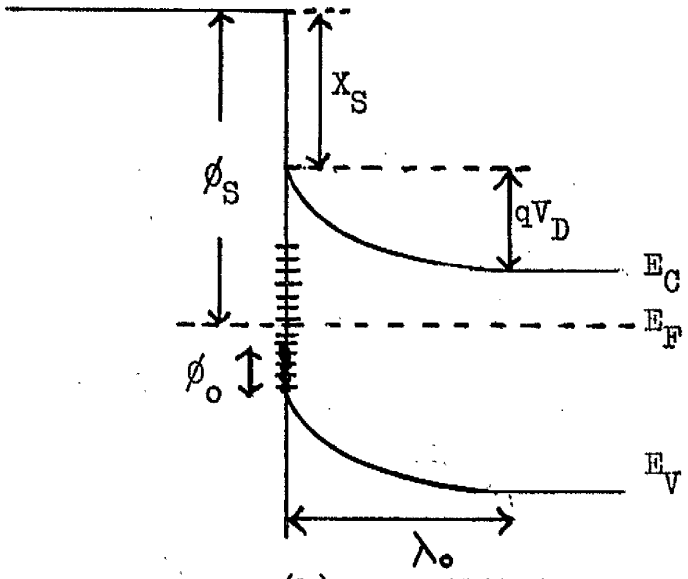


Fig. 2.4(b). Equilibrium.

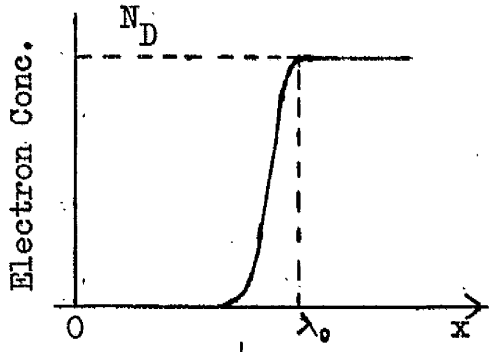


Fig. 2.4(c) Electron concentration.

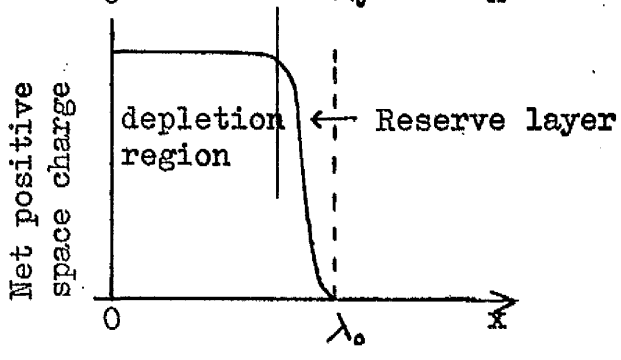


Fig. 2.4(d) Charge distribution

Fig. 2.4. Conditions for n-type semiconductor with acceptor-like surface states.

space charge layer forms in the body of the semiconductor due to the depletion of electrons and consequently the energy bands at the surface bend upwards with respect to the Fermi level until equilibrium is attained (Fig. 2.4(b)). The height of the potential barrier formed by the charge transfer can be calculated by solving Poisson's equation within the depleted region of the semiconductor. This yields

$$V_D = \frac{eN_D\lambda_o^2}{2\epsilon\epsilon_o} \qquad (2.3)$$

A similar result is obtained for donor-like surface states which lie above the Fermi level except in this case the bands bend downwards.

There is a gradual transition from the fully depleted region to the region of bulk ionisation in the semiconductor and this is referred to as the reserve region - Figs. 2.4(c) and 2.4(d). In the case of silicon we are only interested in this region when considering low barriers.

2.2.3 Equilibrium between a metal and semiconductor

2.2.3.1 Without surface states ($\phi_M > \phi_S$).

Fig. 2.5(a) - (d) shows the various stages involved in aligning the Fermi levels when a metal and an n-type semiconductor are brought into contact. A Schottky barrier is formed as described in 2.1.2. This is a similar process as in 2.2.2.2 except here the negative charge resides in the metal instead of in the surface states. From Fig.2.5.it is evident that

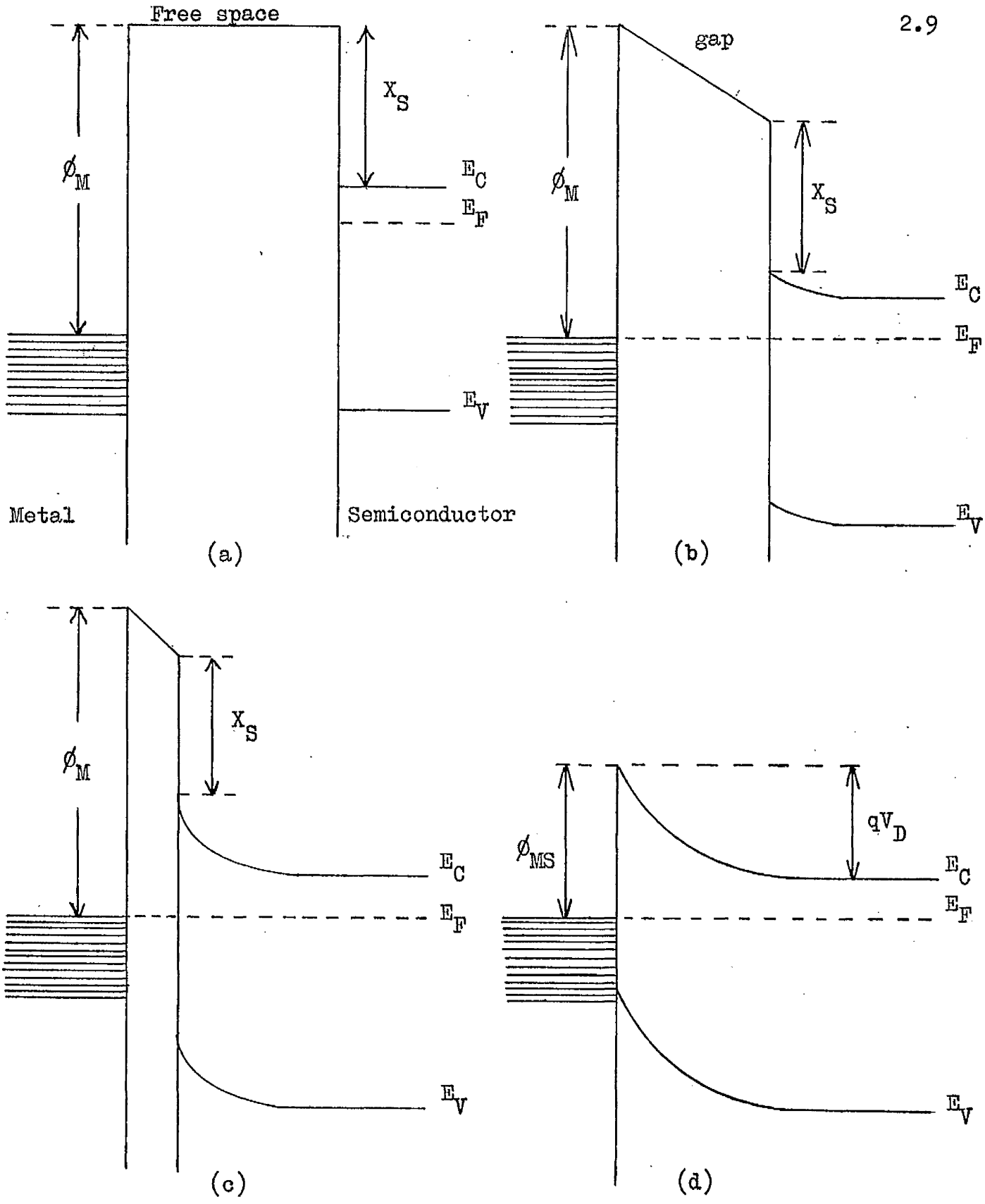


Fig. 2.5. Metal-semiconductor contact with no surface states.
(a) Non-equilibrium.
(b) Equilibrium gap diminishing.
(c) Equilibrium gap diminishing.
(d) Limiting condition.

$$\phi_{MS} = \phi_M - \chi_S \tag{2.4}$$

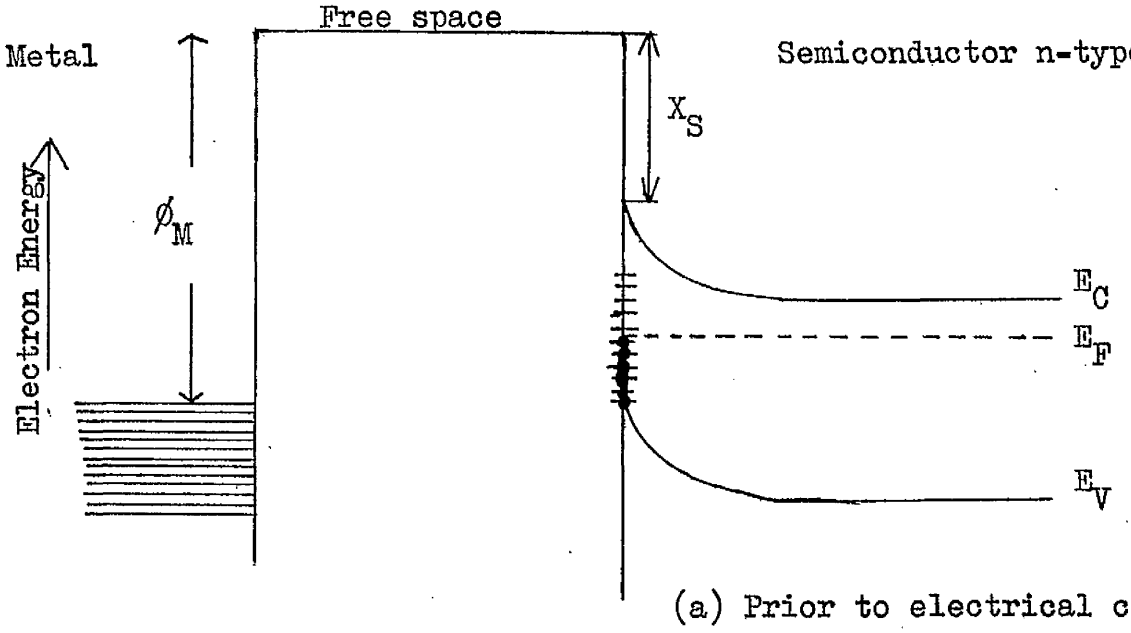
or $$eV_D = \phi_M - \chi_S - \phi_F \tag{2.5}$$

2.2.3.2 With surface states (acceptor)

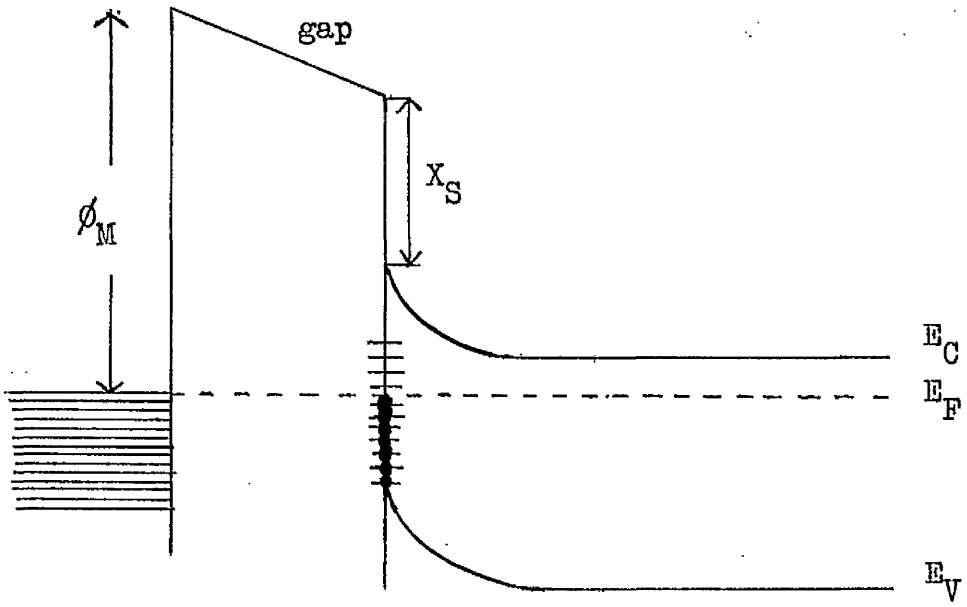
The energy bands of the semiconductor will already be bent upwards if the surface states are appropriately located with respect to the Fermi level (Section 2.2.2.2). As the metal and semiconductor are brought together (Fig. 2.6) the Fermi levels will coincide and the energy bands bend upwards only slightly more. The actual amount of bending will depend on the amount of charge that the surface states can accomodate. The main point is that some of the electrons leave the surface states and enter the metal and the contact potential is dropped almost wholly across the vacuum δ. The field due to the contact potential is terminated by the surface states which appear to screen the bulk of the semiconductor from external effects. We can consider the charge at the metal surface, Q_M, to be balanced by an equal charge partly in the semiconductor, Q_{SC}, and partly in the surface states, Q_{SS}, such that

$$-Q_M = Q_{SC} + Q_{SS} \tag{2.6}$$

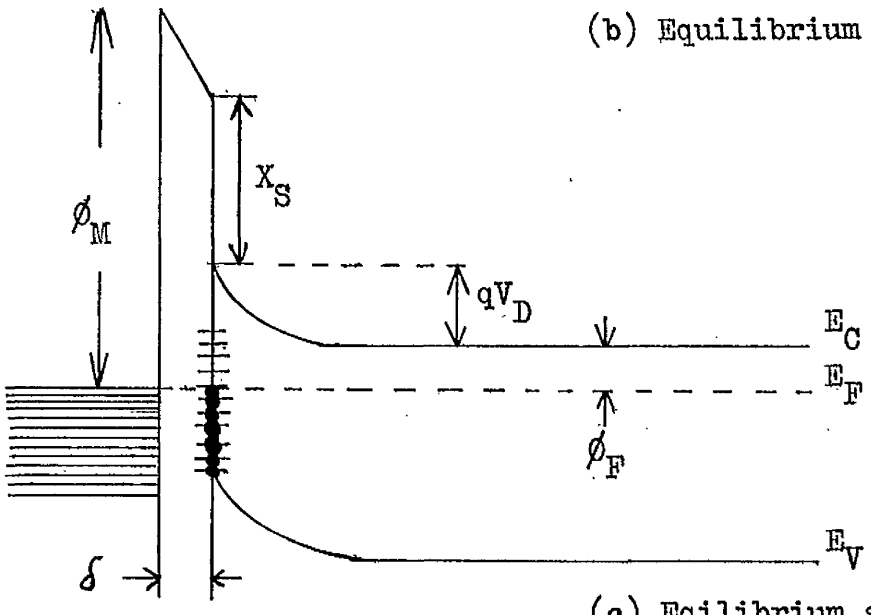
Bardeen[13] has dealt fully with the various cases that arise due to a variation in the density of the surface states and the magnitude of δ.



(a) Prior to electrical contact.



(b) Equilibrium large gap.



(c) Eqilibrium small gap.

Fig. 2.6. Metal-semiconductor contact with surface states (acceptor).

2.2.4 Current-voltage relationship

The rectification characteristic of metal-semiconductor junctions can be derived in several ways and has been done elsewhere[1,2,19]. The two main approaches to the problem are:

(a) Bethe's diode theory[11] which is valid for high barriers in which the mean free path of the electrons in the semiconductor, l, (i.e. the average distance travelled by the carrier between successive collisions with the lattice) is large compared with the distance d within the barrier in which the potential changes by kT. In silicon $l \sim 10^{-5}$ cm and so this theory[2] is restricted to the carrier range

$$10^{14} < N_D < 10^{18} \text{ donors cm}^{-3}.$$

(b) Diffusion theory which assumes the current flow across the barrier is a diffusion process and so d is large compared with l.

This means if we wish to apply these theories to nuclear detectors we should use diffusion theory because for 4,000 Ω-cm n-type silicon (which is typical of the silicon resistivity used in device manufacture) $N_D \approx 10^{12}$ donors cm^{-3}.

For nuclear detector application we are primarily interested in the reverse characteristic of metal-semiconductor junctions and so a fuller discussion of reverse current mechanisms is included in Chapter 3.

We should also note that it has become the practice[20,21] to regard a metal-semiconductor device used in nuclear radiation

detection as a p-n junction when the surface layer of the semiconductor has become inverted (2.3.3). Here the metal is regarded as a means of making contact to this inversion layer. Ordinary p-n junction theory is then applied.

All theories neglect the 5 - 20 Å oxide layer at the metal-semiconductor interface and regard it as transparent to electrons. To a first approximation the theories arrive at a current-voltage relationship given by

$$I = I_S \left[\exp. \left(- \frac{eV_A}{nkT} \right) - 1 \right] \qquad (2.7)$$

where n = 1 in the case of an ideal diode.

2.3 Real semiconductor surfaces

A semiconductor surface cannot be regarded merely as an abrupt cessation of the regular periodicity of the crystal lattice and it is known that the electron states in the region of the surface are not the same as those of the bulk material (2.2.2.2). Surfaces may be prepared and studied in two distinct ways. First of all there are "clean surfaces" which are the best approximation to any idealised model and are prepared by either cleaving or elaborate cleaning in ultra high vacuum. Secondly, there are "real surfaces" which are surfaces prepared under normal laboratory conditions by polishing followed by chemical etching. All work referred to in this thesis was done on real surfaces because these are the surfaces we are interested in regarding device manufacture and operation.

There is a vast literature covering work on real surfaces (Many et al,[18] list 411 references on the topic alone!) and I shall only attempt to summarise results that are important to our investigations.

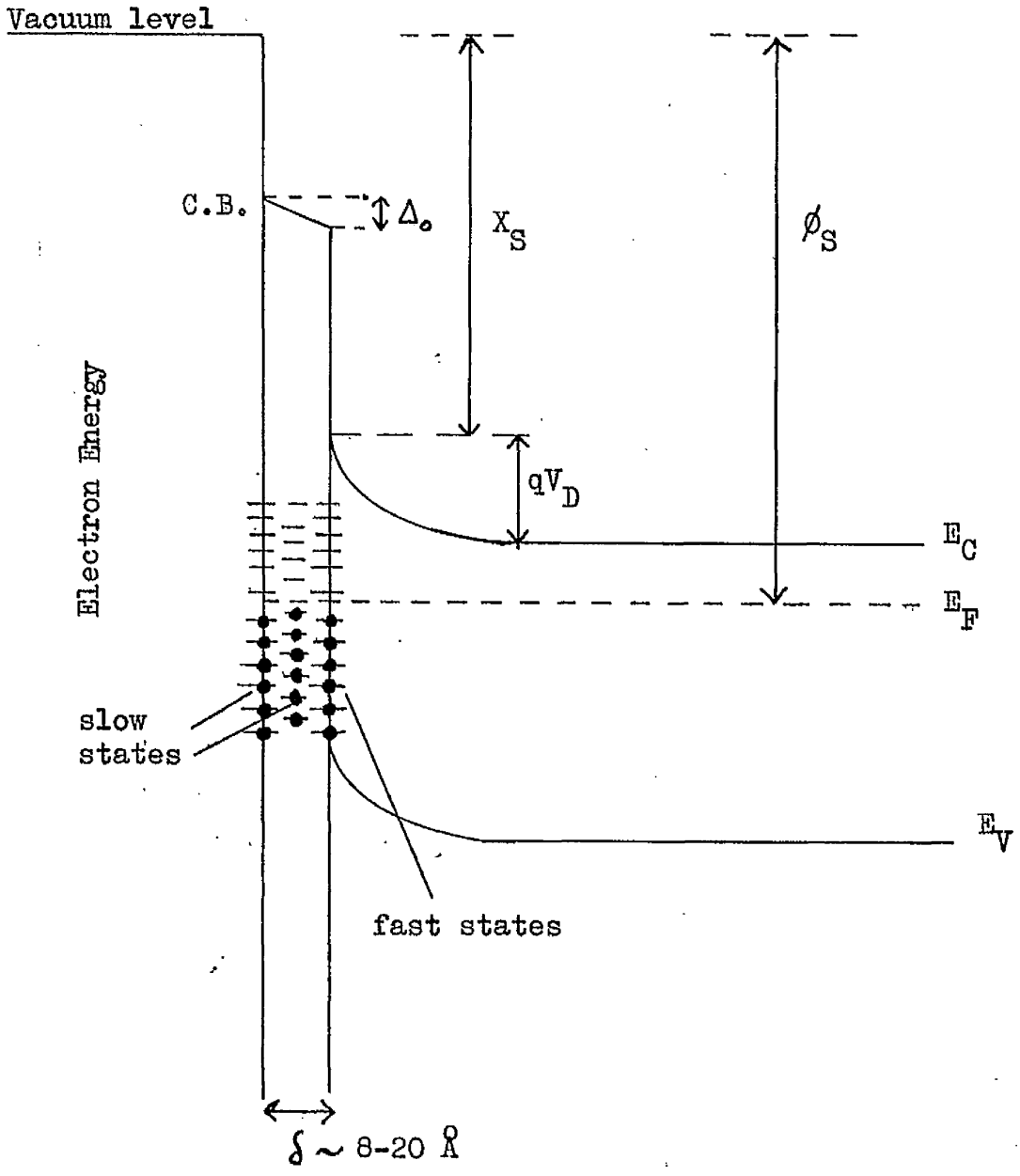
2.3.1 Model of the real semiconductor surface

The idealised model of the free semiconductor surface (2.2.2.2) has only to be modified slightly to include the case of the real semiconductor surface. This is shown in Fig. 2.7.

For silicon the oxide thickness will depend on the exposure time of the surface to the atmosphere following etching[22] and can be < 10 Å (4.4.2). This oxide layer and the surface proper are the sites of the localised electronic states whose occupation can be varied by changing the gaseous or liquid environment.

Silicon and germanium exhibit two distinct types of surface states - fast states located at the semiconductor-oxide interface which are characterised by transition times between the states and the bulk $\approx 10^{-6}$ sec. and slow states distributed within the oxide and at its outer surface and characterised by time constants $\approx$ seconds or longer.

Brattain and Bardeen[16] measured the contact potential and surface photovoltage of etched germanium surfaces and showed how the barrier height, V_D, (or surface potential ϕ_D, Fig. 2.7) could be varied.



Δ_o is the potential drop across the oxide due to distribution of charge in slow states. (Included in electron affinity of semiconductor because it is negligible.)

Fig. 2.7. Energy level diagram of a free real semiconductor surface.

2.3.2 Etched silicon surfaces

For real silicon surfaces the density of fast states $\approx 10^{11} - 10^{12}$ cm^{-2} compared with a density of surface atoms $\approx 10^{15}$ cm^{-2}, indicating a nearly perfect matching between the semiconductor and its oxide. Here the fast states are regarded as due to the incomplete bonding and mismatch between the oxide and semiconductor lattices. Impurities and lack of stoichiometry in the first few oxide layers may also be sources of fast states. The slow state density for silicon $\approx 10^{13}$ cm^{-2} and these states are considered to originate in ions adsorbed from ambient gases.

Many et al.[23] have emphasised the importance of simultaneous measurements of contact potential and surface conductance in order that changes in work function arising from altering a gas ambient can be correlated with both changes in surface potential and changes in electron affinity associated with electric dipoles of adsorbed species. In fact experiments indicate that the adsorbed molecules on etched surfaces do not possess electric dipoles.

2.3.3 The surface potential of silicon surfaces following treatments used in nuclear detector fabrication

Etched silicon surfaces exhibit high values of the surface recombination velocity S ($\approx 10^{3} - 10^{4}$ cm sec^{-1}) so that the effective lifetime of a silicon wafer may be very much less than that of the bulk carrier lifetime.

Buck and McKim[24] investigated how the surface conductivity and the surface recombination velocity of n-type silicon varied for different ambients and surface treatments. These surface treatments are identical to those used in the manufacture of surface barrier detectors before the evaporation of the gold layer. The treatments consisted of soaking HF/HNO_3 etched wafers in the following solutions:

(i) Warm sodium dichromate.

(ii) Boiling deionised water.

(iii) Concentrated HF.

(iv) Ordinary quench of HF/HNO_3 etch in cold deionised water.

The results have been summarised by Holmes[25] and are shown in Fig. 2.8(a), (b). The main points are that

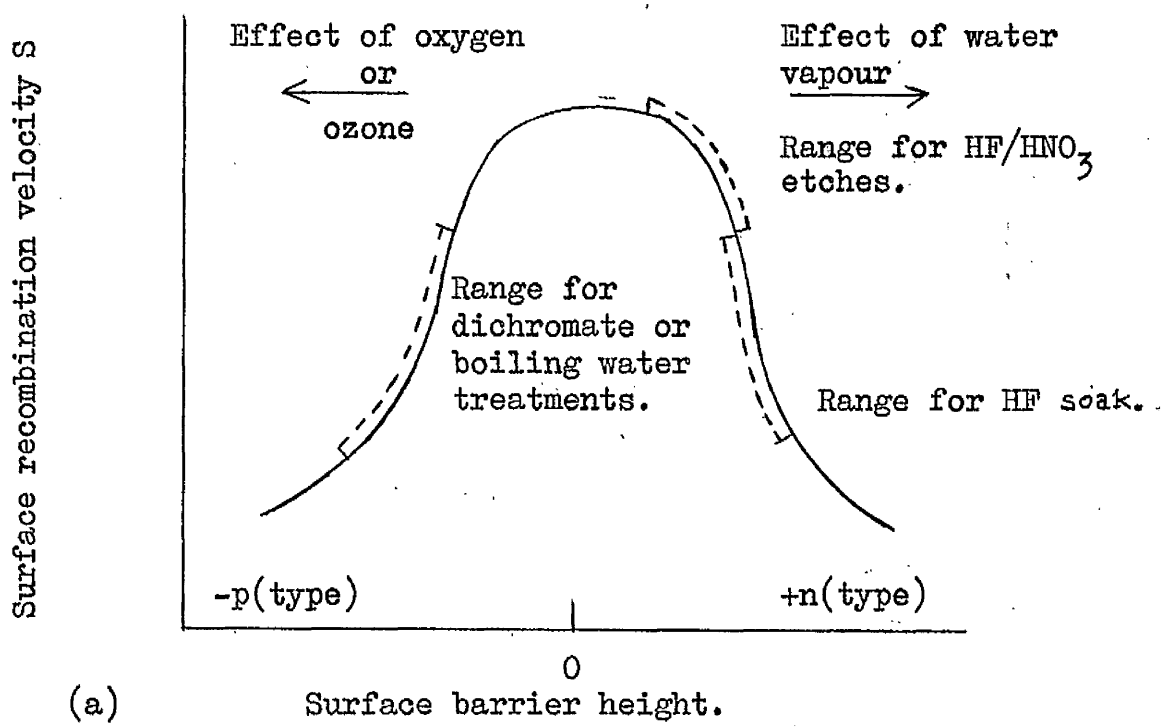
(1) Both oxygen ambients and surface treatments in sodium dichromate solution and boiling deionised water tend to invert the surface, i.e. give the n-type silicon a p-type surface layer and thereby a higher surface potential.

(2) The above treatments also reduced S to about 40 cm sec^{-1}.

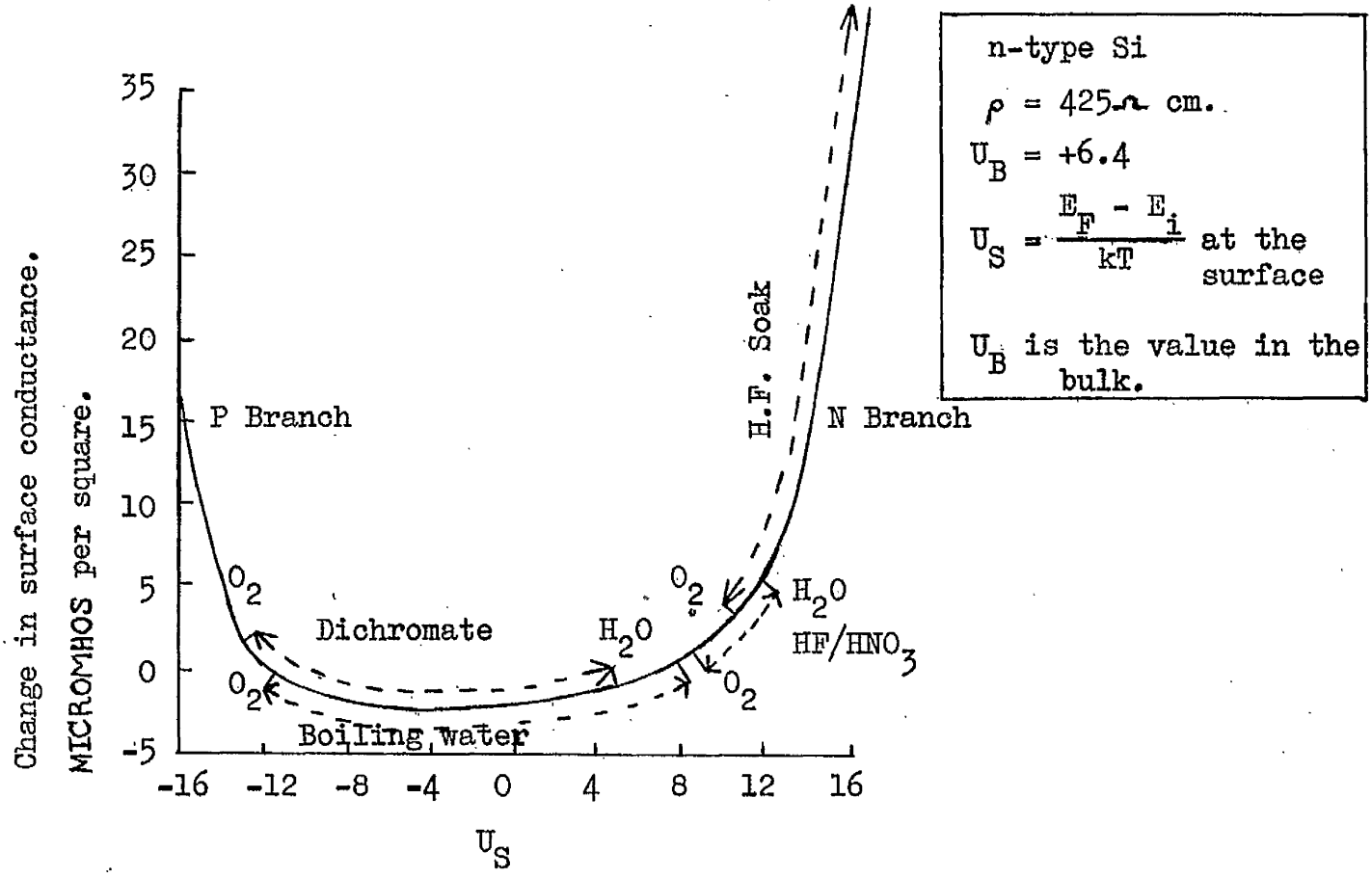
(3) The HF/HNO_3 etch was little affected by ambients and preserved the n-type character of the silicon, but S was large (10^4 cm sec^{-1}).

(4) The HF soak initially left the surface strongly n-type with a low S but after exposure to oxygen the surface tended to behave as in (3).

(5) Physically adsorbed water vapour tended to leave all surfaces more n-type.



(a)



(b)

Fig. 2.8. (a) Effect of ambients on surface recombination velocity and surface potential for n-type silicon. (Taken from ref. 25).
(b) Surface conductivity versus U_S. (Taken from ref. 24).

These shifts in potential are thought to be brought about either by a change in occupation of a constant number of surface states or the activation or passivation of existing defect centres. Excess oxygen appears to be an activating agent which brings the centres and hence the states associated with them inside the forbidden gap whereas physically adsorbed water acts as a neutralising species which induces the centres to shift into an ineffective position.

2.4 Recent research on metal-semiconductor contacts

A considerable amount of research has been carried out on metal-semiconductor contacts in the last four years, probably due to the interest in the metal base transistor. Measurements of the barrier height, ϕ_{MS}, have been made for a variety of metals evaporated on both etched and cleaved surfaces[2,3] and attenuation lengths of hot electrons in various metal films have been measured using the semiconductor as a collector[26,27,28]. This has resulted in an accumulation of information regarding surface states and metal-semiconductor junctions. Consequently there has been much speculation regarding the correlation of metal-semiconductor barrier height with metal work function and the effect of surface states. The literature was reviewed recently[3].

In this laboratory, M. J. Turner has made exhaustive measurements of the diffusion potential (V_D) for various metals evaporated on both etched and cleaved silicon[2]. His conclusions regarding metal-silicon contacts are as follows:

(1) For etched surfaces, ϕ_{MS} varies with the work function of the metal. The effect of the surface states is small and so the simple Schottky theory is approximately obeyed.

(2) For cleaved surfaces the surface state density is the important parameter making ϕ_{MS} independent of the work function of the metal.

All of the work referred to above has been carried out on small area devices utilising low resistivity semiconductors. We will see in the next chapter that these devices do not meet the requirements of surface barrier nuclear detectors. Nevertheless the fundamental ideas and experimental results are of the utmost importance.

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Chapter 3

Surface Barrier Detectors

We have seen how a surface barrier detector operates (Chapter 1) and the physical processes involved in making a metal-semiconductor contact and how this depends on the state of the semiconductor surface (Chapter 2). Whether a metal-semiconductor contact is a useful device for detecting nuclear particles depends primarily on its energy resolution. In this chapter the factors governing the resolution of a detector and how one achieves an acceptable noise level are considered. The latter half of the chapter concerns device manufacture and associated problems.

3.1 Depletion layer thickness and diode capacitance

If the metal-semiconductor junction is considered to be a simple Schottky barrier with donor centres uniformly distributed and fully ionised, then the depletion width, λ, can be found by solving Poisson's equation[1] to yield

$$\lambda = \left[\frac{2(V_D + V_A)\epsilon\epsilon_o}{N_D e} \right]^{\frac{1}{2}} \qquad (3.1)$$

For n-type silicon, $\lambda = 5.3 \times 10^{-5} \left[\rho(V_D + V_A)\right]^{\frac{1}{2}}$ cm when the resistivity ρ is in Ω cm and $(V_D + V_A)$ in volts.

It is obvious that for long range particles when λ will need to be large that it is beneficial to use high resistivity silicon.

Again for the case of a Schottky barrier, with a contact area A, the depletion layer capacitance is given by

$$C_{dep} = A\left[\frac{2\epsilon\epsilon_o N_D e}{(V_D + V_A)}\right]^{\frac{1}{2}} \tag{3.2}$$

and the incremental or differential capacitance, $^{dQ}/_{dV}$ is given by

$$C_{inc} = A\left[\frac{\epsilon\epsilon_o N_D e}{2(V_A + V_D)}\right]^{\frac{1}{2}} \tag{3.3}$$

The refinements necessary to take into account charge in surface states have been dealt with elsewhere[2].

3.2 Operation of counter

The effective circuit of an operational counter is shown in Fig. 3.1. The time constant of the circuit is given by $\tau = CR$, where $C = C_d + C_s$ and $R = \frac{R_L R_D}{R_L + R_D}$ (3.4)

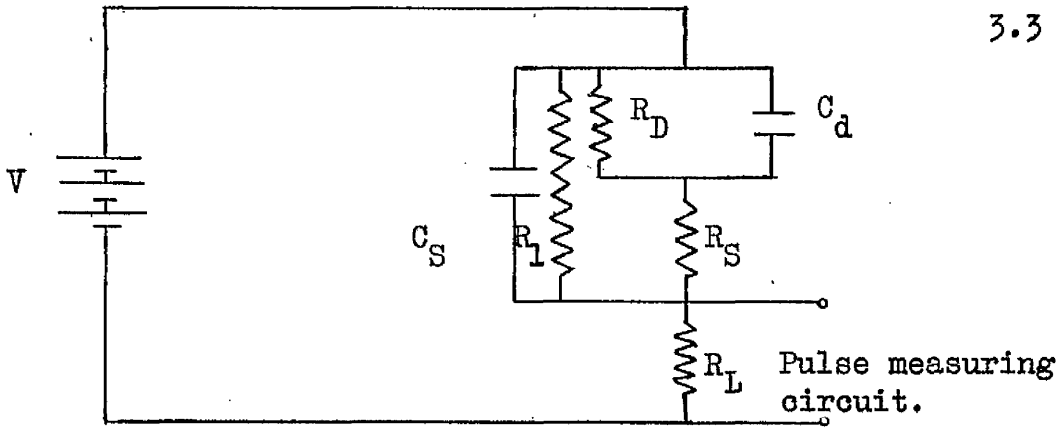
In practice $\tau > \tau_c$, where τ_c is the charge collection time for both carriers, and $\tau < \tau_o$ the dielectric relaxation time of the semiconductor. For reverse voltages greater than 10 V, R_D is typically about 100 MΩ.

3.3 Resolution criteria

3.3.1 Statistical limitation

When an energetic particle releases N ion pairs in a perfect detector then the charge collected $\bar{q}$ is given by

$$\bar{q} = Ne \tag{3.5}$$



(a)

C_d = diode capacitance.

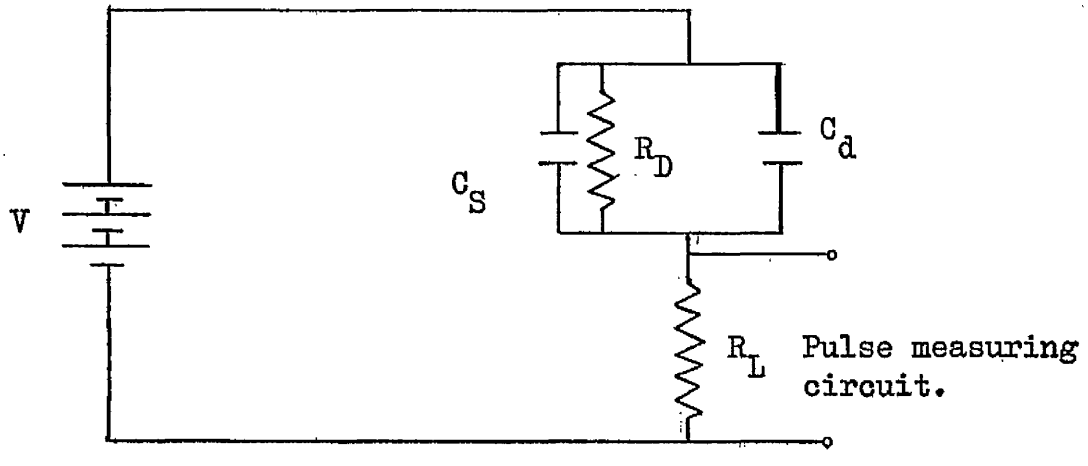
R_D = dynamic resistance of diode.

R_S = series resistance of diode.

R_l = leakage resistance of diode.

R_L = lead resistor.

C_S = stray capacitance.



(b)

Fig. 3.1. (a) Actual effective circuit of a counter.
(b) Effective circuit of an operational counter.

For N entirely independent events then the statistical deviation, σ_N, in N is $\sqrt{N}$, but in the case of related events σ_N is $\sqrt{FN}$, where $F = \sigma_N^2/N$ and is called the "Fano factor"(3).

The standard deviation of $\bar{q}$ is therefore σ, where

$$\sigma = e\sqrt{FN} \tag{3.6}$$

and the resolution of a counter, R, due to these fluctuations is defined by

$$R = \frac{\sigma}{\bar{q}}$$

$$= \sqrt{\frac{F}{N}} \tag{3.7}$$

Three ways are used to express R.

(a) For a particle energy W and a mean energy per ion pair w, $N = \frac{W}{w}$

so $$R = \sqrt{\frac{Fw}{W}} \tag{3.8}$$

In silicon w = 3.6 eV and if W = 1 MeV and F = 1 (worst case) R is 0.19%.

(b) The resolution is often expressed as the energy of a particle which would produce a signal equal to σ i.e. $\frac{\sigma}{e}$. w.

$$\frac{\sigma_w}{e} = \sqrt{FwW} \tag{3.9}$$

Again for 1 MeV particles in a silicon counter with F = 1 the resolution is 1.9 keV.

(c) The most common method used is to plot the pulse height spectrum obtained when particles from a mono-energetic source are incident upon the counter and measuring the full width of this distribution at its half maximum values (FWHM). This is expressed either as a ratio or percentage of the peak value or as an energy. If the pulse height spectrum is Gaussian the FWHM is 2.35 times the resolution defined above for the standard deviation.

These values give the worst resolution possible (if F = 1) due to the fluctuations in N alone and this may be insignificant compared with the noise contributions from the following sources.

3.3.2 Incomplete charge collection

This is generally much smaller than 3.3.1 provided one arranges for the charged particles to be incident through the gold electrode. The geometrical effects of incomplete charge collection have been discussed elsewhere[4].

3.3.3 Thermal noise

All noise is expressed as the energy of an ionising particle, ΔW, which would produce a signal equal to the r.m.s. noise. In the case of thermal noise or Johnson noise which arises because the velocity distribution of the carriers leads to a fluctuating distribution of the carriers in the conductor ΔW is given by[4]

$$\Delta W = \frac{W}{e} (kTC)^{\frac{1}{2}} \qquad (3.10)$$

where k is Boltzmann's constant and $C = C_d + C_s$.

For silicon at room temperature

$$\Delta W = 1.4\ C^{\frac{1}{2}}\ \text{keV} \qquad \text{when C is in pF.}$$

Typically, for a 1 cm^2 surface barrier diode of 4,000 ohm cm. n-type silicon operating at 10 V reverse bias for alpha detection, C would be $\simeq$ 100 pF. Hence, Δ W = 14 keV (or FWHM 31 keV) and so if possible it is best to operate at higher reverse voltages in order to reduce this source of noise.

3.3.4 Current noise

This arises due to the discrete movements of holes and electrons within the counter. All processes which tend to disrupt the movement of the carriers such as trapping or recombination will contribute to the noise level.

(i) Shot noise

If there is no correlation between charge carriers while in transit from one electrode to the other, then for N' charge carriers ΔW is given by

$$\Delta W = w\left(\frac{N'}{2}\right)^{\frac{1}{2}} \left(\frac{\tau}{\tau_c}\right)^{\frac{1}{2}} \qquad (3.11)$$

where the charge collection time $\tau_c < \tau$ (= CR).

In order to obtain an estimate for ΔW generation-recombination noise must also be considered.

(ii) Generation-recombination noise

In fact the carriers in a counter may undergo trapping or

recombination before they are collected at the electrodes or carriers may be thermally generated at some point in the counter and so these shorter current pulses contribute to the noise. If the mean free time of the carriers is τ' then

$$\Delta W = w\left(\frac{N'}{2}\right)^{\frac{1}{2}}\left(\frac{\tau\tau'}{\tau_c^2}\right)^{\frac{1}{2}} \qquad (3.12)$$

Both shot noise and generation-recombination noise are to an extent mutually exclusive and for a 5 MeV alpha particle incident upon a silicon counter the maximum energy resolution either source could give is

$$\Delta W = 3.0 \text{ keV.}$$

(iii) Excess noise

Excess noise in semiconductors has been dealt with fully by van der Ziel[5]. It comprises all current noise which is greater than that due to shot noise or generation-recombination noise. So far as surface barrier detectors are concerned both surface treatments of the silicon and the nature of the 'ohmic' back contact will contribute to this source. A complete formulation is not possible.

3.4 Reverse current mechanisms

3.4.1 Electron emission

3.4.1.1 Principle of rectification

In Fig. 3.2(a) electrons in the metal are in dynamic equilibrium with those in the semiconductor. The transition rates of electrons from metal to semiconductor and from semiconductor to metal are

equal. If the semiconductor is made positive with respect to the metal (Fig. 3.2(b)) the probability of a transition from the metal is still proportional to $\exp(-\phi_{MS}/kT)$ but the probability of a transition from the semiconductor conduction band into the metal, which is proportional to $\exp(-e(V_D + V_A)/kT)$ is reduced, i.e. there is a net electron flow from the metal to the semiconductor. When the metal is made positive with respect to the semiconductor (Fig. 3.2(c)) then the reverse is true and the probability of electron transfer from the semiconductor into the metal is greatly increased. This is the electron transfer mechanism envisaged in both Diode theory and Diffusion theory.

3.4.1.2 Diffusion equation

It has already been pointed out that the barrier thickness is large compared with the mean free path of a charge carrier for metal-semiconductor contacts when $N_D < 10^{14}$ carriers cm^{-3} (section 2.2.4). Consequently the charge carrier experiences numerous collisions within the barrier. Moreover, if the mobility of the carrier remains field independent and both image force lowering of the barrier and tunnelling are neglected then the current density for a Schottky barrier in reverse bias is given by(6)

$$j_D = \frac{1}{\rho}\left[(V_D + V_A)\frac{2N_D e}{\epsilon\epsilon_o}\right]^{\frac{1}{2}} \exp\left(\frac{-eV_D}{kT}\right)\left[1 - \exp\left(\frac{-eV_A}{kT}\right)\right] \qquad (3.13)$$

provided $eV_D \gg kT$.

It is obvious that a saturation current will not be observed, the reverse current being voltage dependent. For a detector of

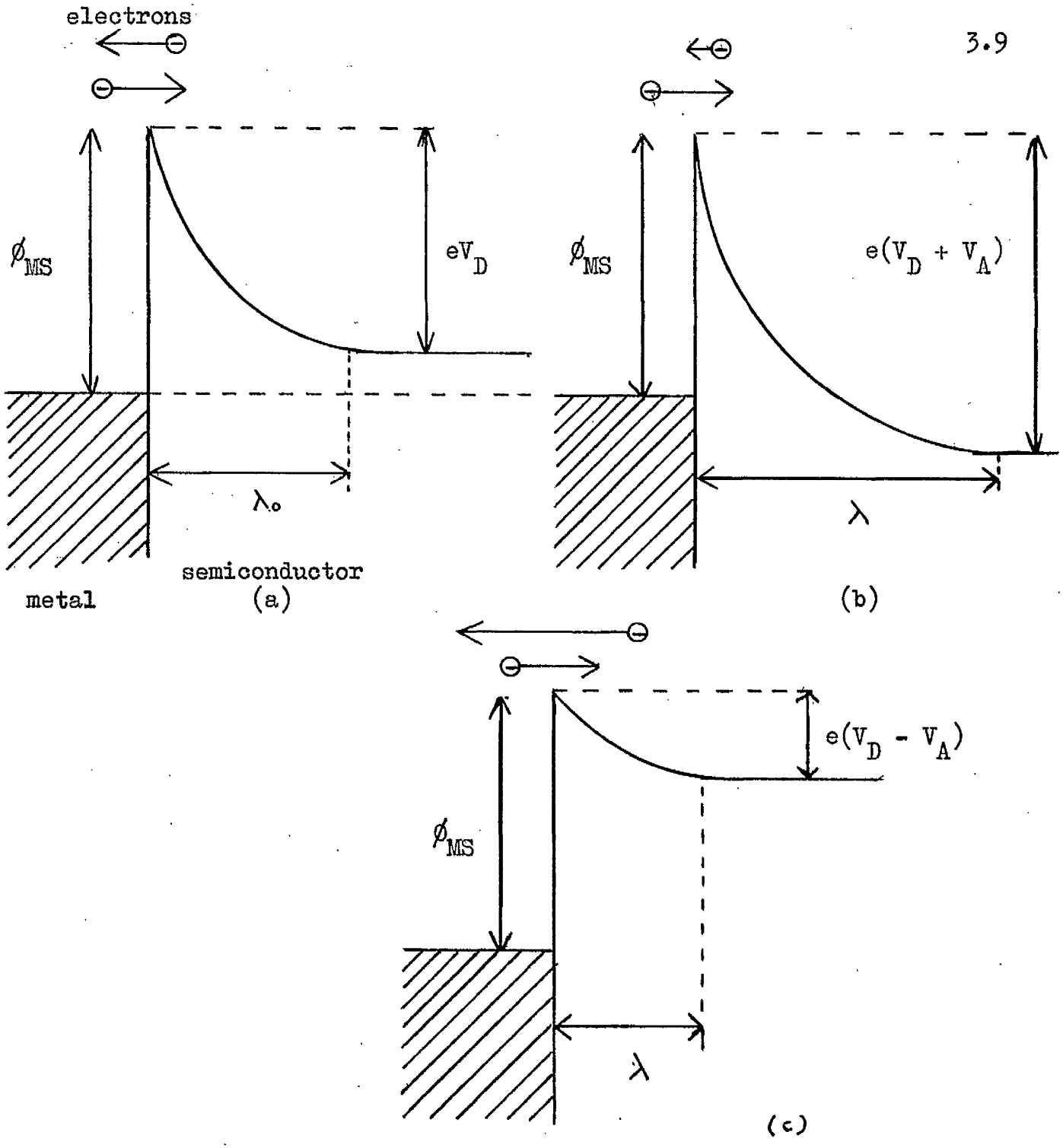


Fig. 3.2. Principle of rectification

(a) Equilibrium condition.
(b) Reverse voltage applied.
(c) Forward voltage applied.

4,000Ω cm n-type silicon at 300°K with a gold-silicon barrier for which ϕ_{MS} = 0.80 eV this reduces to:

$$j_D = 3.8 \times 10^{-8} \, (0.38 + V_A)^{\frac{1}{2}} \left[1 - \exp\left(\frac{-eV_A}{kT}\right)\right] \quad A \, cm^{-2} \qquad (3.14)$$

when V_A is expressed in volts.

This expression is plotted in Fig. 3.3 for $0 > V_A > -100$ volts. If ϕ_{MS} = 0.75 eV the constant becomes 2.8×10^{-7} and the reverse current increases by almost an order of magnitude (Fig. 3.3). Similarly if ϕ_{MS} = 0.85 eV the constant becomes 4.9×10^{-9} and the current decreases by more than ten times (Fig. 3.3). Again if the temperature is decreased or increased by 18°K then j_D would change by the same amounts as above.

In some cases reverse currents less than 1μA cm^{-2} are observed for surface barrier detectors, but in general the observed currents are slightly larger.

3.4.1.3 Diode equation

The diffusion theory is not really valid for junctions under high reverse bias when the drift velocity of the carriers within the barrier exceeds the thermal velocities for the particular temperature. Solution of the diffusion equation under these conditions yields a solution almost identical to the diode equation[6] which predicts a saturation current in the reverse direction, j_S, given by

$$j_S = eN_D \left(\frac{kT}{2\pi m^*}\right)^{\frac{1}{2}} \exp\left(\frac{-eV_D}{kT}\right) \qquad (3.15)$$

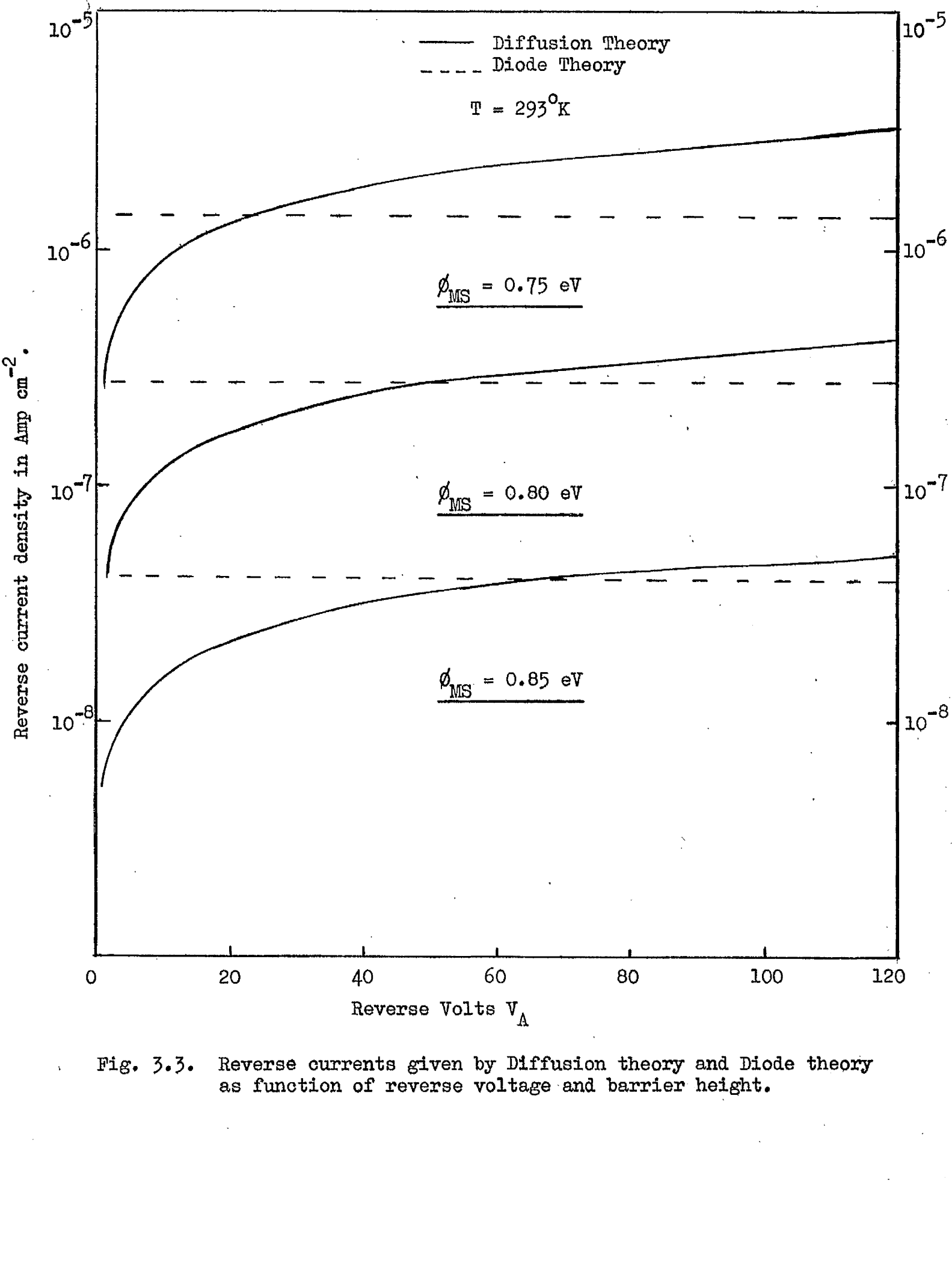


Fig. 3.3. Reverse currents given by Diffusion theory and Diode theory as function of reverse voltage and barrier height.

or $$\dot{j}_S = A^* T^2 \exp\left(\frac{-\phi_{MS}}{kT}\right) \qquad (3.16)$$

where $$A^* = \frac{4\pi m^* e k^2}{h^3} .$$

A^* has been calculated by Crowell[7] for a variety of semiconductor tensor effective masses including the silicon [111] direction. At 300°K when $\phi_{MS} = 0.80$ eV, $\dot{j}_S \approx 3 \times 10^{-7}$ A cm^{-2}. Values of $\dot{j}_S$ are indicated on Fig. 3.3 for the barrier heights referred to in 3.4.1.2.

3.4.2 Hole diffusion current

Holes can be generated in the undepleted n-type silicon by electrons undergoing transitions into recombination centres which may exist in the forbidden energy gap. If these holes are within a diffusion length of the high field existing in the depletion layer then they may be swept across it and be collected by the metal.

The generation rate for holes G is given by

$$G\tau_r = p_n$$

where p_n is the equilibrium density of holes in the n-type silicon and τ_r is the recombination time[8].

The diffusion current is the product of the generation rate and the diffusion length L_p.

$$J_D = \frac{e p_n D_p^{\frac{1}{2}}}{\tau_r^{\frac{1}{2}}} \qquad \text{and} \qquad L_p = (D_p \tau_r)^{\frac{1}{2}} \qquad (3.17)$$

For n-type silicon resistivity 4,000 cm $p_n \approx 10^8$ cm^{-3} and if $\tau_r \sim 10\mu$sec then $J_D \approx 1 \times 10^{-9}$ A cm^{-2}.

Strictly, τ_r will not be the bulk lifetime but will depend on the surface recombination velocity s and so τ_r should be replaced by an effective lifetime τ_{eff} which for a thin detector of thickness d will be given by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_r} + \frac{2s}{d} \qquad (3.18)$$

This has been allowed for in the above estimate of J_D.

The above analysis is only valid for $(d - \lambda) \gg L$. The case of $(d - \lambda) < L$ has been dealt with by Gossick[9] and as the detector becomes fully depleted J_D does not remain independent of the voltage.

From the example given one can see that the contribution to the total reverse current from this source is negligible.

3.4.3 Generation current

None of the above theories take into account generation current. Sah, Noyce and Shockley[10] have shown that the maximum value of the current which arises due to the generation of hole-electron pairs via recombination centres in the space charge region is given by

$$J_g = \frac{e\lambda}{2\tau_r} \quad n_i \qquad (3.19)$$

where n_i is the intrinsic carrier concentration.

Again for a 4,000 Ω cm n-type silicon counter with $\tau_r = 100\mu$ sec. and under a 100 V reverse bias then $J_g = 2.4 \times 10^{-7}$ A cm^{-2}. From equation 3.1 it can be seen that J_g is proportional to $(\rho V)^{\frac{1}{2}}$.

3.4.4 Excess current

Generally the reverse current exceeds $1\mu A\ cm^{-2}$ (which is about the value expected from 3.14 and 3.16) and special encapsulation techniques have to be adopted in order to reduce it to an acceptable level. This may be attributed to a number of sources. First there may be an electron-hole component due to generation at the surface. If there is surface contamination which gives rise to energy levels as the surface of the crystal these may provide efficient recombination centres. An expression for this component is possible[11] but a numerical evaluation involves a knowledge of the number of states, their energy location and their capture probabilities and these factors will change with ambient gases and the particular surface contaminant. Secondly there will be large currents associated with scratches and surface channels at the edge of the barrier unless proper care has been taken during the surface preparation of the semiconductor.

3.4.5 Criteria for low reverse currents

From the foregoing one can see that the main considerations in order to achieve small reverse currents are as follows:

(i) Large value of ϕ_{MS}.

(ii) High value of carrier lifetime.

(iii) The semiconductor surface must be free from contaminants and scratches.

3.5 Reverse current noise

3.5.1 Space charge generated noise

The total number of electrons N_{ge} in the depletion layer due

to generation is given by n × volume of space charge region, where n is the number per unit volume. From equation (26)

$$J_g = \frac{e\lambda}{2\tau_r} = ne\mu_n \frac{V_A}{\lambda}$$

i.e. $$N_{ge} = \frac{n_i A \lambda^3}{2\tau_r \mu_n V_A} \qquad (3.20)$$

where A is the area of the device.

Similarly the number of holes will be N_{gh} where

$$N_{gh} = \frac{n_i A \lambda^3}{2\tau_r \mu_p V_A} \qquad (3.21)$$

Therefore the number of charge carriers in the depletion region N_c is

$$N_c = \frac{n_i A \lambda^3}{2\tau_r V_A}\left(\frac{1}{\mu_n} + \frac{1}{\mu_p}\right) \qquad (3.22)$$

The generation events are independent of each other and so the current due to these carriers will be subject to full shot noise. (Recombination noise may be neglected assuming carriers are not retrapped on account of the high field present.) Putting equation 3.22 in equation 3.11

$$\Delta W = w\left[\frac{n_i A}{4\tau_r V_A}^3 \left(\frac{1}{\mu_n} + \frac{1}{\mu_p}\right)\right]^{\frac{1}{2}} \left(\frac{\tau}{\tau_c}\right)^{\frac{1}{2}} \qquad (3.23)$$

Taking $\frac{\tau}{\tau_c}$ as unity, then for a 4,000Ω-cm n-type silicon device at

100 V reverse bias with $\tau_r = 100\mu$ sec. and area 1 cm^2

$$\Delta W = 0.59 \text{ keV}.$$

3.5.2 Electron emission noise

For a gold-silicon counter operating at room temperature the value of the reverse current due to electron emission into the semiconductor is about $1\mu A\ cm^{-2}$ (equation 3.14). An estimate of the maximum number of effective electrons in the depletion region for the same device as above at 100 V reverse bias due to this current is 8.2×10^3. These carriers will be subject to full shot noise (equation 3.11 giving a resolution

$$\Delta W = w \left(\frac{8.2 \times 10^3}{2}\right)^{\frac{1}{2}} \left(\frac{\tau}{\tau_c}\right)^{\frac{1}{2}}$$

i.e. $\Delta W = 0.23$ keV taking $\frac{\tau}{\tau_c}$ as unity.

3.5.3 Hole diffusion current noise

This contributes negligible amount of noise.

It is apparent from these considerations that excess noise will dominate and hence the ultimate resolution of surface barrier diodes is governed by the extent of the excess noise.

3.6 Detector fabrication and encapsulation techniques

3.6.1 Front contact

Some workers prefer merely to etch and encapsulate their silicon slices and then evaporate a thin layer of gold in order to

achieve a rectifying contact[12]. Other groups treat the surface after etching to ensure that an inversion layer is formed[13,14,15] and then evaporate a gold layer which makes contact to the oxide. The surface treatments have been described in Section 2.3.3. Even after these surface treatments which make the surface of the n-type silicon become p-type it is then found necessary to expose the detectors to a humid atmosphere in order to achieve an acceptable noise level.

Detectors manufactured by this technique exhibit extraordinarily low reverse currents $\simeq 10^{-8}$ A cm^{-2} and this, presumably, is because the treatments not only keep the surface conductivity low and form a high barrier, but also reduce s quite considerably, thereby reducing the generation current to a minimum.

3.6.2 Ohmic back contact

The type of back contact employed depends primarily on the device application. For thin $\frac{dE}{dx}$ counters a method is required which does not impede the energetic particle in any way. Gold evaporated onto the back face of the silicon slice which is coarsely lapped[16] and electroless nickel plating deposited onto a similar surface[17] have both been used successfully. Unfortunately these methods introduce many recombination levels and consequently the contacts inject carriers when operated fully depleted. A similar drawback is experienced with counters manufactured by evaporating gold on both sides.

Andrews[18] was the first to point out the advantages of evaporating aluminium on etched n-type silicon surfaces to form an

ohmic back contact and this method has been used successfully for a number of years. Unfortunately these contacts tend to rectify after a time and so the resolution does not remain constant[19]. Moreover, good rectifying characteristics have also been claimed for evaporated aluminium on n-type silicon[20].

Alloying and diffusion methods were rejected because of the degradation in carrier lifetime with the introduction of unwanted impurities due to the heating processes involved. Walter and Bates[21] have shown this to be the case even after a thermal cycle to only 500°C in clean conditions. However, recently Owen[12] has succeeded in producing non-injecting stable back contacts by a phosphorus diffusion to give a thin N^+ region. Contact to this is made by an evaporated metal film.

3.6.3 Encapsulation

Nearly all surface barrier diodes are encapsulated using an epoxy resin technique introduced by Fox and Borkowski[16]. They observed microplasmas at the edge of the junction when breakdown occurred under high reverse bias. Using a combination of an amine-free epoxy resin doped with iodine (to ensure a p-type inversion of the silicon) and an amine type epoxy resin (which kept the surface strongly n-type) they removed the edge of the gold film from the electric field of the junction. At the present time an edge protection technique utilising the amine-free epoxy resin alone is used in order to reduce surface leakage and is found to give satisfactory results[12].

3.6.4 Guard rings

Guard ring techniques are sometimes employed[22,16] in order to reduce surface leakage and hence noise. They are generally only used after processes have been employed in the device manufacture which encourage large surface currents.

3.7 Formation of the rectifying contact

In 1964 Gibbons[23] reported that the reverse current of gold-n-type silicon contacts decreased by more than three orders of magnitude when oxygen was admitted to the vacuum system; subsequent re-pumping to 10^{-4} mm. Hg indicated that the process was irreversible. It was suggested that this could be due to the oxygen atoms on the silicon surface being desorbed by the impinging gold atoms during the evaporation process and that the oxygen atoms then diffused through the gold layer when air was admitted to the system.

Siffert, Laustriat and Coche[20,24] observed similar phenomena and have investigated the degree of rectification of twenty metals evaporated on silicon as a function of time. They conclude that the rectification is due to the migration of oxygen through the metal film and oxide layer, the rate at which this proceeds depending entirely on the work function of the metal.

Recently, Walter and Boshart[25] prepared silicon wafers as in 2.3.3 and left them for one month before evaporating the gold layer. They found that in the case of the silicon slices which were only etched, V_D was zero while in the vacuum chamber (capacity plots

were used to determine V_D) but that a barrier formed upon exposure to oxygen.

Turner[2] has measured V_D in vacuum for the gold-silicon system and found that the barrier existed immediately after the evaporation process. He claims that subsequent admittance of oxygen has very little effect. Moreover he found the properties of the gold-silicon contact to be independent of the gold thickness - this is in complete disagreement with Siffert et al..

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Chapter 4

General Experimental Apparatus and Specimen Preparation Techniques

4.1 Vacuum deposition equipment

Two evaporation systems have been utilised for the deposition of the aluminium and gold films. They are described separately.

(i) A modified Edwards high vacuum coating unit model 6.E.2.

This system had a 6" diameter bell jar which could be replaced by a 6" diameter glass cylinder with L gasket seals and a metal top plate. Fixed to this metal plate was a multiple substrate carriage with facilities for moveable masks and shutters. There was also provision for extra electrical leads into the system. A liquid nitrogen cold trap was designed and fitted to the unit and an extension range added to the Penning gauge. This system attained an ultimate pressure of 1×10^{-5} torr. A Mullard ionisation gauge was used to calibrate the Penning gauge. All of the aluminium films were deposited in this system.

(ii) An Edwards high vacuum coating unit model 12.E.3.

This had a 12" diameter bell jar which could also be replaced by a 12" diameter glass cylinder. The same specimen mounting jig, etc. used in (i) could easily be fitted to this system as shown in Fig. 4.1. This unit had an Edwards NT4 liquid nitrogen trap added for most of the work. An operating pressure of 4×10^{-6} torr was attained in approximately one hour. The pressure was recorded on an A.E.I. VC.10. ionisation

gauge control unit utilising a 29D15 head, because the Penning gauge was found to be erratic and unreliable. All the gold films were deposited in this system. The detectors were also made using this unit.

Gold was evaporated from resistance heated molybdenum boats and aluminium from suitably prepared tungsten spirals (Section 5.2).

4.2 Film thickness and rate control

An Edwards Thin Film Monitor, model 1, was used to control the rate of film deposition and film thickness. The 6 Mc/s quartz crystal, which oscillates in shear mode, was situated alongside the specimens in the evaporating vapour stream (Fig. 4.1). An aperture (0.25" diameter) to the crystal just larger than the active area of the oscillating crystal was found necessary, otherwise reproducible results were not obtained. This is because the crystal varies in sensitivity over its active area[1]. The monitor output was fed to a Beckman potentiometric recorder. Crystals were calibrated for both aluminium and gold by a multiple beam interferometric technique, based on Tolansky white light fringes of equal chromatic order[2,3].

The basic experimental arrangement is shown in Fig. 4.2(a) and Fig. 4.2(b) is an enlarged view of the interference plates. Dark line fringes with steps are observed in the spectrometer, Fig. 4.2(c) and the thickness of the film Δt is given by

$$\Delta t = \left[\frac{\lambda_2}{\lambda_2 - \lambda_1}\right] \frac{\Delta\lambda_1}{2}$$

These parameters are indicated in Fig. 4.2.

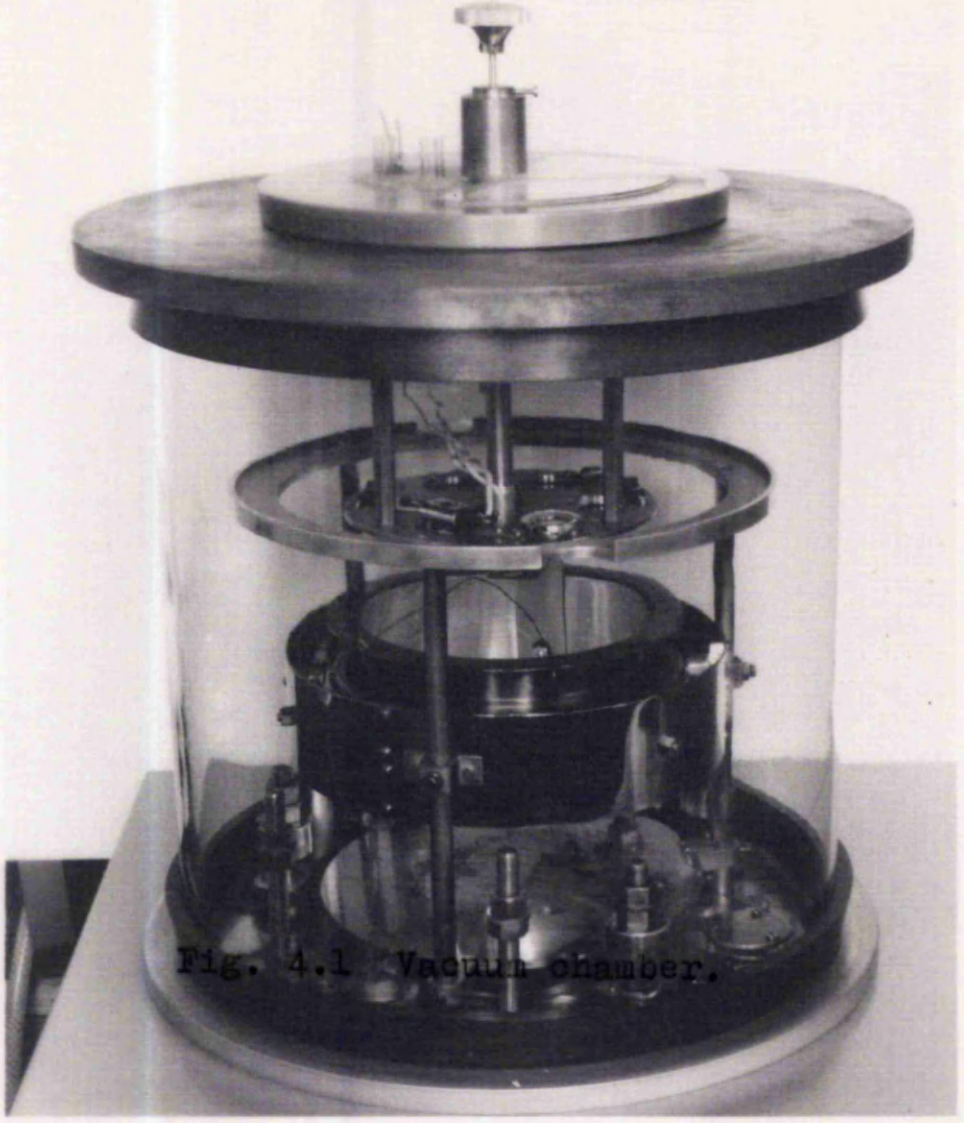
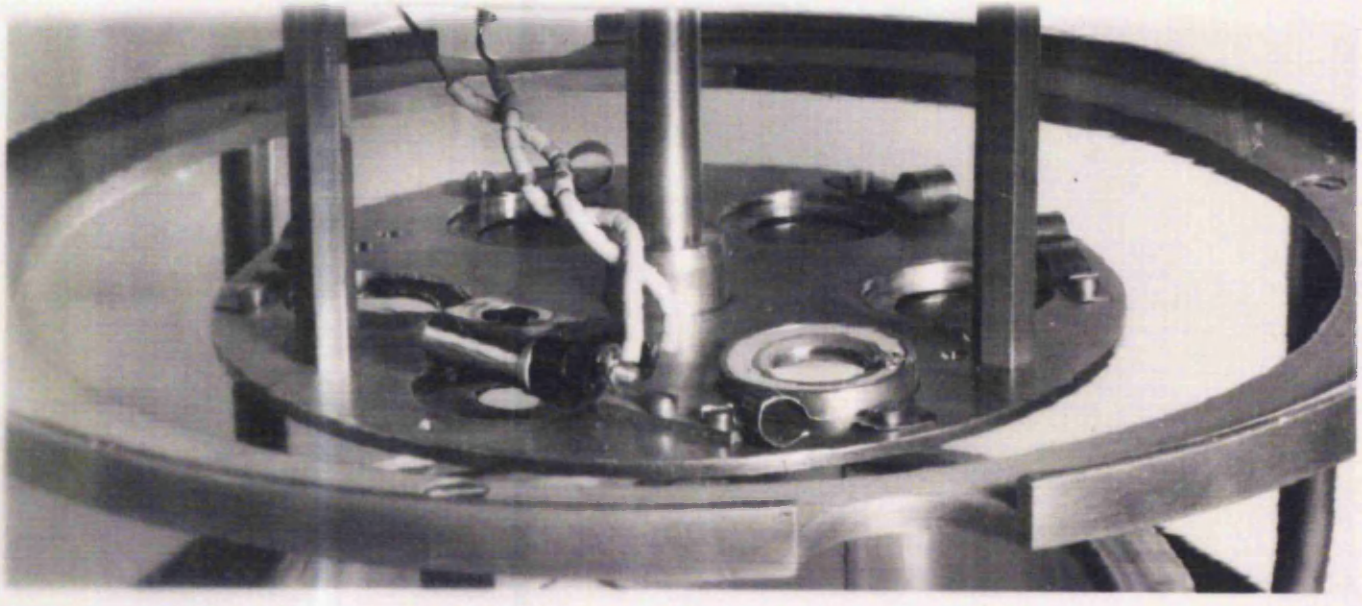


Fig. 4.1 Vacuum chamber.



4.3 Current-voltage testing apparatus

Current-voltage characteristics were measured to 2% accuracy using the circuit in Fig. 4.3. The voltage across the specimens was measured on a Keithley Electrometer 610 A. and the current through the devices was determined by measuring the voltage developed across a series of 1% resistors using a Keithley Microvolt-Ammeter, model 150 A. The voltage across the resistors was less than 10 mV at full scale deflection for all current ranges considered. The 10 volt. f.s.d. outputs from the Keithleys were fed to the X and Y inputs of a Moseley "Autograf" recorder and the I - V characteristics plotted automatically by varying the output of the D.C. supply. Using a suitably designed variable voltage supply in conjunction with variable resistances, bias voltages in the range 0.01 v/inch - 10 v/inch and currents from 10^{-3} A/inch - 10^{-8} A/inch could be conveniently recorded.

4.4 Specimen preparation

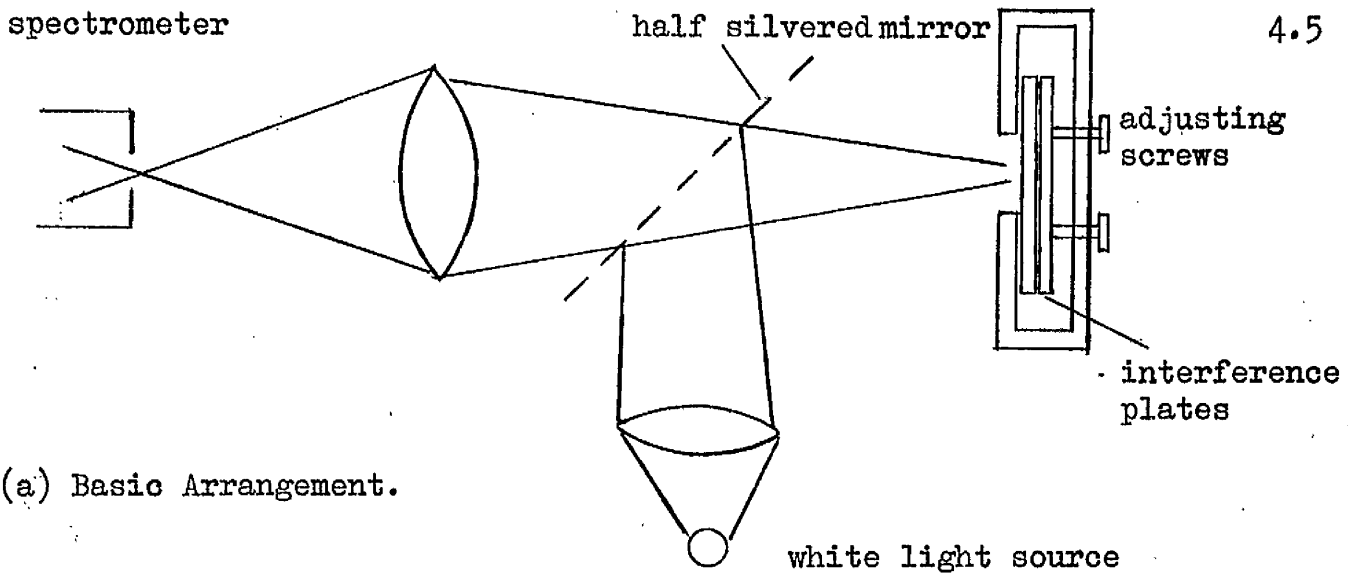
The basic specimen preparation of the silicon slices prior to the evaporation process involved:-

(i) The formation of an ohmic contact to the slice.

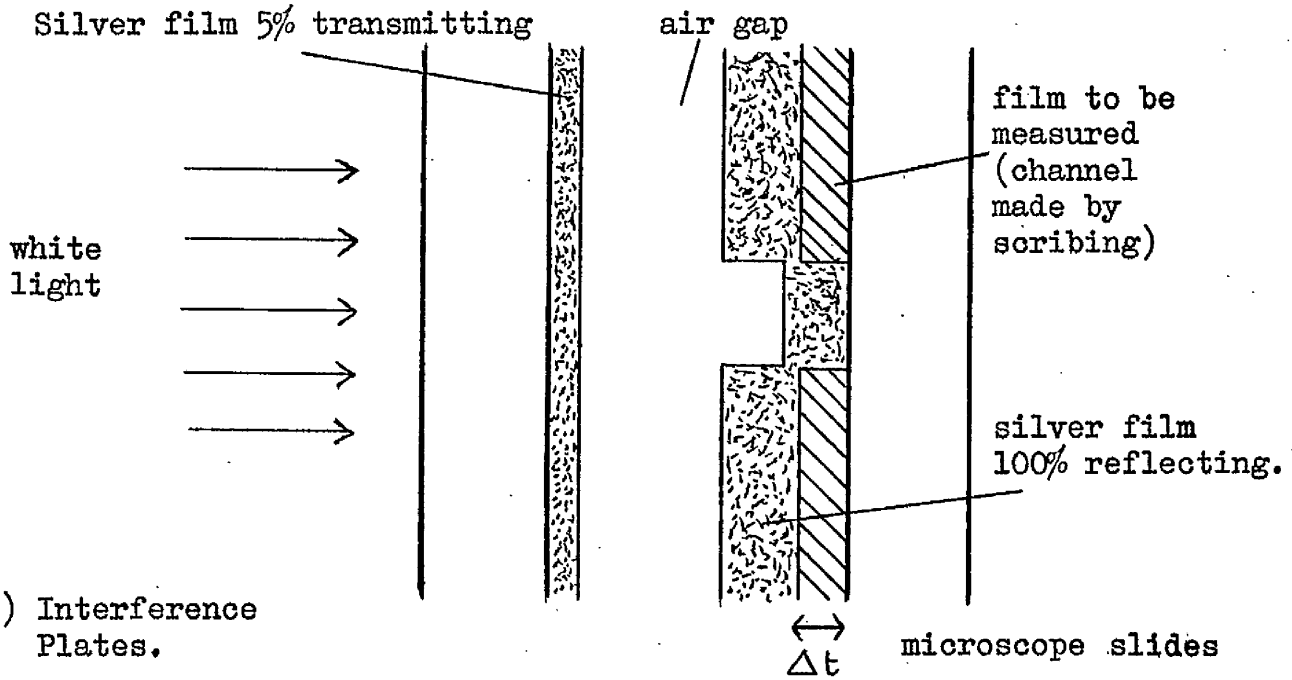
(ii) Suitably preparing the reverse face of the slice for the particular experiment envisaged.

4.4.1 Formation of the ohmic contact

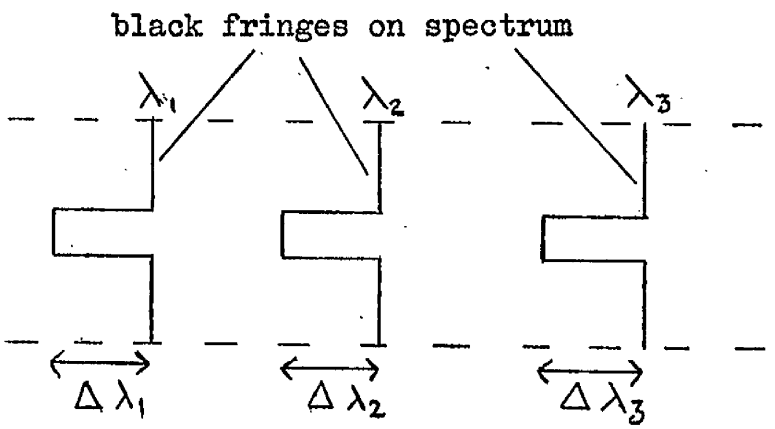
The appropriate resistivity silicon (depending on the application) was cut into slices with the faces perpendicular to the [111] direction by means of a diamond impregnated wheel (n-type silicon has



(a) Basic Arrangement.



(b) Interference Plates.



(c) Appearance in Spectrometer

Fig. 4.2. Optical Measurement of Film Thickness.

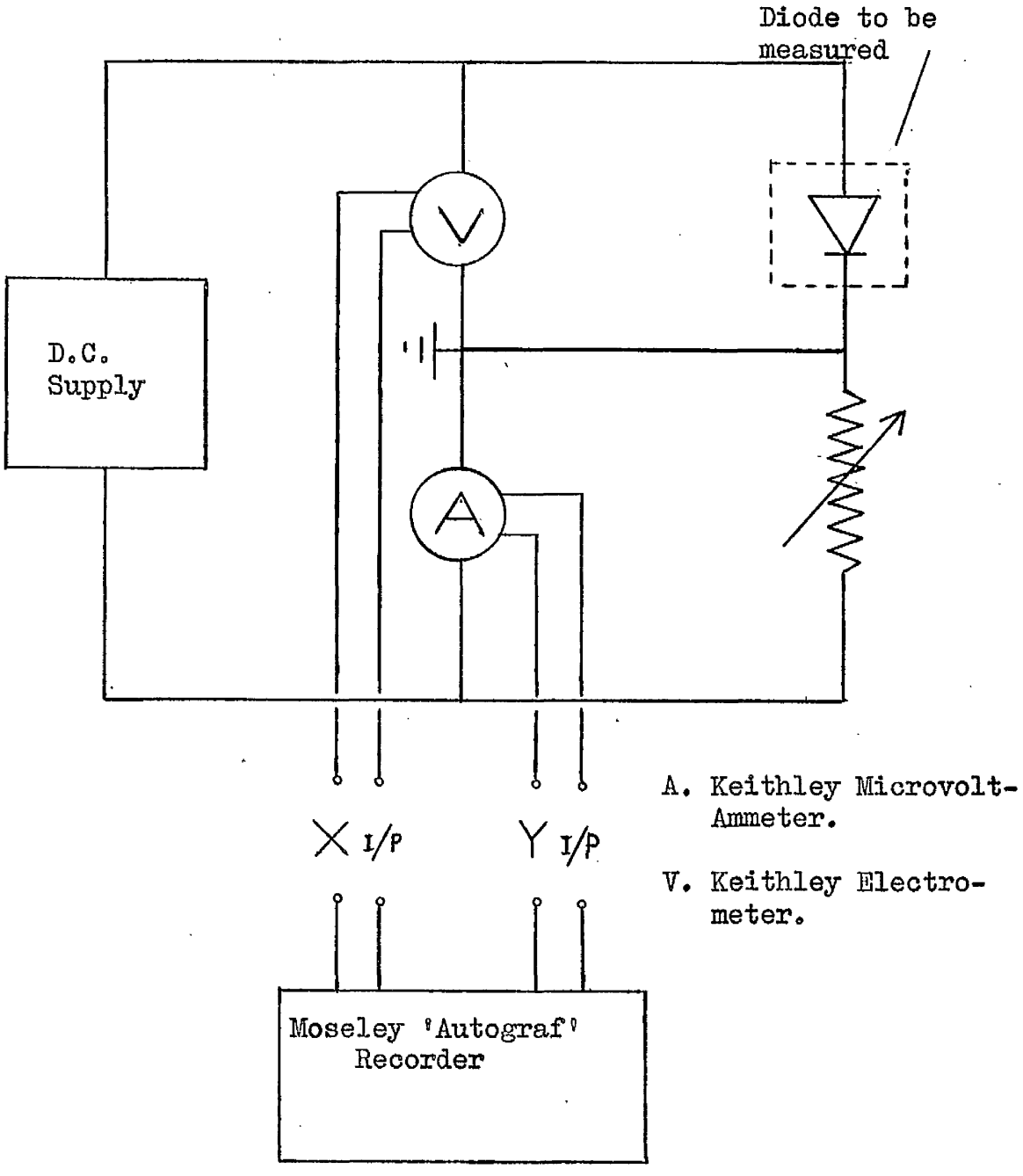


Fig. 4.3. Current-Voltage Measuring Circuit.

been used exclusively). The cutting damage was then removed by lapping on glass plates with silicon carbide powders starting with 240 grade and finishing with 600 mesh. A one minute etch in White etch[4], HF/HNO_3 in proportions 1/3, removed the remaining surface damage before evaporating a layer of gold/antimony (1%) alloy on one surface which was then alloyed in situ at about 500°C for a few minutes. This formed a good ohmic contact to the n-type silicon. (Electrical contact to this alloyed region was made at a later stage.) The ohmic contact was then covered in black wax to protect the alloyed region from attack in the subsequent front surface preparation.

4.4.2 Chemical etching of the front surface

After the alloying process it is necessary to ensure that the front surface of the wafer is clean, highly polished and free from all surface damage and contamination. Archer[5] has shown that the strong affinity for oxygen of the free valence bonds at the silicon surface causes a layer of silica about 10 Å thick to grow after etching. The fact that this initial oxide layer is not thicker, as has often been postulated, has been confirmed by Holmes and Newman[6] using medium-energy electron diffraction techniques. Irving[7] has reviewed the chemistry and kinetics of the chemical etching of semiconductors and we may regard the process as one in which the surface atoms are being continuously oxidised by one of the etch constituents, the other constituent dissolving away this surface oxide. In the case of silicon, HF/HNO_3 mixtures are commonly used. Here the HNO_3 oxidises the silicon and the HF dissolves the oxide.

The etching of silicon in HF/HNO_3 solutions has been extensively investigated by Klein and D'Stefan[8] who pointed out the various factors which influence the resulting surface. In order to obtain reproducible silicon surfaces suitable for the experiments it was found necessary to use these etchants. Particular attention was paid to the following; surface preparation of the slices prior to etching, etch composition and purity of the constituents, etch temperature, agitation of the slices in the etchant. The detailed process was as follows:-

(a) Surface lapped using alumina powders finishing with B.A. 304 on selvyt cloth. - Specimen had dull polished appearance.

(b) Wafer ultrasonically shaken in (i) carbon tetrachloride, (ii) acetone, (iii) methanol, (iv) demineralised water.

(c) Wafer etched in appropriate HF/HNO_3 solution.*

(d) Wash in acetone - to remove black wax protecting the alloyed region.

(e) Several ultrasonic washes in carbon tetrachloride.

(f) Two ultrasonic washes in acetone.

(g) Two ultrasonic washes in anhydrous methanol.

The slices were finally blown dry in a nitrogen ambient before transferring immediately to the evaporator. Transistor chemicals were always used in the above processes. During (c) the wafer was held in polythene tweezers and agitated in a random manner for seven minutes - automatic methods were not sufficiently random and etch flow patterns remained afterwards. Quantities of etch were used which ensured no

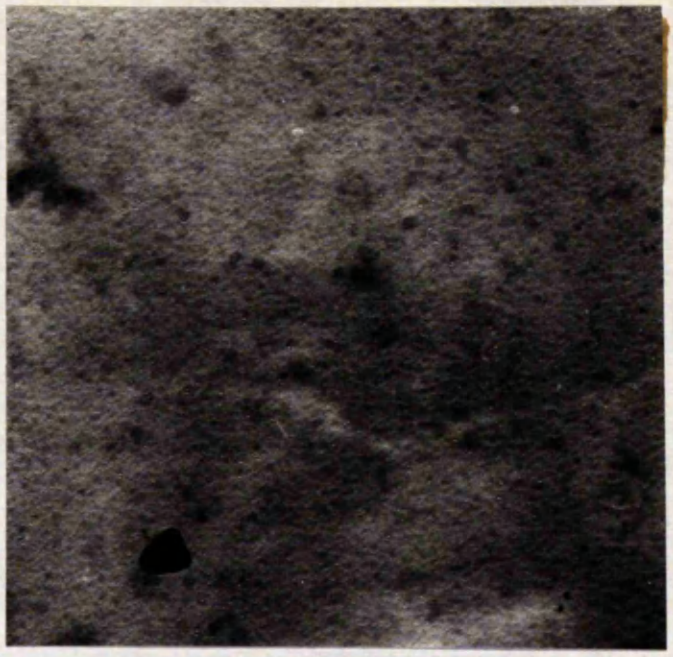
* The HF/HNO_3 ratios are quoted in the relevant sections.

appreciable temperature rise of the solutions. The etch was quenched by flooding with demineralised water (resistivity $> 10^7 \Omega$ cm) and the slice was ultrasonically agitated in liberal quantities of freshly demineralised water in a clean polythene beaker. [Holmes[4] has pointed out the need for flooding the etch as opposed to transferring the wafer to the demineralised water .]

4.5 Surface topography

The topography of the etched silicon slices prepared by the above methods was investigated. On a macroscopic scale the surfaces, although undulating, rarely resembled the peel of an orange and inspection with our optical microscope using oblique illumination revealed little detail. Accordingly attention was paid to electron microscope replication techniques.

Replicas formed by shadowing carbon-platinum (resolution about 30 Å) revealed no major surface imperfections at high magnification for any of the etched surfaces employed in later experiments. This is the most sensitive technique available, the resolution being governed by the background structure caused by the contaminating hydrocarbons in the vacuum system [9]. (The coating unit employed for the replication processes was an A.E.I. model with no liquid nitrogen trap.) A replicated surface, prepared as in section 4.4.2 using CP4A etch, is shown in Fig. 4.4. The shadowing angle was 45° and it is evident that the surface is relatively smooth and homogeneous.



shadowing angle 45°

Fig.4.4 Carbon-platinum replica of etched silicon surface.

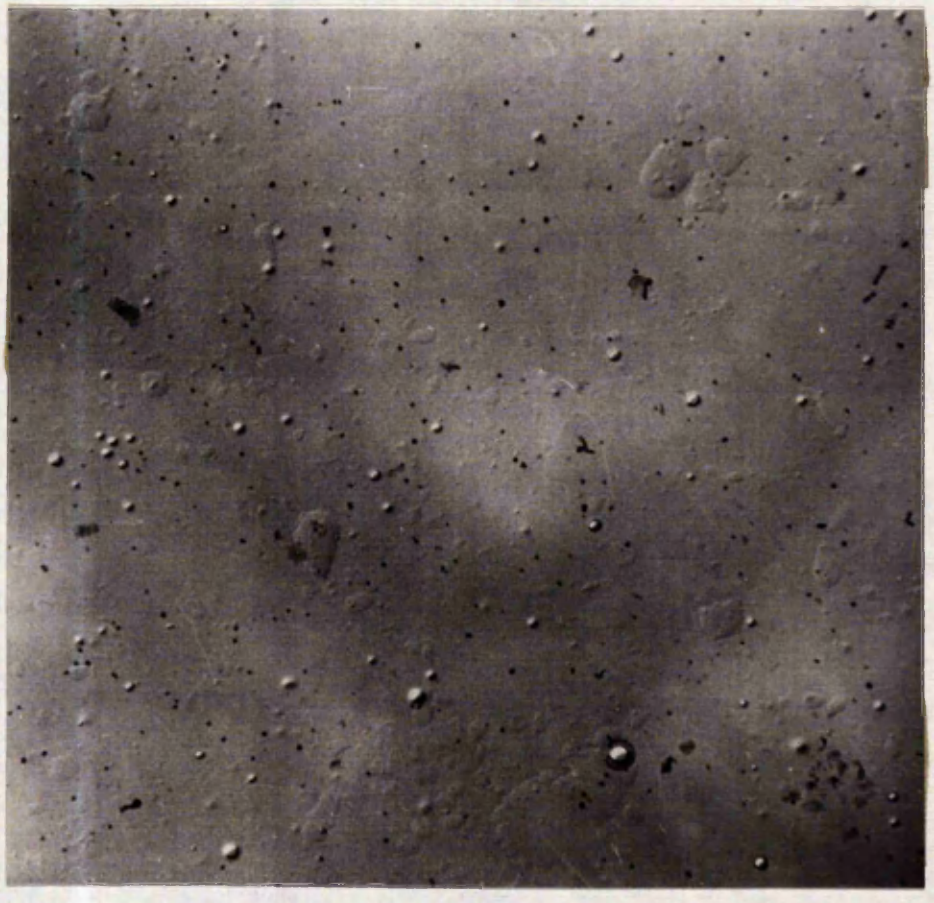


Fig.4.5 Two stage carbon/formvar replica of etched silicon surface pre-shadowed at 45° with gold-palladium.

At lower magnification a two stage carbon-formvar replication technique was adopted. The replicas were pre-shadowed with gold-palladium at 45°. A silicon surface replicated using this method is shown in Fig. 4.5. From the micrograph one can see that small protrusions 0.1 - 0.3 μ high are scattered over the surface and that rather abrupt plateaus about 400 Å high are present. The largest plateaux are about 1 - 2 μ in diameter and it is not clear how these can arise during the etching process. I believe these plateaus to be genuine features and not artefacts and they could well be stains on the surface following the quenching of the etch. Silicon hydride stains which can be present following etching in HF/HNO_3 mixtures are about this thick (300 Å)[10].

Recently Rawlins and Broselard[11] have replicated similarly etched silicon surfaces while investigating epitaxial silicon nucleation and confirm that the surface is smooth on a microscopic scale but that undulations of about 2 - 20 μ variation may occur in peak-valley height across the silicon slice.

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Chapter 5

Evaluation of Aluminium as an Ohmic Contact

The electrical properties of evaporated aluminium contacts on n-type silicon (in the resistivity range 0.5 - 10^3 Ω cm) were studied over a period of one year. Standard surface preparations and evaporation conditions were used.

5.1 Surface preparations

Slices of silicon were prepared with alloyed back contacts as described in 4.4.1. The top surfaces of the slices were then subjected to one of the following treatments.

A. Polishing to 0.25 μ diamond finish - degreased - 30 sec. etch in HF/HNO_3 (ratio 1 : 6).

B. As in 4.4.2. using CP4A etch[1] - surface then anodically oxidised* - oxide later dissolved in HF.

C. As in 4.4.2. using CP4A etch - etch time seven minutes.

D. As in 4.4.2. using HF/HNO_3 etch (ratio 1 : 6) - etch time seven minutes.

E. Same as D - surface then repeatedly oxidised in boiling HNO_3 and oxide removed in HF.+

These treatments are summarised in Table 5.1.

* The surface was anodically oxidised in a solution of boric acid and sodium tetraborate using a technique developed by K. V. Anand (2) in our Laboratory. The oxide layer was about 0.3 μ thick.

+ The oxide growth by this process is about 40 Å and the process was repeated about 15 times. Care was taken to wash (in deionised water) and dry the sample after each step, otherwise staining resulted. Beck (3) has reported that this process gives reproducible surfaces.

The samples were stored under methanol until about one minute before entry into the vacuum chamber. A batch, comprising one sample of each of the surface preparations A - E, had aluminium evaporated simultaneously to ensure identical evaporation conditions. This was repeated for various silicon resistivities.

The surface preparation A was chosen because if a metal is deposited (by electroplating or by evaporation) on such a semiconductor surface then it is known that an ohmic contact results. Thus, a contact prepared in such a manner served as a standard with which to compare the others.

5.2 Evaporation of aluminium

It is well known that aluminium is easy to evaporate at pressures below 10^{-3} torr and that it alloys freely with refractory metals and reacts with carbon and oxide crucibles. As a result of this the aluminium does not evaporate at a constant rate but the rate fluctuates as the aluminium flows from the molten globule to the hottest part of the filament. The fluctuation in rate of evaporation was easily demonstrated using the Thin Film Monitor. For reproducible experiments it was necessary to deposit the aluminium at a constant rate and uniformly over a large surface area. This was achieved as follows. A multi-strand tungsten filament was loaded with 99.99% pure aluminium wire (Johnson, Matthey & Co.) and was heated in the vacuum system at a high temperature until the whole of the filament was uniformly wet by a layer of molten aluminium. In subsequent use an aluminium source

Method Reference.	Details
A	Diamond polish - 30 sec. etch.
B	Normal lapping - CP4A etch - anodic oxid$\frac{n}{}$.
C	Normal lapping (4.4.2) - CP4A etch.
D	Normal lapping (4.4.2) - HF/HNO_3 etch.
E	Same as D. - Thin oxide growth/removal procedure.

Table 5.1. Summary of Surface Preparations.

prepared by this technique was at a constant temperature throughout its whole length and vaporised uniformly. Accordingly, the evaporation rate was easy to control.

The aluminium was deposited on the silicon at a rate of 5 Å/sec and to a thickness of 600 Å through cleaved mica masks. These masks allowed a rectangular area (1.5 x 0.35 cm) and eight dots (0.20 cm diameter) of aluminium to be formed on the silicon slices. In the case of surface preparation B, the slices were only large enough for five dots to be evaporated.

5.3 Measurements

After the aluminium deposition, contact was made to the alloyed region of the silicon by spreading air drying silver paint (Johnson, Matthey FSP. 51) over the area and pressing a disc of gold plated nickel on top. Contact was then easily made via the metal disc. The devices were stored inside a dessicator in a dark cupboard between measurements.

Current-voltage characteristics were plotted immediately after fabrication of the devices and at various time intervals. These electrical measurements were made in the dark to avoid photovoltaic effects and contact to the aluminium was made by lowering a gold probe on each area in turn. On the first day the pressure of the probe had no effect on the readings but after a few days a slightly different set of results would be obtained if the probe was re-lowered at a different pressure. This was almost certainly due to the surface of the aluminium oxidising and the probe piercing this oxide. The general shape of the characteristic

was not affected and after a period of about one month the effect of pressure was negligible - presumably the oxide layer had then grown sufficiently to become durable. According to Hass[4] the aluminium oxide grows rapidly to a thickness of 15 - 20 Å immediately upon exposure of the film to the atmosphere and that it reaches a limiting thickness of about 45 Å over one month.

All plots referred to as 'forward characteristics' are those when the metal is made positive with respect to the semiconductor. One complete set of data was obtained in situ immediately after the deposition and the changes in characteristics noted when air was admitted to the system.

Some of the aluminium films were later removed and studied in an A.E.I. EM6.G. electron microscope.

5.4 Experimental results

A summary of many I/V characteristics is contained in Tables 5.2, 5.3, 5.4 and 5.5. It was clear from the I/V plots taken over a period of one year that the speed with which the aluminium-silicon contact deteriorated into a rectifying contact depended solely on its surface preparation. Methods C and D tended to produce a contact which showed signs of rectification within a day or two whereas preparations B and E produced ohmic contacts. [There has only been one exception to this rule - a specimen prepared by method D which was used in an unrelated experiment has remained perfectly stable for nine months.]

Surface Preparation	Number of ohmic areas		
	Day of Evaporation	Following Day	One Week Later
A	8	8	8
B	4/5	4/5	4/5
C	5	5	1
D	4	4	1
E	5	5	5

Table 5.2. State of evaporated aluminium on 0.5Ω cm n-type silicon as a function of time.

Surface Preparation	Number of ohmic areas			
	Day of Evaporation	Following Day	Two Weeks Later	One Year Later
A	8	8	8	8
B	5/5	5/5	3/5	2/5
C	8	0	0	0
D	0	0	0	0
E	8	7	4	0*

Table 5.3. State of evaporated aluminium on 110Ω cm n-type silicon as a function of time.

Surface Preparation	Number of ohmic areas			
	Day of Evaporation	Following Day	One Week Later	One Year Later
A	8	8	8	8
B	5/5	5/5	5/5	5/5
C	8	8	4	0
D	3	0	0	0
E	8	8	8	7

Table 5.4. State of evaporated aluminium on 930Ω cm n-type silicon as a function of time.

Surface Preparation	Number of ohmic areas.		
	Day of Evaporation	Two Days Later	One Year Later
A	8	8	0
B	5/5	5/5	5/5
C	8	1	0
D	8	8	0
E	8	8	8

Table 5.5. State of evaporated aluminium on 1,000Ω cm on n-type silicon as a function of time.

* But only slightly rectifying.

A typical deterioration of an aluminium-silicon device from an ohmic characteristic to a rectifying one is shown in Fig. 5.1. It is obvious from Tables 5.2 - 5.5 that the actual time scale involved for the transition depended on the particular area chosen, however, the ageing of the diodes was the same.

The values of the resistance obtained from the areas on surfaces A were as expected from the geometry and bulk resistivity values and changed hardly at all ($<5\%$) over a period of one year. Fig. 5.2(b). Moreover, in the case of the aluminium deposited on the surface A of the low resistivity material, no change in the resistance was observed at all over the first week where any effect of a series resistance due to oxide growth would have been most predominant. (Fig. 5.2(a)).

None of the non-rectifying areas on any of the other surface preparations gave values of resistance expected from the contact area and bulk resistivity values. The value obtained progressively increased with time (up to one year), Fig. 5.3 - even if it did not show signs of rectification. For surface preparations B - E the series resistance of devices on low resistivity silicon, after rectification, was between 60 - 100 ohm, instead of the calculated value of about 3 ohm - indicating an interfacial layer resistance of around 100 ohm. This could not be accurately measured on the high resistivity slices because their calculated values were two orders of magnitude greater.

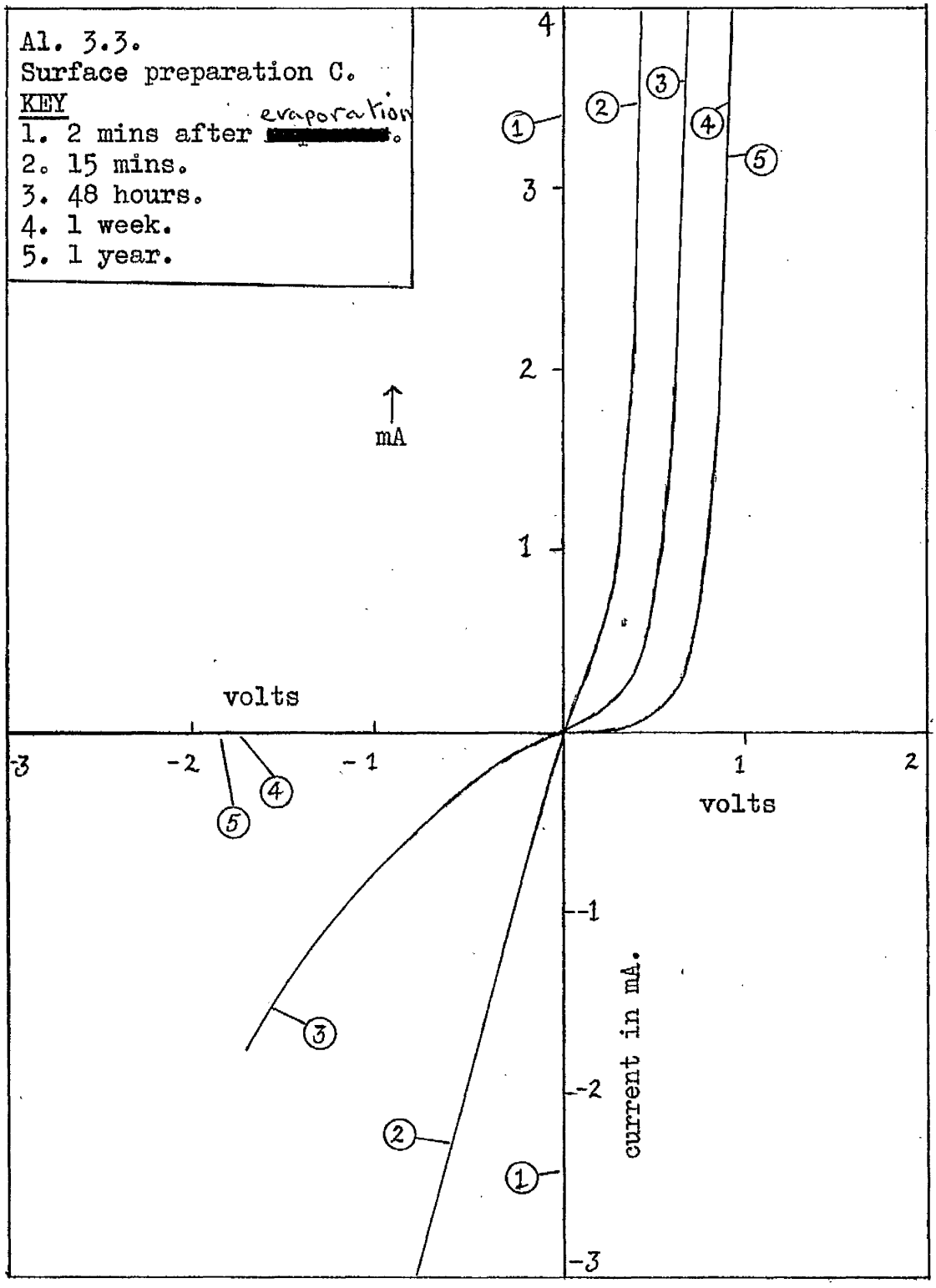
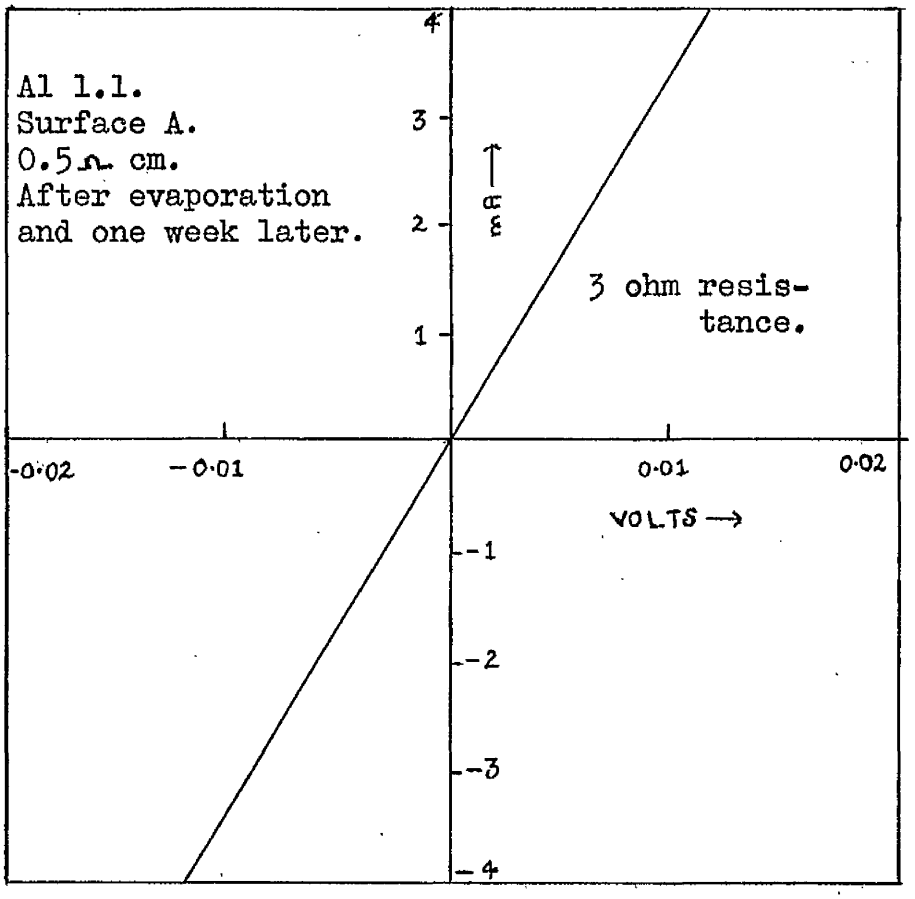


Fig. 5.1. Typical Deterioration of an Aluminium-Silicon Device from an Ohmic Characteristic to a Rectifying One.

(a)



(b)

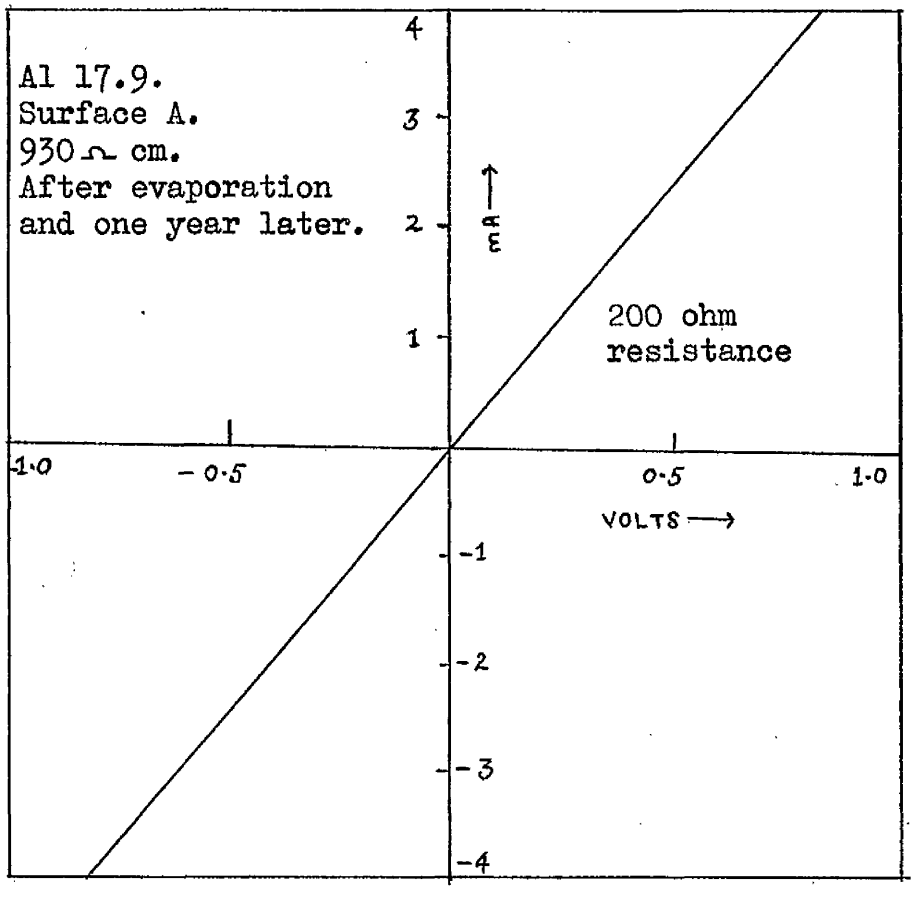
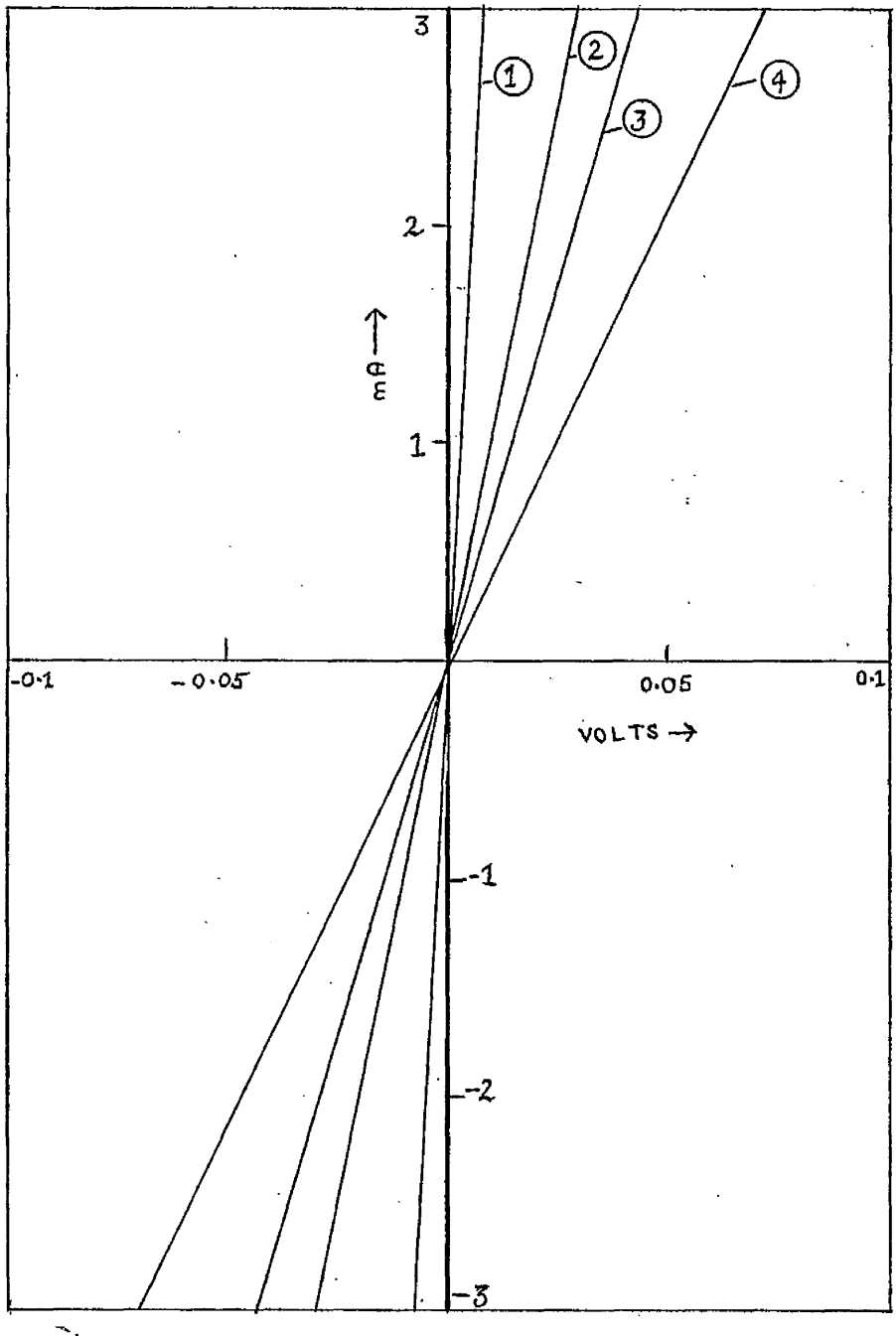


Fig. 5.2. Stable Ohmic Aluminium-Silicon Contacts.



Al 4.9. 0.5 Ω cm.
Area. 0.6 cm^2
Surface D
Calculated resistance 0.17 Ω .

KEY

(1) 1st day 3.3 Ω .
(2) One week later 10 Ω .
(3) Two weeks later 14.5 Ω .
(4) One year later 25 Ω .

Fig. 5.3. Increase in Resistance with Time of a Non-Rectifying Aluminium-Silicon Contact.

The fact that the small areas on the slices showed signs of rectification at different rates, whereas the large rectangular area merely became more resistive indicated that the aluminium contact was probably a patchy one. This was confirmed by taking a large rectangular area after a period when the characteristics of the small dots showed signs of rectification and scribing it up into smaller areas. By lowering the probe on each area it was found that some of the areas were ohmic and some were rectifying.

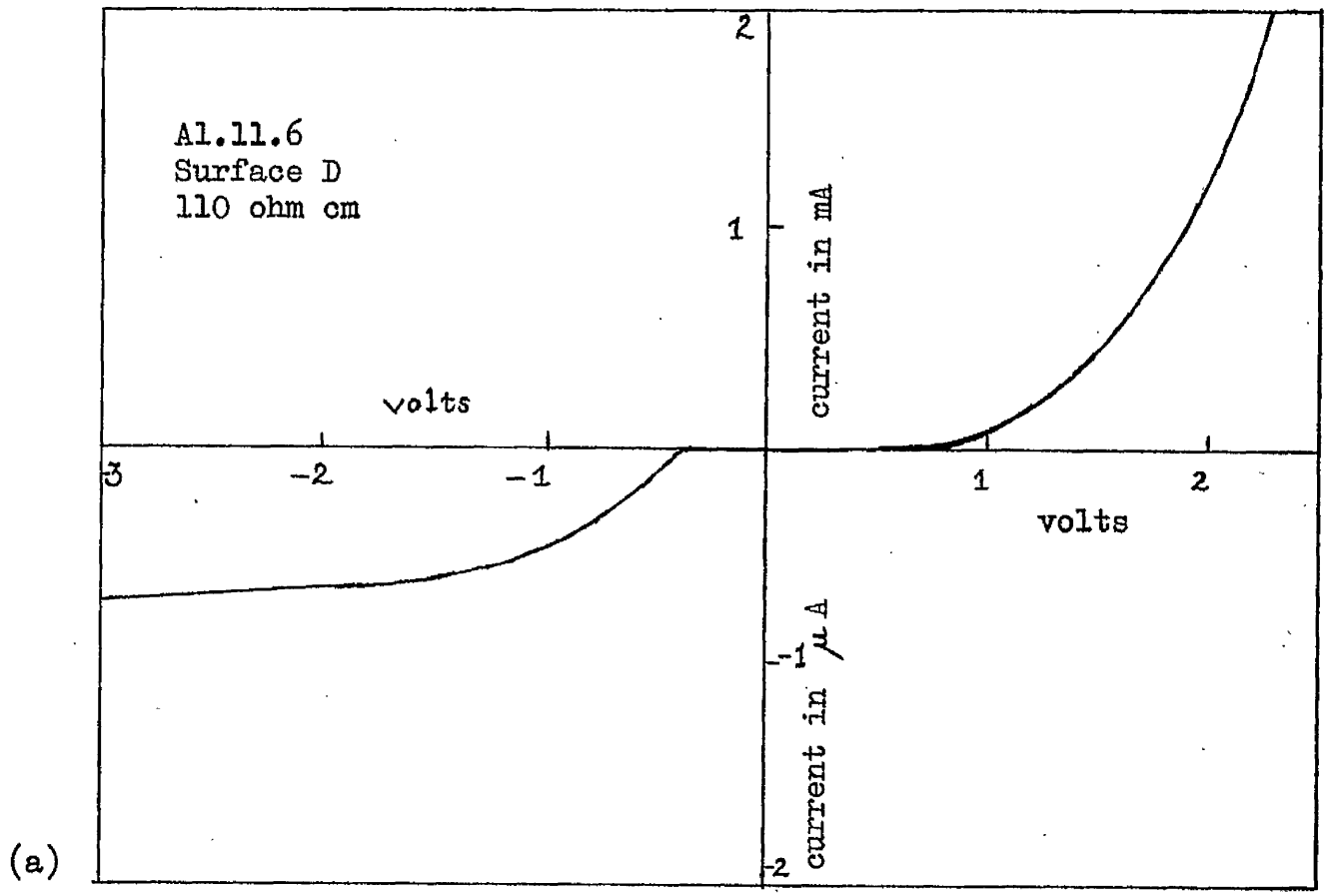
The reverse characteristics of some of the diodes were not of the conventional shape - Fig. 5.4(a) and (b). This was not confined to "aged" diodes but appeared in all stages of the rectification process from 10^{-3} - 10^{-6} A reverse current. There was no other marked difference between the characteristics of the specimens which exhibited this anomaly and the other diodes.

After one year, when the diodes formed on surfaces C and D had aged the forward characteristics of a number of diodes were investigated in more detail to see if they obeyed the simple diode equation 2.7. Two distinct types of log plots were obtained, Fig. 5.5(a) and (b). The "n" values from the linear graphs gave $2 < n < 4$.

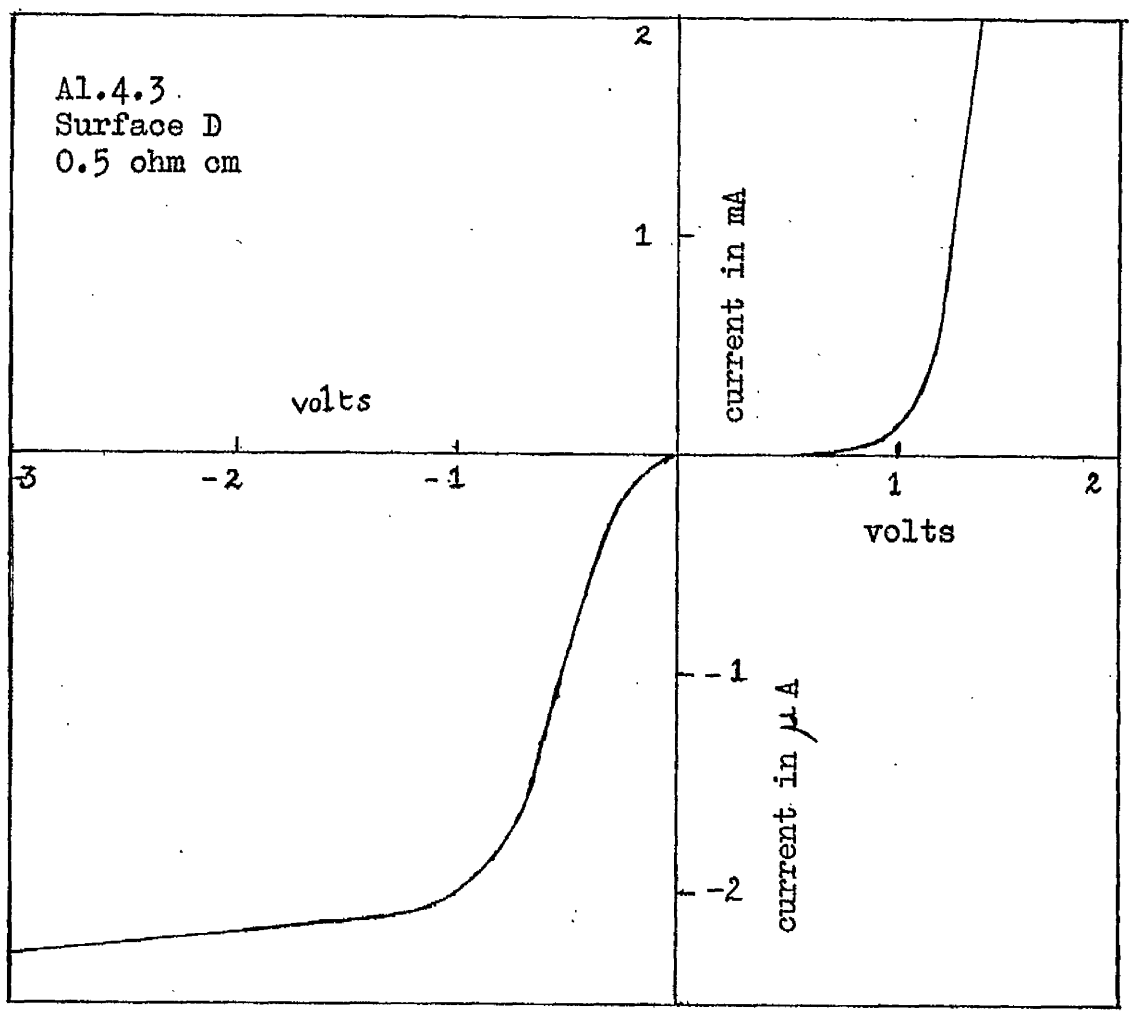
5.5 Effect of environment on characteristics

5.5.1 Experimental

Some slices of silicon were prepared using methods C and D. Before entering the vacuum system the slices were subject to the atmosphere for about one hour in order that contacts could be made to them.



(a)



(b)

Fig. 5.4(a) and (b). Illustrating the unconventional reverse characteristic.

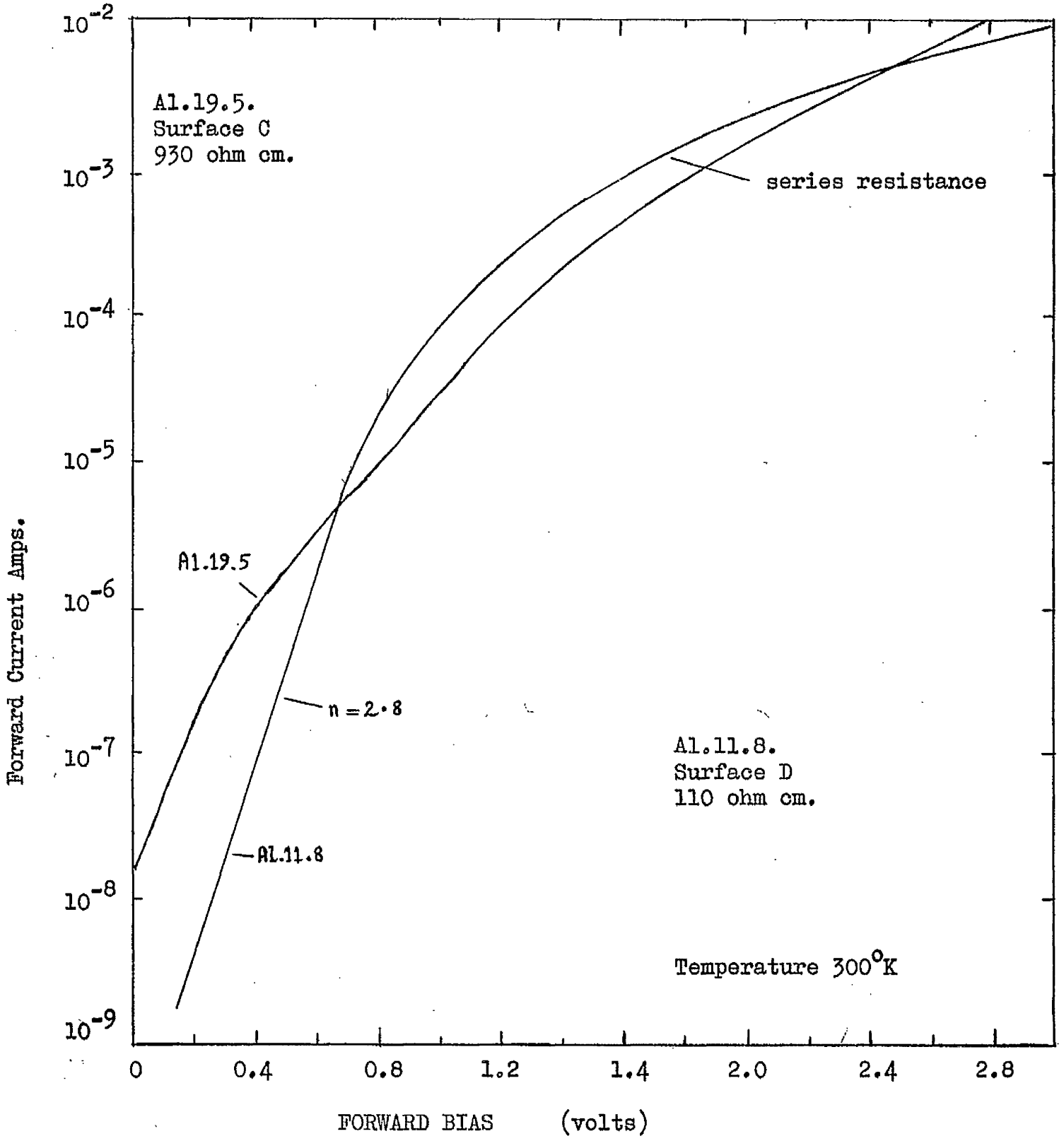


Fig. 5.5(a). Showing how some typical aluminium-silicon diodes obey the diode equation.

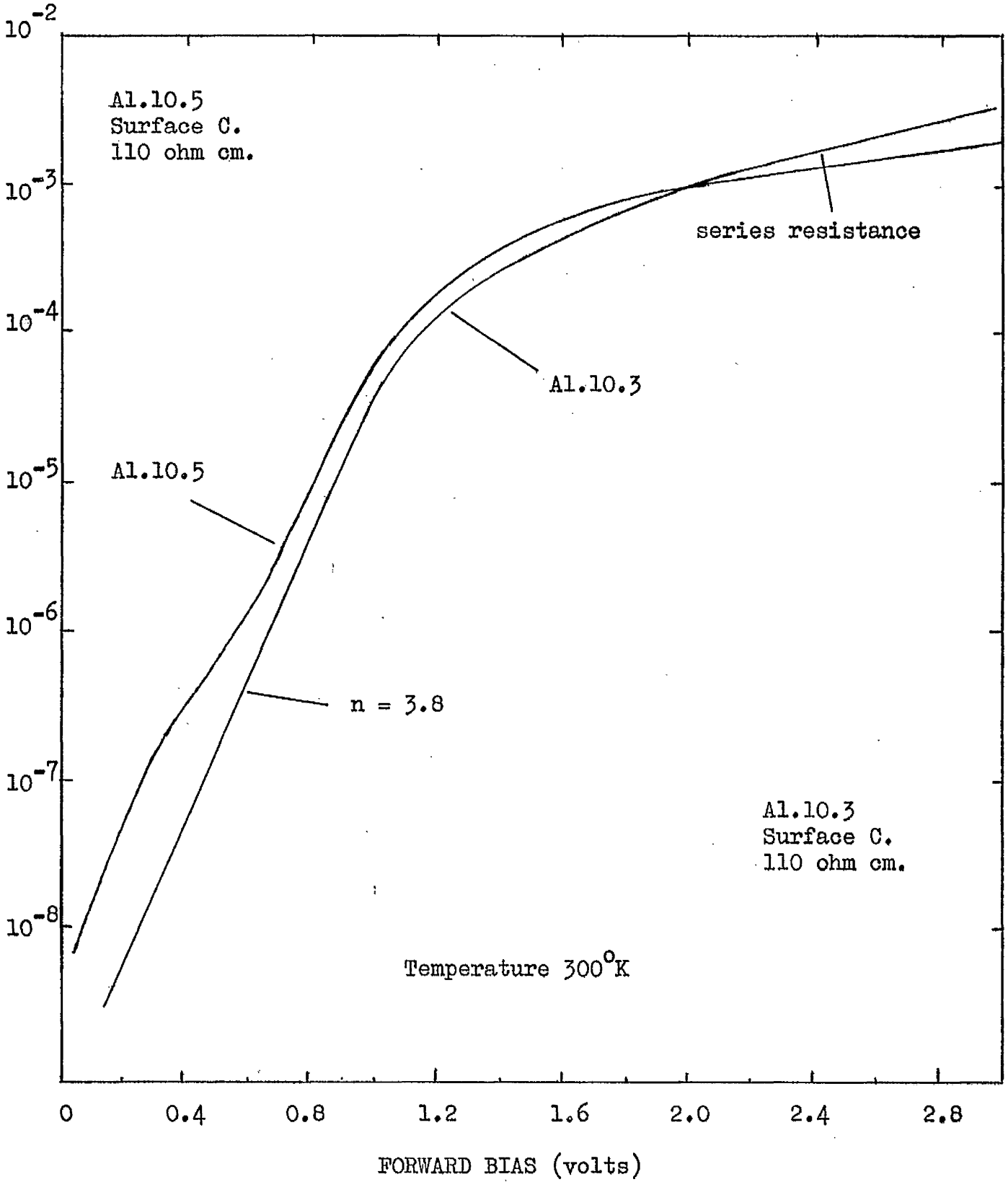


Fig. 5.5(b). Showing how some typical aluminium-silicon diodes obey the diode equation.

The rate of evaporation and thickness of the aluminium films were the same as before. The current-voltage characteristics were plotted:-

(a) Immediately after evaporation in vacuum.

(b) In the chamber one hour later.

(c) Just after air admission.

(d) During re-evacuation of the system.

(e) In air again.

(f) Two days later.

(g) One week later.

All areas yielded almost identical curves at all times and ageing progressed at the same rate for each aluminium-silicon contact.

5.5.2 Results

None of these aluminium-silicon contacts was initially ohmic and the only difference between surface preparations C and D was that the diodes on surface D were more rectifying. There was an insignificant change in the characteristics after one hour with the specimen still in the vacuum chamber. When air was admitted to the system no immediate change took place, but after ten minutes the characteristics changed quickly, Fig. 5.6(a). The system was then re-evacuated and the characteristics re-plotted - but the change was irreversible. There was now a marked degree of rectification and upon exposure to the atmosphere the rectification developed as usual, Fig. 6(b). Note the change in scale of Fig. 5.6(a) and Fig. 5.6(b). The 'knee voltage' of these devices was greater than any of the previous ones.

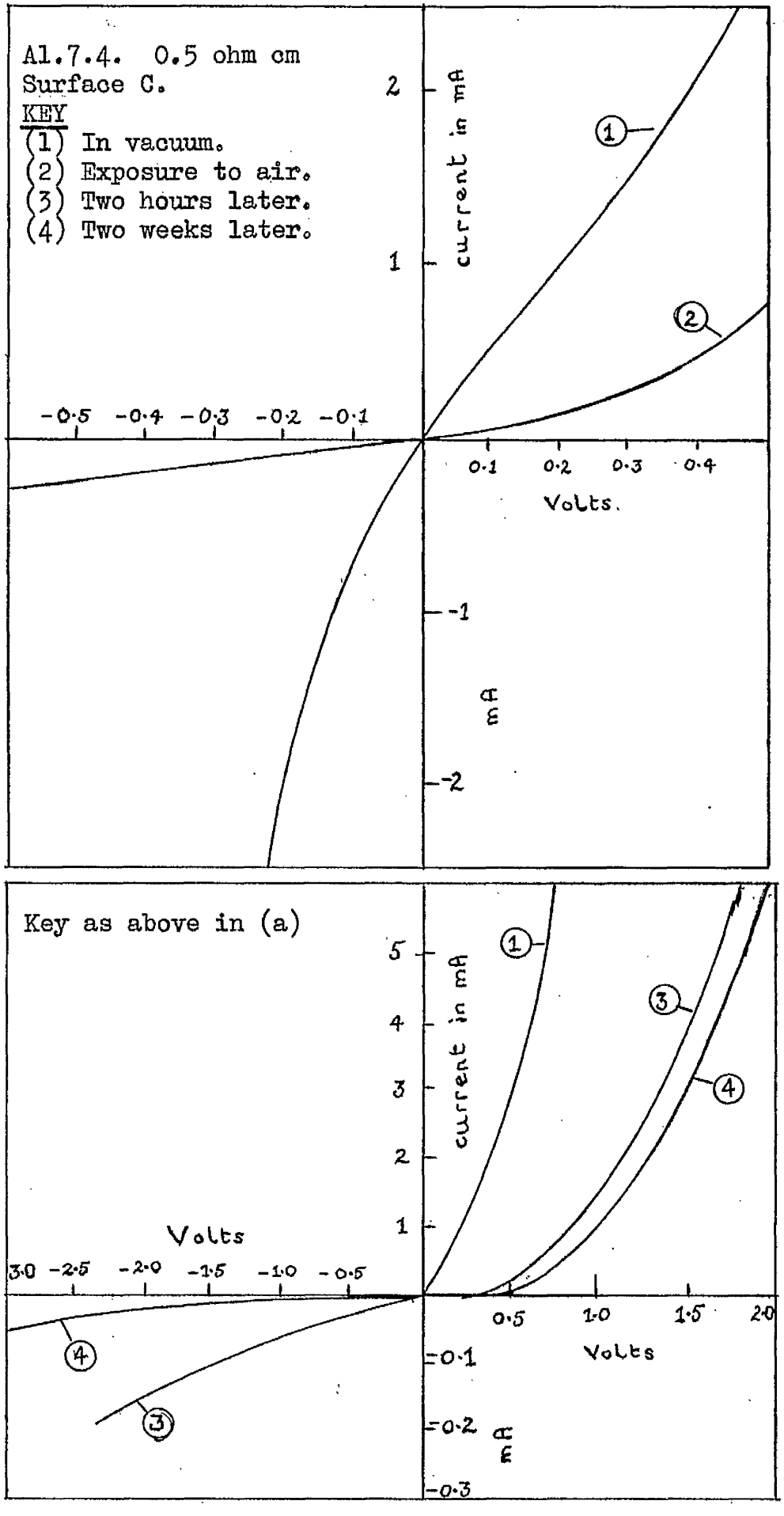


Fig. 5.6. Rectification of Aluminium-Silicon Devices when Device was Exposed to Atmosphere.

It appeared that the exposure of the slices to the atmosphere for a while prior to evaporation inhibited the formation of an ohmic contact between the aluminium and the silicon. Moreover, the rate at which rectification subsequently developed was the same for all aluminium areas on each slice.

5.6 Physical structure of aluminium films

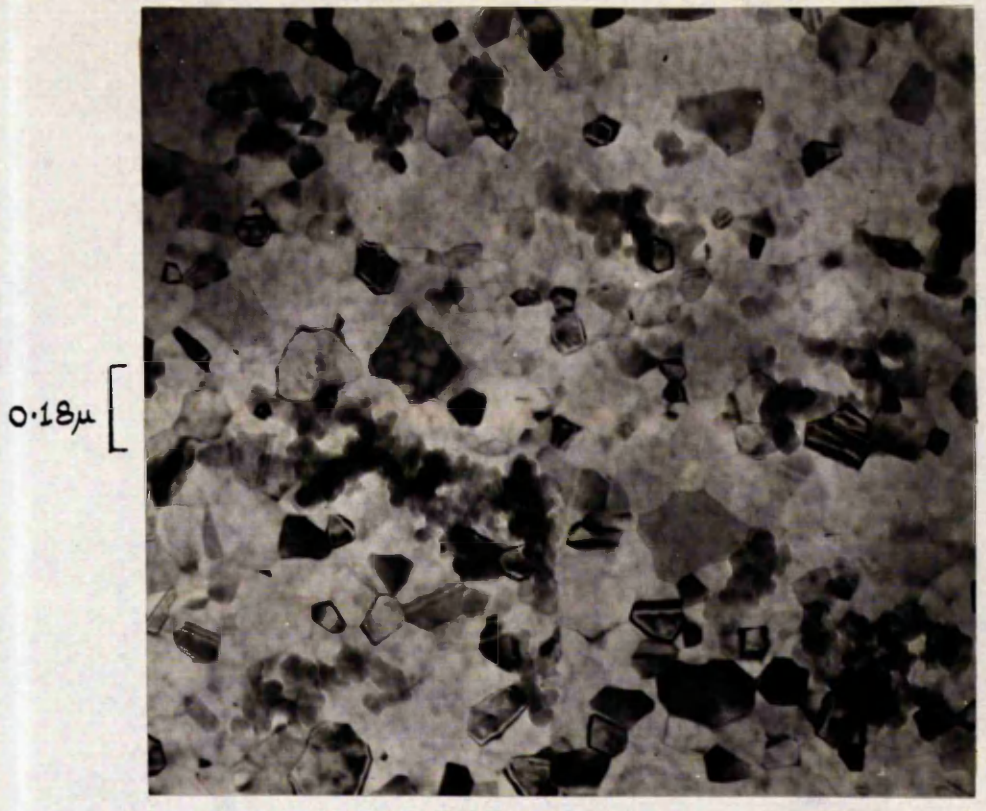
The properties of evaporated aluminium films have been the subject of much research over the last thirty years and this work has been summarised by Holland[4]. Nearly all the work concerning the structure of evaporated films has been on films deposited on alkali halide substrates, by observing the structure as a function of substrate temperature. Recently Vernier, Coquet and Landrot[5] have used electron microscope techniques to investigate the structure of aluminium films on carbon substrates. They observed a textured structure when the rate of deposition was greater than 100 Å/sec. in which the aluminium (111) was parallel to the supporting film. Suito et al.[6] evaporated aluminium films on cleaved rocksalt at room temperature and then annealed them in air for several hours in the temperature range 100 - 600°C and found three types of oxide were formed. I have found only one reference to an investigation of the structure of evaporated aluminium films removed from silicon surfaces. This is by Archer and Atalla[7], who claimed that such films were amorphous - but they did not present any photographs.

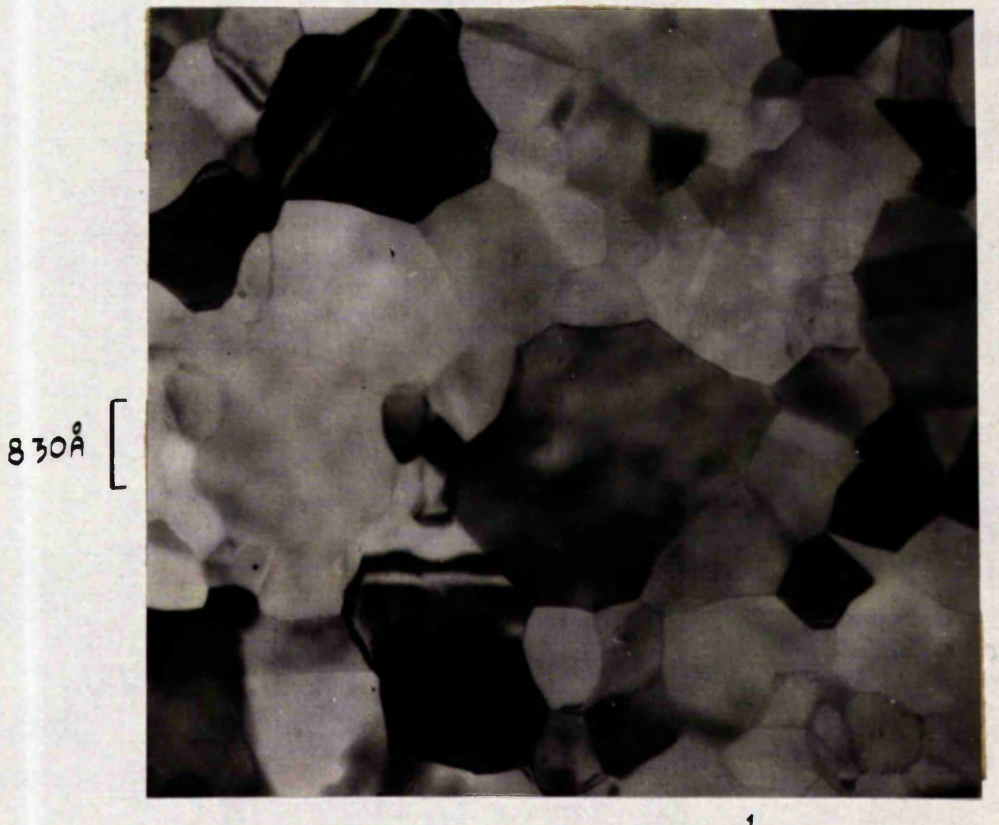
Fig. 5.7(a) and (b) are transmission pictures of an aluminium film deposited at 10 Å/sec. and then removed from the silicon slice. The effect of the rate of evaporation (in the range 2 - 20 Å/sec.) is merely to increase the grain size slightly - the faster the evaporation process the larger the grain size. The grain size is about 0.1μ for the film in Fig. 5.7 and there was a complete absence of any holes in the film whatsoever. The electron diffraction pattern obtained from this film is shown in Fig. 5.8. The pattern is spotty due to the largish grain size and shows that the film is composed of randomly oriented crystal grains of the usual f.c.c. structure.

A very thin film of aluminium deposited on etched silicon under unknown evaporation conditions and which had been subject to the atmosphere for over one year was removed and the diffraction pattern is shown in Fig. 5.9. The diffuse rings are typical of an amorphous structure, almost certainly aluminium oxide in this case.

5.7 Conclusions

Only two major facts emerge from the measurements of the aluminium-silicon contacts. First, the silicon dioxide film on the silicon surface has no appreciable resistance. Secondly, there is a significant correlation between the surface preparation and the life of an evaporated aluminium ohmic contact. Moreover, if freshly etched silicon surfaces are exposed to the atmosphere for a period of time before the aluminium is deposited then true ohmic contacts are not formed at all.





Rate of deposition 10Å sec^{-1}.

Fig. 5.7 Transmission pictures of evaporated aluminium films deposited on etched silicon.

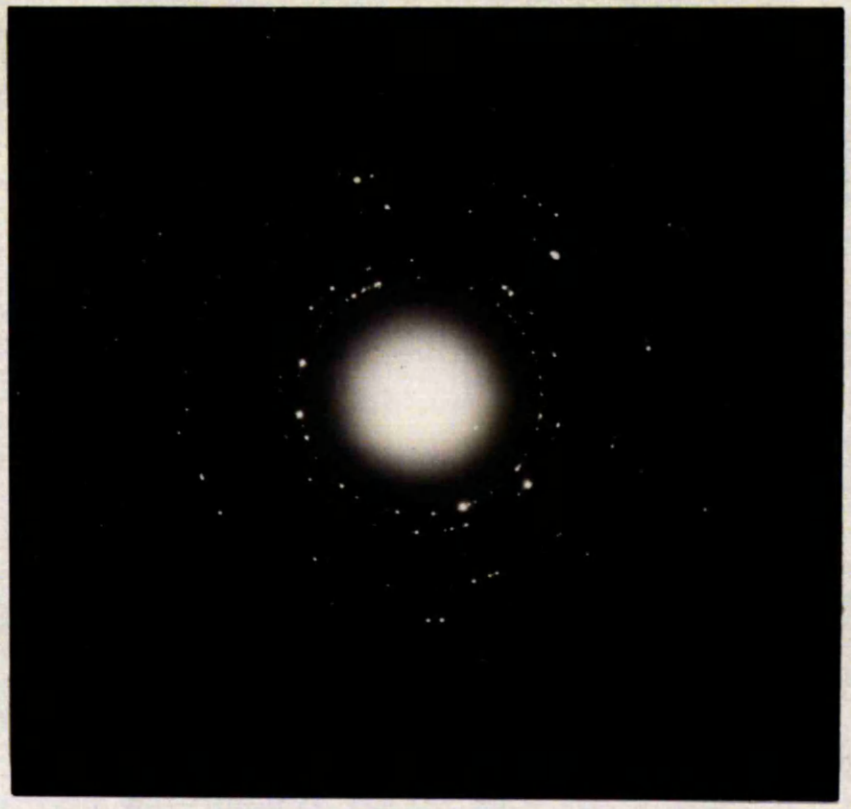


Fig. 5.8 Diffraction pattern from evaporated aluminium film in Fig. 5.7.

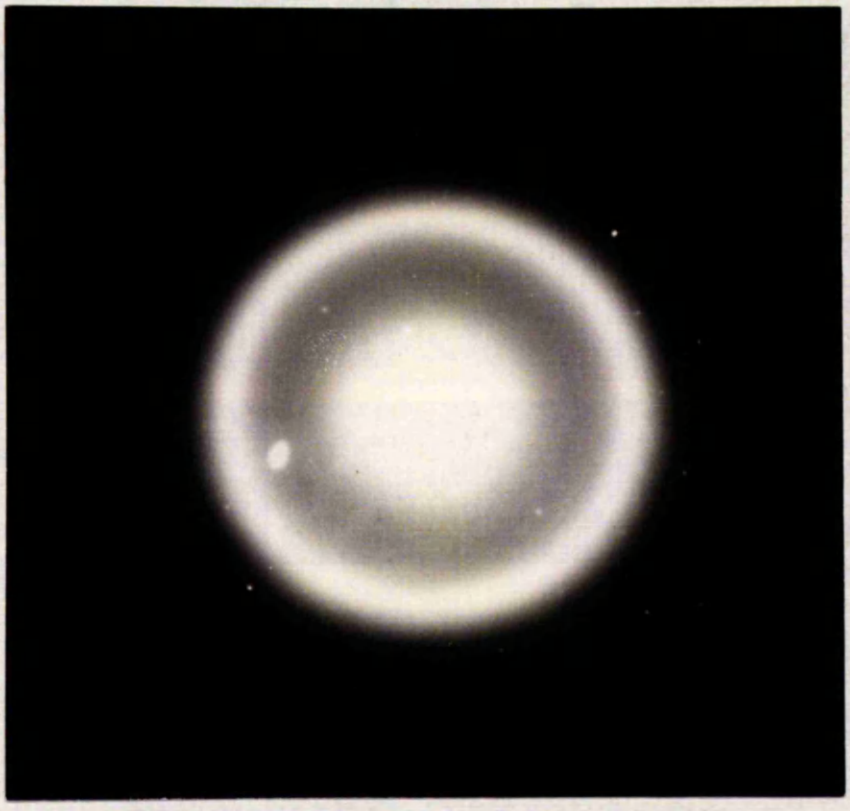


Fig. 5.9 Diffraction pattern from aged aluminium film.

The electron microscope study of the aluminium films revealed that aluminium films evaporated on etched silicon surfaces were not amorphous as reported previously[7] but crystalline. However, removal of a very thin film which had been exposed to the laboratory atmosphere for over one year indicated that an initially crystalline film can deteriorate into a decidedly amorphous structure.

References to Chapter 5

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Chapter 6

Structure of Evaporated Gold Films Deposited on Etched Silicon

6.1 Review of film growth

During the past ten years a large effort has been devoted to the epitaxial deposition of gold from the vapour phase on various types of substrates. The majority of these substrates have been either molybdenum disulphide or one of the alkali halides. The former substrate is generally used for observations of the growth process in situ in the electron microscope so that the degree of alignment of the crystallites may be assessed and the latter substrate is used to facilitate easy film removal. Gold deposited on mica has also received substantial attention. As a result of all this work the mechanism of film growth in terms of nucleation theory and island growth is well documented and literature reviews have been given at regular intervals[1,2,3,4,5]. The important deposition parameters have been summarised in most of these reports.

It is well known that the growth sequence of vapour deposited films consists of a nucleation stage followed by growth and coalescence of the nuclei, leading to a channel stage and finally the formation of a continuous film by the filling in of the holes. Moreover, the liquid-like behaviour of the islands during coalescence has been excellently demonstrated[6].

Although there is much interest in metal-semiconductor contacts fabricated by depositing gold on etched silicon held at room

temperature very little attention has been paid to the structure of the gold films. I have investigated some of the structural properties of these films. The normal methods of device manufacture were adhered to as far as possible.

6.2 Experimental procedure

All depositions were carried out with the silicon substrate held at room temperature. The rate of evaporation and thickness were controlled as explained previously (section 4.2). All silicon slices were prepared as described in section 4.4.2. The temperature rise of the substrate during the deposition process depends on the radiated energy it receives from the source, the kinetic energy of the incident molecules and the latent heat of vaporisation of the condensing molecules. For the samples used in the experiments the magnitude of the temperature rise was estimated at less than $10^{o}C$ and a thermocouple strapped to a substrate indicated a temperature rise of about $3^{o}C$ during the longest deposition.

The gold films were stripped from the silicon using a cold removal technique by immersing the substrates in an HF/HNO_3 mixture (ratio about 1/40) followed by washing in deionised water. Each series of experiments was carried out on one slice of silicon using masking techniques and the slice was later divided into various specimens by means of a diamond tool - this ensured sample homogeneity. The films were examined by the usual electron microscope techniques.

The parameters which were varied are as follows:-

(a) Rate of deposition.

(b) Substrate preparation.

(c) Substrate orientation.

(d) Substrate environment.

6.3 Experimental results

All the gold films removed from the silicon slices fell into one of the following three categories.

Type A - Polycrystalline discontinuous films composed of randomly oriented grains.

Type B - Polycrystalline, continuous, hole-free films composed of randomly oriented grains.

Type C - Polycrystalline, continuous, hole-free films composed of highly oriented grains.

The grain size was always about 200 Å or less and the parameters which affect the growth of each particular film are discussed separately.

(1) Type A films

The governing parameter in this case was the substrate environment. Initially all depositions were carried out at moderate pressures ($<10^{-5}$ torr) without a liquid nitrogen cold trap fitted to the coating unit and regardless how the parameters (a) - (c) were varied the films were always of this type. Typical films are shown in Fig. 6.1. The film thickness was 300 Å and the rates of deposition are as indicated

alongside the figures. Thicknesses of at least 800 Å were necessary before a continuous film was formed.

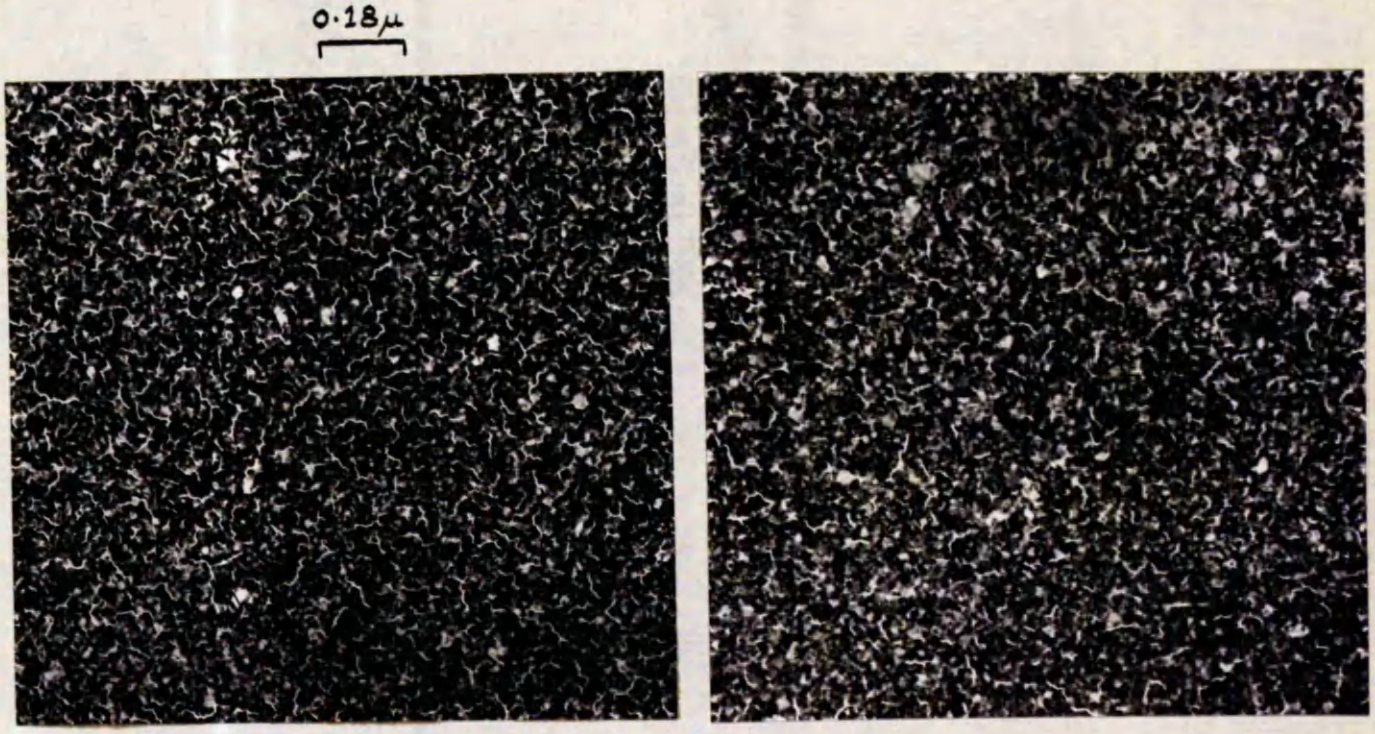
When the cold trap was attached to the system no films of this type were again observed.

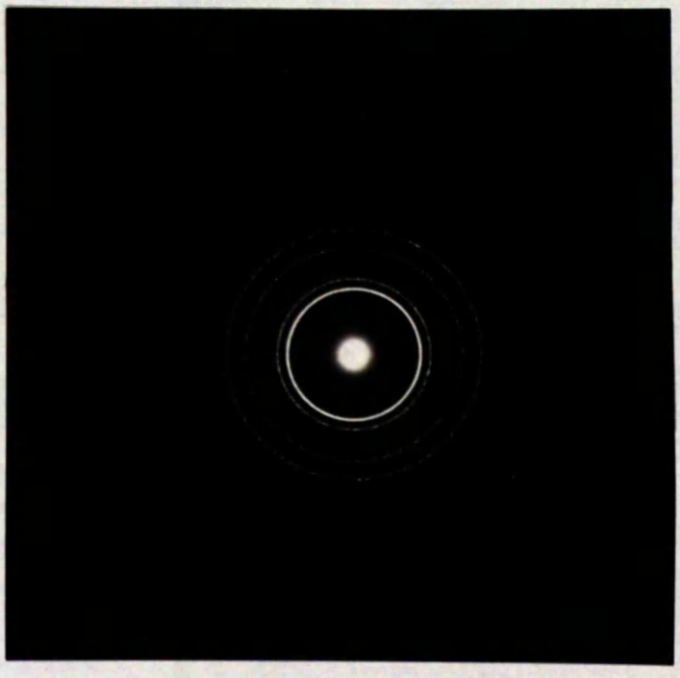
(2) Type B films

These films were characterised by substrate preparation and also by rate of deposition. If the silicon slice was not immediately transferred to the evaporator following etching but left exposed to the air for a day or two then provided the rate of evaporation of the gold waslow enough a type B film was deposited. Fig. 6.2 shows a series of transmission and diffraction pictures for films deposited at rates of 0.5 Å sec^{-1}, 3 Å sec^{-1} and 20 Å sec^{-1} on the same silicon slice which was exposed to the laboratory atmosphere. All the films are of 300 Å thickness. The crystallites became more oriented as the rate of deposition increased.

(3) Type C films

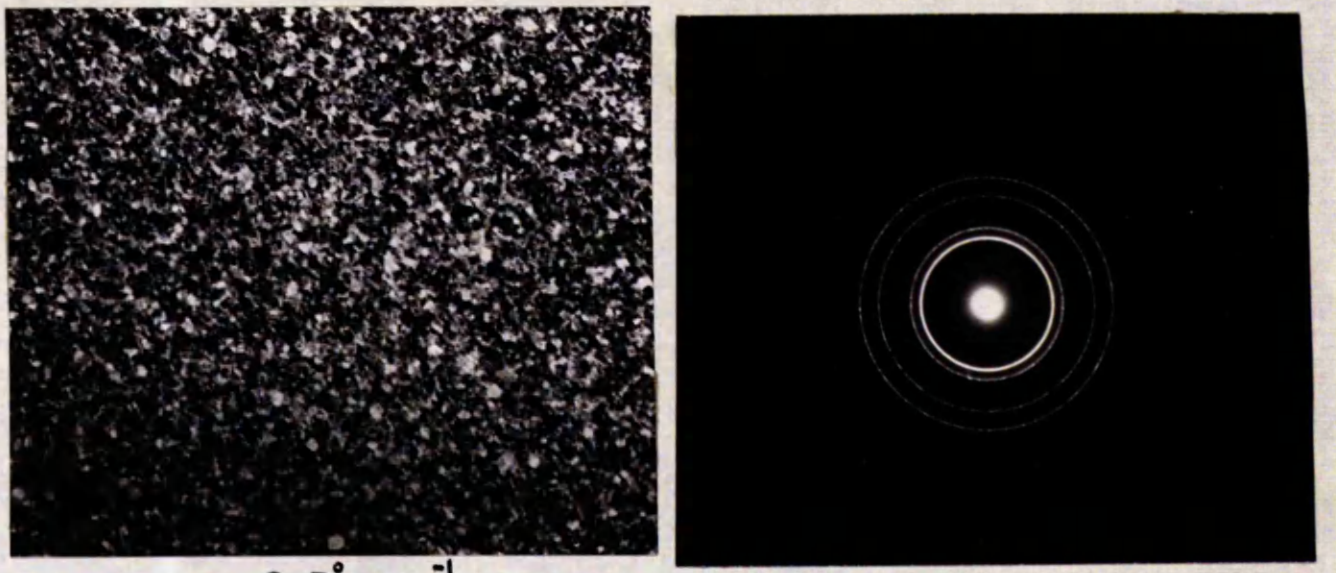
These are the films which were always deposited in later experiments. The important parameters here were the surface preparation and its crystallographic orientation. Provided the gold was deposited on freshly etched silicon (111) faces then a type C film always resulted - in this case the rate of deposition seemed to have little effect on the structure. A sequence of transmission pictures illustrating the film growth at 3 Å sec^{-1} on freshly etched silicon is shown in Fig. 6.3. When the mean film thickness approaches 100 Å the film is



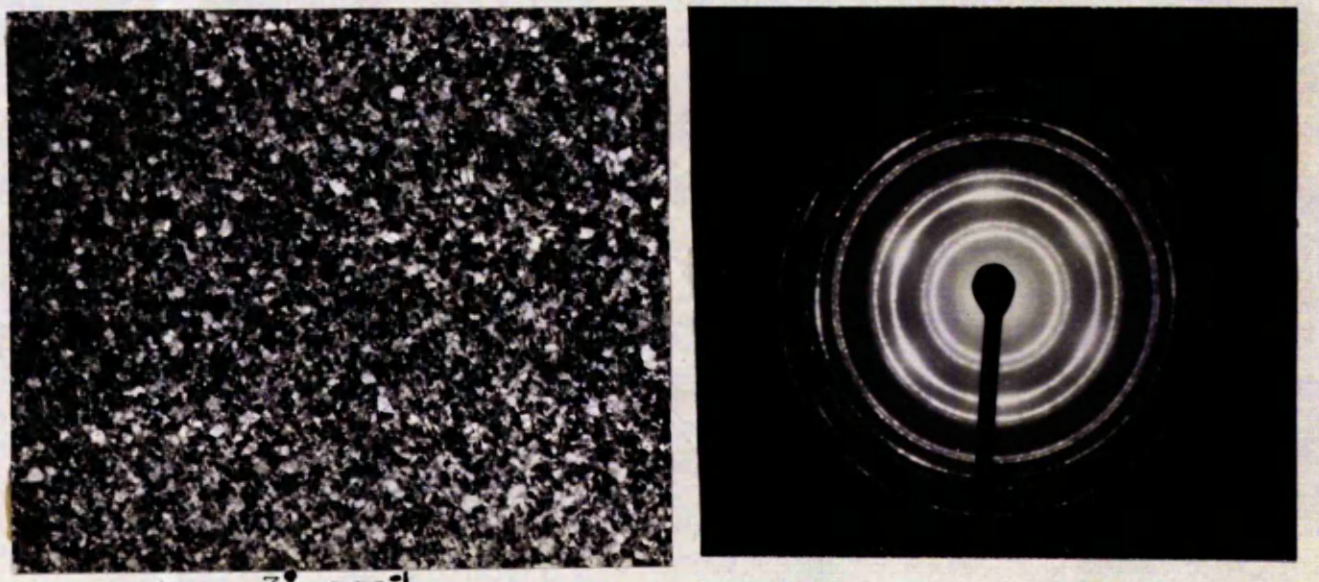


Diffraction pattern.

Fig. 6.1 300Å gold films evaporated on etched silicon with no cold trap fitted to system.

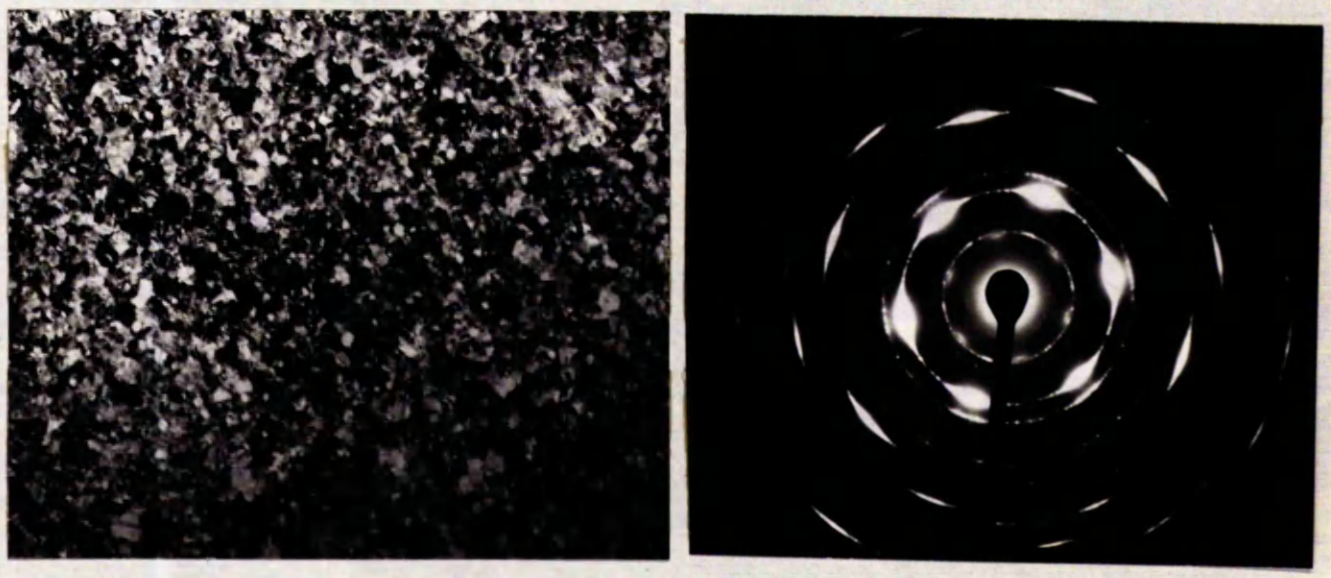


0.5Å sec^{-1}.



0.18μ

3Å sec^{-1}.



20Å sec^{-1}.

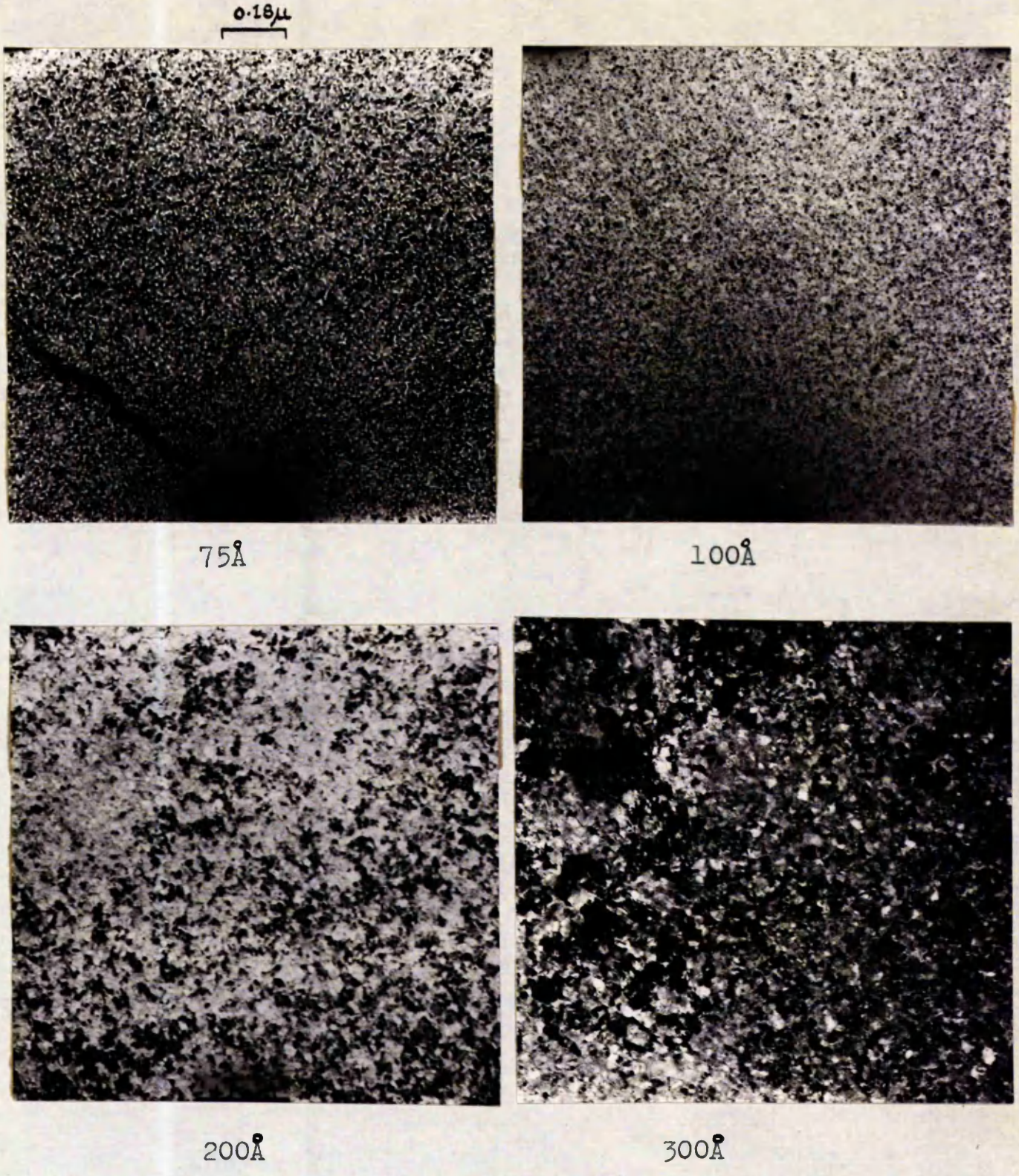
Fig. 6.2 Effect of evaporation rate for 300Å gold films deposited on silicon which was exposed to the atmosphere after etching.

virtually continuous. The effect of annealing one of these films at 100°C for half an hour before removal from the silicon is shown in Fig. 6.4. A small amount of grain growth has taken place. Films deposited on silicon surfaces prepared using the oxide removal technique were composed of crystallites which were particularly highly oriented. Analysis of the diffraction pattern shows that all the oriented films have the (111) face of the gold in the plane of the film (i.e. both the (111) faces of the gold and the silicon are in the same plane). Moreover, the crystallographic directions of the individual gold crystallites are highly oriented with respect to each other.

It is worth noting that these oriented gold films have only appeared on the silicon (111) face. When gold was deposited on both the silicon (100) face and the silicon (101) face (with the silicon still at room temperature) randomly oriented films of type B resulted even though the rate of deposition was varied in the range 0.5 - 20 Å sec^{-1} (Fig. 6.5).

6.4 Discussion

We conclude from the fact that no type A films were observed once the cold trap was added to the system that the film growth for these films was influenced by a contaminating layer of diffusion pump oil over the silicon surface. In the case of the type B films it appears that once an oxide layer of a certain thickness has grown on the silicon surface then the silicon has very little influence on the growth conditions - the critical oxide thickness depending on the rate of evaporation.



Deposition rate 3Å sec^{-1}.

Fig. 6.3(a) Showing the formation of films deposited on freshly etched silicon as a function of thickness.

(Diffraction picture overpage)

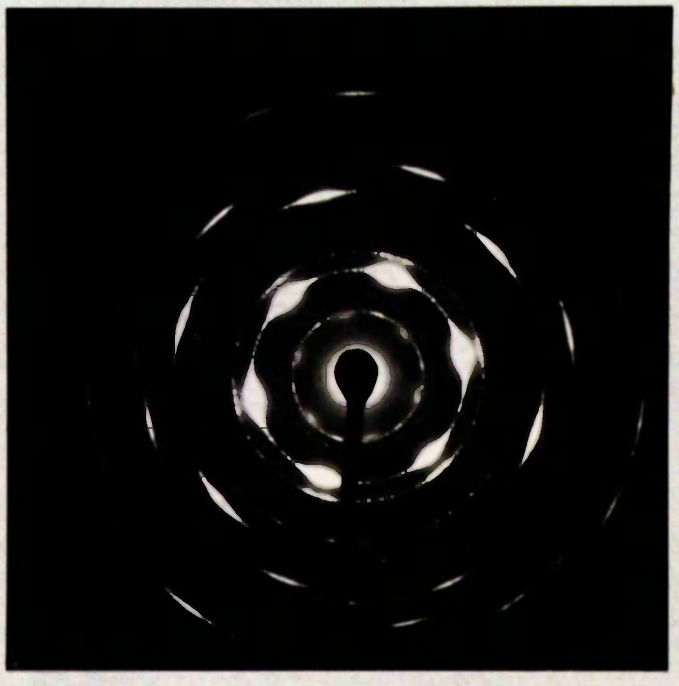


Fig. 6.3(b) Diffraction pattern from 300Å gold film in Fig.6.3(a).

The fact that the films of type B and C are composed of very small crystallites is not very surprising. It is well known that the nucleation rate is considerably higher for low temperature substrates than for high temperature substrates because in the latter case the substrate can provide sufficient energy to the incident molecules to either enable them to re-evaporate or to migrate across the surface of the substrate to a site of lower energy. In the case of gold on room temperature silicon it appears that only a small nucleation barrier exists and that many small, stable, aggregates are formed in the initial stage of the film growth, resulting in a continuous film at a relatively small average thickness (about 100 Å). The orientation of the silicon substrate is certainly an important parameter influencing the structure of the gold films. However, it is not clear from these investigations that the strong periodicity of the substrate surface is in fact the predominant force influencing the condensing atoms since it is known that textured gold films can be found on glass substrates[7].

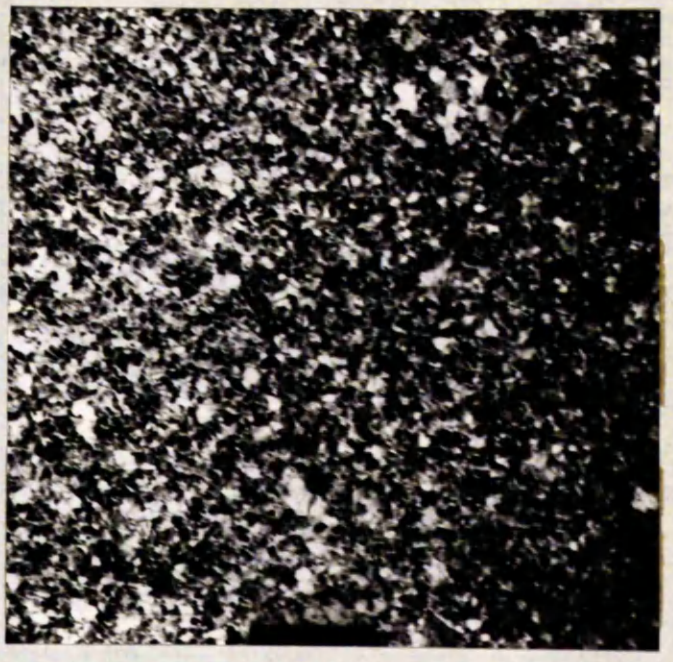
It is interesting to note that recently gold has been deposited on the germanium (111) face at room temperature resulting in the gold (111) plane aligning with the germanium (111) plane[8]. Also, epitaxial gold films have been deposited on the low index faces of heated germanium substrates[9]. Apart from these reports there has been little attention paid to the structure of metal films on semiconductor surfaces.

Before anneal.

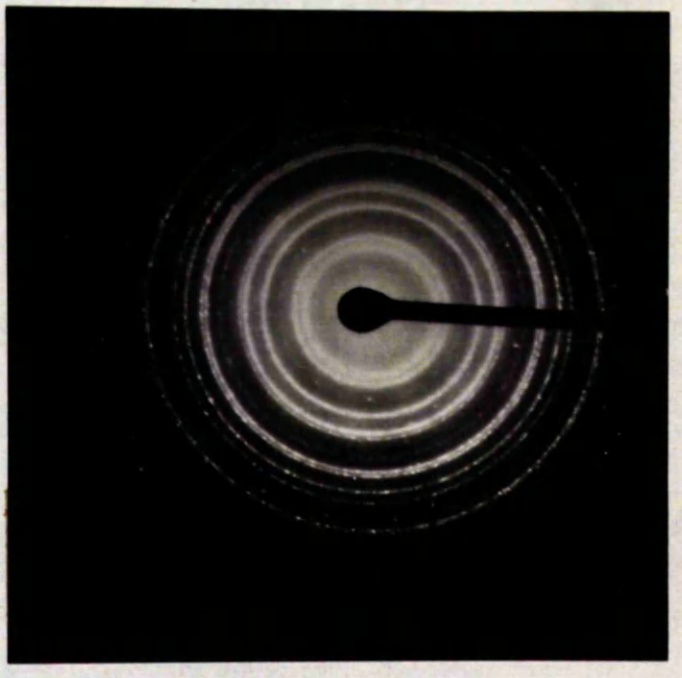
After anneal.

Film thickness 300Å Rate of deposition 3Å $sec.^{-1}$

Fig. 6.4 Effect of annealing oriented gold films.



Transmission



Diffraction

Fig. 6.5 300Å gold film deposited on the silicon (100) face at 20Å sec^{-1}.

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Chapter 7

Resistivity Measurements of Gold Films on Silicon

7.1 Introduction

Although electron microscopy is a powerful tool for examining the physical structure of thin crystals it is not the best means of assessing the imperfection density of metallic films. According to transport theory, for a perfect, stationary, metallic lattice the electron waves would pass through unhindered and therefore no electrical resistance would be observed. However both the thermal motion of the atoms and any crystal imperfections cause scattering of the conduction electrons, thereby giving rise to a finite resistance of the metal. By measuring the resistance of thin metallic films as a function of thickness the important scattering processes taking place may be identified. This additional information, coupled with electron microscope studies leads to a realistic assessment of the structure of the films.

Matthiessen's rule states that

$$\rho_{total} = \rho_{ideal} + \rho_{residual}$$

where ρ_{total} is the total resistivity, ρ_{ideal} is the resistivity due to scattering arising from the thermal motion of the lattice (strongly temperature dependent in a reversible fashion) and $\rho_{residual}$ is the resistivity arising from lattice defects (generally temperature independent for bulk metals - but not necessarily so in the case of thin evaporated films).

For thin films when one boundary dimension is comparable to the mean free path of the conduction electrons, then another component of resistivity becomes important and must be added to the above rule. The total resistivity is now given by

$$\rho_{total} = \rho_{ideal} + \rho_{residual} + \rho_{thickness}$$

where $\rho_{thickness}$ is the resistivity due to boundary scattering of the electrons.

The actual magnitude of $\rho_{thickness}$ depends solely on the type of scattering which takes place at the boundary of the thin film. The two extreme cases are those of perfectly diffuse scattering and perfectly specular scattering (both have been dealt with theoretically by Sondheimer[1]). Diffusely scattered electrons completely lose their drift velocity upon collision with the boundary whereas the velocity component normal to the surface is reversed when an electron is specularly scattered. In the latter case $\rho_{thickness}$ becomes zero.

A conduction electron has a de Broglie wavelength of about 5 Å associated with it and so any surface which is smooth on this scale should ensure that specular reflection takes place. In the case of most types of substrates used in the deposition of thin films the above criterion is not fulfilled and the reflection at the boundaries is very much diffuse. The resistivity of annealed gold films on bismuth oxide[2,3] have been interpreted in terms of nearly specular reflection but are not very convincing. Recently Chopra et al.[4], sputtered gold on freshly cleaved mica held at 300°C and obtained

single crystal films. Their resistance-thickness curves are indicative of specular scattering at the crystal boundaries.

From transport theory the conductivity, χ , of a metal with a single conduction band and which is isotropic is given by[5]

$$\chi = \frac{Ne^2}{m} \tau_F \tag{7.1}$$

where N is the number of electrons per unit volume, m is the electron effective mass, e the electronic charge and τ_F the relaxation time associated with electrons at the Fermi level. This leads to the definition of a mean free path ℓ, given by:

$$\tau_F v = \ell \tag{7.2}$$

where v is the electron velocity at the surface of the Fermi distribution. The collisions must be elastic (i.e. the magnitude of the scattered electron's wave vector, $|\underline{k}|$, is unchanged by the collison) in order to define a relaxation time for the scattering process. In the case of pure metals above the Debye temperature, the scattering is predominantly due to lattice vibrations and l becomes the phonon scattering mean free path l_p (400 Å for gold). For randomly distributed imperfections we can also define a mean free path l_i but it is usual to include both the lattice and imperfection scattering in the relation:

$$\frac{1}{\ell} = \frac{1}{l_i} + \frac{1}{l_p} \tag{7.3}$$

where ℓ is the effective mean free path.

Here the imperfection scattering includes scattering from impurity atoms, structural defects and grain boundaries.

In the case of a thin film the artificial limitation of the mean free path, ℓ, by the boundaries, causes an increase in the resistivity, which, for completely diffuse boundary scattering is given by the Fuchs-Sondheimer relation:

$$\rho = \rho_\infty \left(1 + \frac{3\ell}{8t}\right) \qquad \text{when } (t > \ell) \tag{7.4}$$

and

$$\rho = \frac{4\rho_\infty}{\left(\frac{3t}{\ell}\right)\left[\ln \frac{\ell}{t} + 0.4228\right]} \qquad \text{when } (t < \ell) \tag{7.5}$$

where t is the thickness of the film.

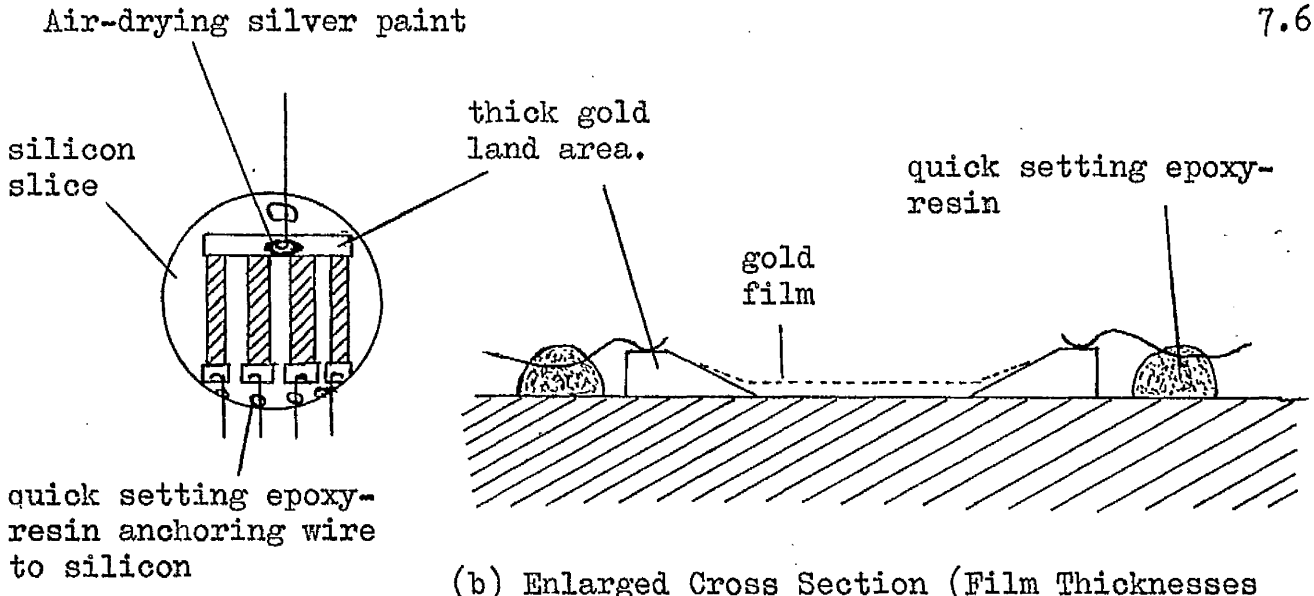
The history of attempts to relate resistivity-thickness curves with these equations and the requirements of such measurements have been reviewed by Mayer[6]. It was decided to measure the resistance of gold films deposited on etched silicon as a function of thickness in order to determine the effective mean free path, ℓ.

7.2 Experimental

Slices of 4,000 ohm cm n-type silicon were prepared as described in section 4.4.2. The etch consisted of 50 cc HNO_3, 20 cc CH_3COOH and 15 cc HF, and the etch time was seven minutes. Land strips were first of all evaporated on the silicon and leads attached to these areas by means of air drying silver paint (Johnson Matthey FSP.51). The leads were pinned to the silicon with a drop of quick setting (45 sec) epoxy resin, Fig. 7.1. Four areas of gold 1 x 0.15 cm

were deposited on each slice at the usual rate for oriented growth (3 Å/sec). The thickness of each area was different and was determined from a microscope slide placed alongside the specimen. The above method of making contact to the gold was perfectly satisfactory for film thicknesses greater than 100 Å, provided the land areas were tapered as shown in Fig. 7.1(b). For measurements with $t < 100$ Å, contact was made by evaporation onto the resistive film strip ends and land areas after the main deposition had taken place (this was achieved by rotating masks). When the former contact technique was used, anomalous effects were observed for films with $t < 100$ Å when gaseous ambients were admitted to the system and these effects disappeared when the latter method of contact was employed. [Such environmental changes have been observed by a number of workers[7,8] using the first contact technique - their observations are of dubious origin and may well be due to weak regions of the film where it joins the contact areas].

All resistance values were made using a MarconiBridge TF2700. A 4-probe technique was used on both the thickest and the thinnest films deposited and measured resistivities were identical with the values obtained from the bridge method - indicating negligible contact resistance. The measurements were initially recorded immediately following the deposition process with the specimens in situ and resistance values obtained for the thickness range 80 - 800 Å.



(a) Plan View.

(b) Enlarged Cross Section (Film Thicknesses Greatly Exaggerated).

Fig. 7.1. Illustrating method of resistivity measurement.

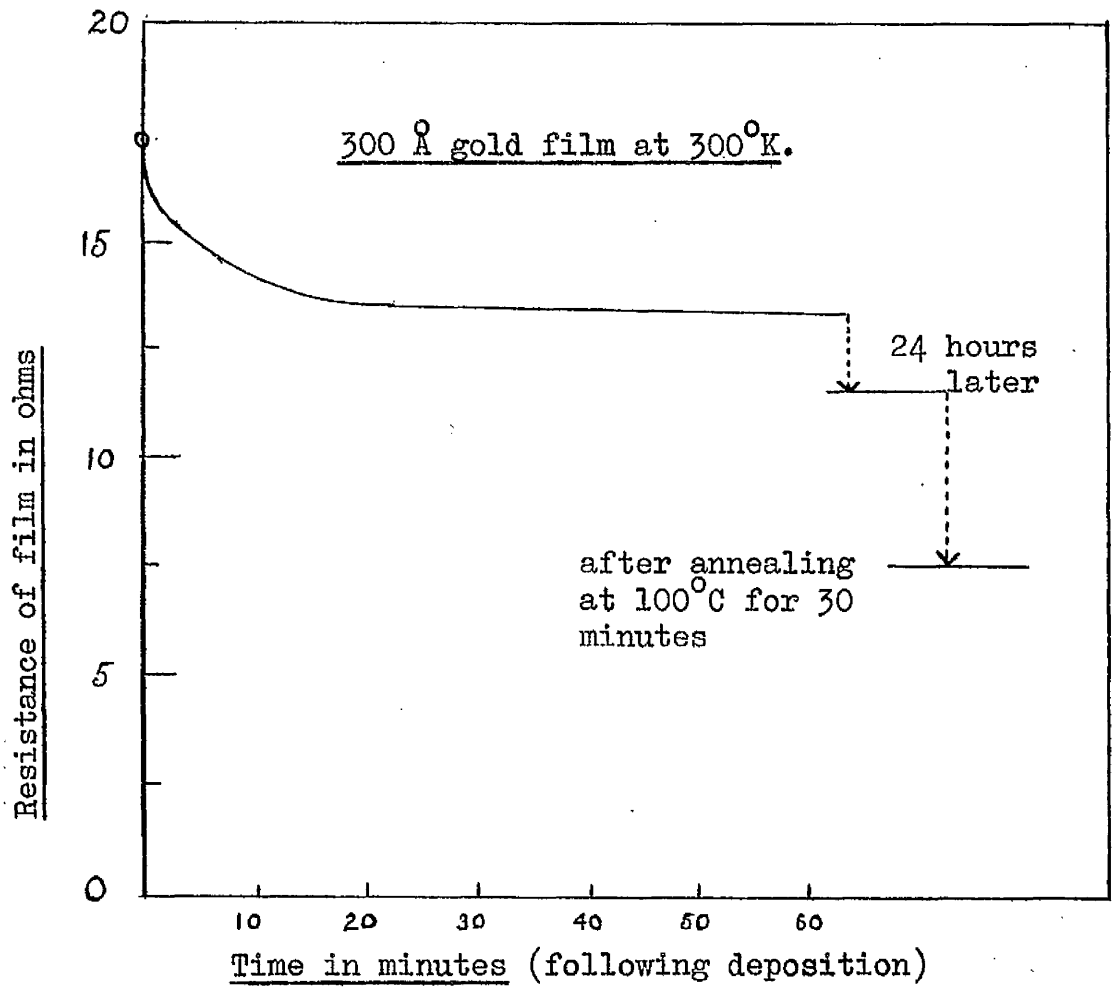


Fig. 7.2. Resistance-time plot of a typical gold film.

7.3 Results

After deposition of the gold the resistance of all films decreased with time. A typical resistance-time plot is shown in Fig. 7.2. At first there was a rapid drop of resistance (probably due to the film cooling) and this was followed by a gradual decrease which lasted about one week or longer. Obviously any resistance-thickness relationship was quite meaningless until the film became stable and it was found that annealing the films for about half an hour at 100°C produced a dramatic reduction in the resistivity. After annealing the film was completely stable and no further change could be detected. Subsequent annealing at 150°C or 200°C had negligible effect but heating above 200°C caused the resistance to increase - presumably due to agglomeration of the gold. All films for the thickness-resistivity plot of Fig. 7.3 were annealed at 100°C for half an hour following the gold deposition.

The Fuchs-Sondheimer relation for diffuse scattering and for $t > \ell$ (equation 7.4) was fitted as follows. From equations 7.1 and 7.2 $\rho = D/\ell$, where D is a constant which has the value 9.8×10^{-12} ohm cm^2 for gold (taking $\rho_{bulk} = 2.45 \times 10^{-6}$ ohm cm and $l_p = 400$ Å). This value of D should apply to gold films as well as to bulk gold (Chopra et al.[4] have shown that lp is the same for films). Thus, for the films $\rho_\infty = D/\ell$, where ℓ is the mean free path including both imperfection and lattice scattering and putting this in equation 7.4,

$\rho = \frac{D}{\ell}\left(1 + \frac{3\ell}{8t}\right)$. At t = 750 Å, $\rho = 6 \times 10^{-6}$ ohm cm, so ℓ = 173 Å. Hence, ρ is given by:

$\rho = 5.65 \times 10^{-6}\left(1 + \frac{66}{t}\right)$ ohm cm, when t is expressed in Å units. This curve is drawn in Fig. 7.3.

The experimental points agree quite favourably with the Fuchs-Sondheimer equation provided t > 100 Å. The abrupt drop in resistivity as the thickness passes through the critical range 80 - 100 Å is due to the film being at the coalescence stage of film growth (Chapter 6).

Taking ℓ = 173 Å and l_p = 400 Å, then from equation 7.3 the mean free path for imperfection scattering, l_i, is given by l_i = 305 Å.

7.4 Discussion

From the resistivity-thickness plot for annealed gold deposited on etched silicon at room temperature it is apparent that the boundary scattering is diffuse and that the effective mean free path of electrons is about 170 Å. This value of ℓ compares very poorly with the value (350 Å) obtained by Soshea and Lucas[9] for gold deposited on similar surfaces but in an ion-pump system. This implies that the imperfection density of the films deposited in the diffusion pump oil system is very much greater than in an ion-vac system. This large discrepancy is not so surprising when one bears in mind the huge difference that the addition of the liquid nitrogen cold trap made to the physical structure of the films (Chapter 6).

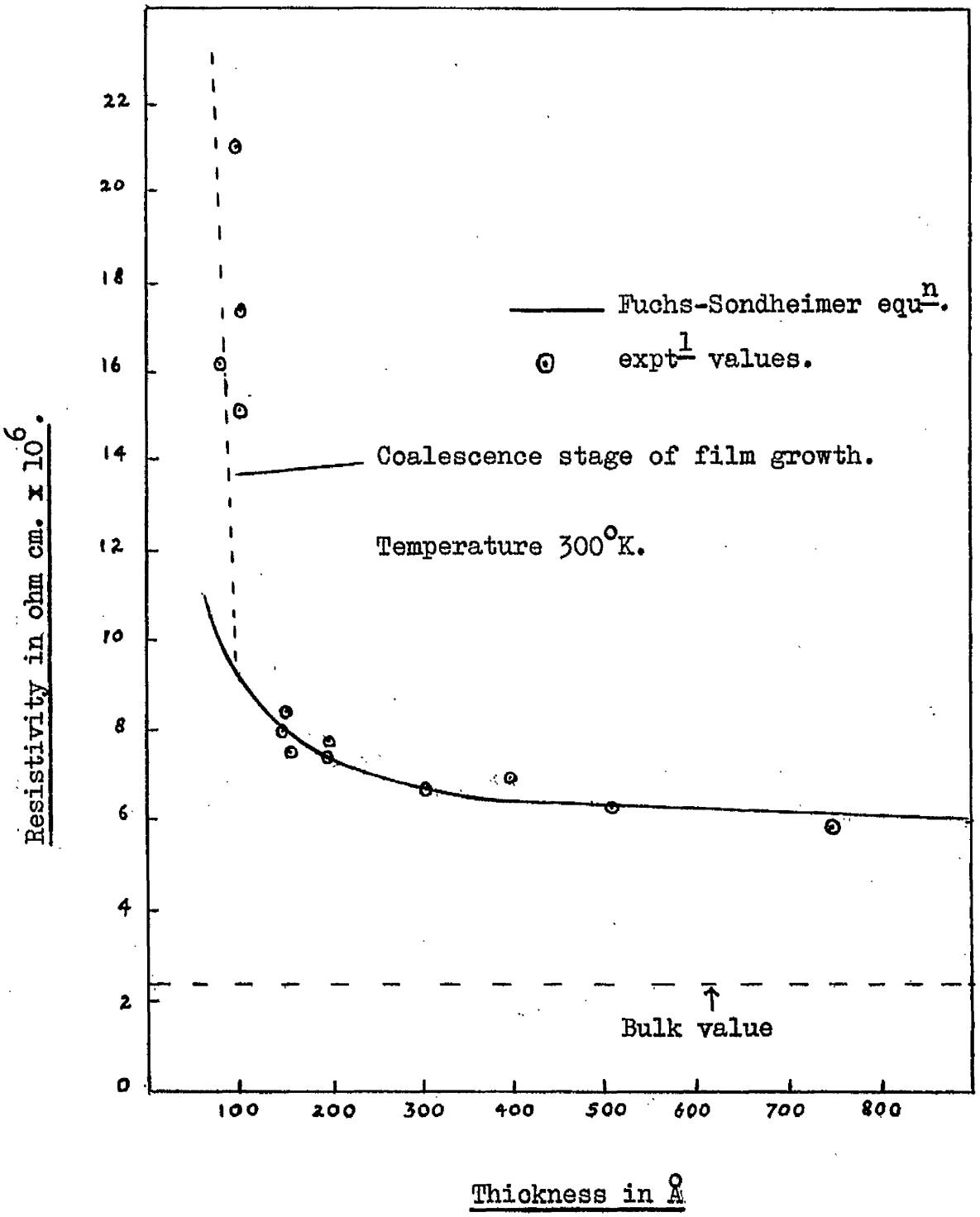


Fig. 7.3. Resistivity-thickness plot for annealed gold on silicon.

The decay of resistance of the films with time is probably caused by self annealing, in which many of the gross lattice imperfections are removed - this process being assisted when the films are gently heated to 100°C - although it has been suggested that the dramatic reduction in the resistivity upon annealing may be due to an expulsion of occluded gas[2]. The most probable explanation is a reduction of the imperfection density accompanied by an increase in grain size, since the electron microscope observations indicate that structural changes do take place during the annealing process.

The fact that the effective mean free path is so small is supported by photoexcitation measurements involving the transport of hot electrons in the gold films (Chapter 8). Moreover, Turner[10], using the same type of vacuum system and surface preparation failed to observe hot electron effects in gold films which were part of a semiconductor-metal-semiconductor sandwich - this is discussed more fully later (section 8.6). Accordingly we conclude that the gold films deposited on etched silicon were structurally very imperfect although the small crystallites were highly oriented.

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Chapter 8

Measurement of Gold-Silicon Barrier Height

8.1 Introduction

In section 3.4.1 it was pointed out that the value of the metal-semiconductor barrier height, ϕ_{MS}, was an important parameter in determining the magnitude of the reverse current in metal-semiconductor junctions. There are several experimental methods of determining ϕ_{MS}.

(a) Capacitance plots

From equation 3.3 it can be seen that the differential capacitance C of a metal-semiconductor junction is related to the applied voltage V_A as follows:

$$\frac{1}{c^2} = \text{constant } (V_A + V_D)$$

Thus by plotting $1/c^2$ versus V_A the value of V_D can be derived from the intercept on the voltage axis. The capacitance plot can be made in two ways. First, if we assume that the system is a majority carrier one in which the minority carriers can be neglected, then by superimposing a small a.c. signal on the diode the differential capacitance can be measured as a function of V_A using a suitable a.c. bridge. This method assumes a knowledge of the equivalent circuit of the device and a large number of deviations from the ideal case arise, many of which have been dealt with by Goodman[1] Secondly,

the diode can be placed in series with a very much smaller known capacitance and a voltage pulse applied to the combination. The voltage developed across the diode is a measure of its capacitance. This method has been used to determine the capacitance of large area surface-barrier diodes[2].

The value of ϕ_{MS} is then obtained by adding the energy difference between the Fermi level and the conduction band edge to the energy derived from the diffusion potential measurement.

(b) Current-voltage characteristics

Assuming that the ideal diode equation (2.7) holds then I_S can be obtained from both the forward and the reverse characteristics. The value of ϕ_{MS} corresponding to this value can then be calculated from equation (3.15).

(c) Activation plots

The value of I_S, derived as in (b) can be plotted as a function of temperature and the activation energy obtained. Turner[3] has done this for evaporated gold on low resistivity silicon.

(d) Optical threshold plots

When photons are incident on a metal-semiconductor junction then a fraction of the photons will be absorbed in the metal and some of the conduction electrons are excited to higher energy levels. If $\phi_{MS} < h\nu < Eg$ then the thermal equilibrium conditions (section 3.4.1.1) will be upset and hot electrons from the metal cross the metal-semiconductor interface, thereby generating a photocurrent. In certain

circumstances (see Appendix A) the photocurrent per absorbed photon, Y, is related to the photon energy $h\nu$ by:

$$Y = \text{constant.} \left[h(\nu - \nu_o)\right]^2 \qquad (8.1)$$

where $h\nu_o$ is the threshold energy (equal to ϕ_{MS}). (See Appendix A for a full treatment.)

Consequently, a plot of $Y^{\frac{1}{2}}$ versus $h\nu$ is a straight line whose intercept on the energy axis is the threshold energy $h\nu_o$. Such a plot is commonly termed a Fowler plot and is based on Fowler's method of determining the true photoelectric threshold[4]. This method has been used to measure the ranges of photoexcited holes and electrons in thin metal films[5,6,7,8], besides the magnitude of the barrier ϕ_{MS}.

For our large area diodes it was decided to measure ϕ_{MS} using the last method because methods (b) and (c) rely on the ideal diode equation and the diodes remaining perfect over a temperature range. Again, method (a), although very attractive, assumes a knowledge of the equivalent circuit and for a strict interpretation one must operate at the correct frequency. Moreover, interfacial layers, if they exist, affect capacitance methods greatly but not the optical threshold measurement.

The conditions imposed by equation (8.1) can be slightly relaxed in the case of gold films. The silicon bandgap, Eg, is 1.08 eV (at room temperature) and so for wavelengths less than 1.1 μ silicon absorbs strongly. We are interested in wavelengths greater

than 1.1μ for our measurements and Crowell et al.[6] have shown that absorption in gold films is independent of wavelength for radiation greater than 1.0μ; Fig. 8.1 has been interpreted from their data. This result implies we can regard Y as the photocurrent per incident photon. [The actual values quoted by Crowell[6] are for gold on glass and these values have since been corrected for gold on silicon by Soshea and Lucas[8] - this is important for attenuation length measurements - but the variation with wavelength was not questioned.]

8.2 Experimental apparatus and preliminary investigations

The experimental arrangement is shown in Fig. 8.2. A Leiss double monochromator with quartz prisms was used with a tungsten ribbon filament projector lamp as a source. The tungsten lamp was fed from a 20 A d.c. supply and the voltage across the lamp was maintained at 7 V. The light was chopped at just less than 500 c.p.s. and after passing through the monochromator the light fell on the specimen placed at the exit slit. The photocurrent was measured by means of a Brookdeal Phase Sensitive Detector, Model PD629. In fact the signal was fed into a Brookdeal Low Frequency Voltage Amplifier LA635 which was coupled to the PSD and the balanced output read from a Brookdeal Model MU947 meter unit. The maximum gain with this apparatus was 56,200. A 6 V p/p reference signal for the PSD was taken from a Fairchild photodiode located in the chopper unit. For maximum sensitivity it was found necessary to box in the device and exit slit of the monochromator, in order to reduce the dark signal of the gold-silicon junction.

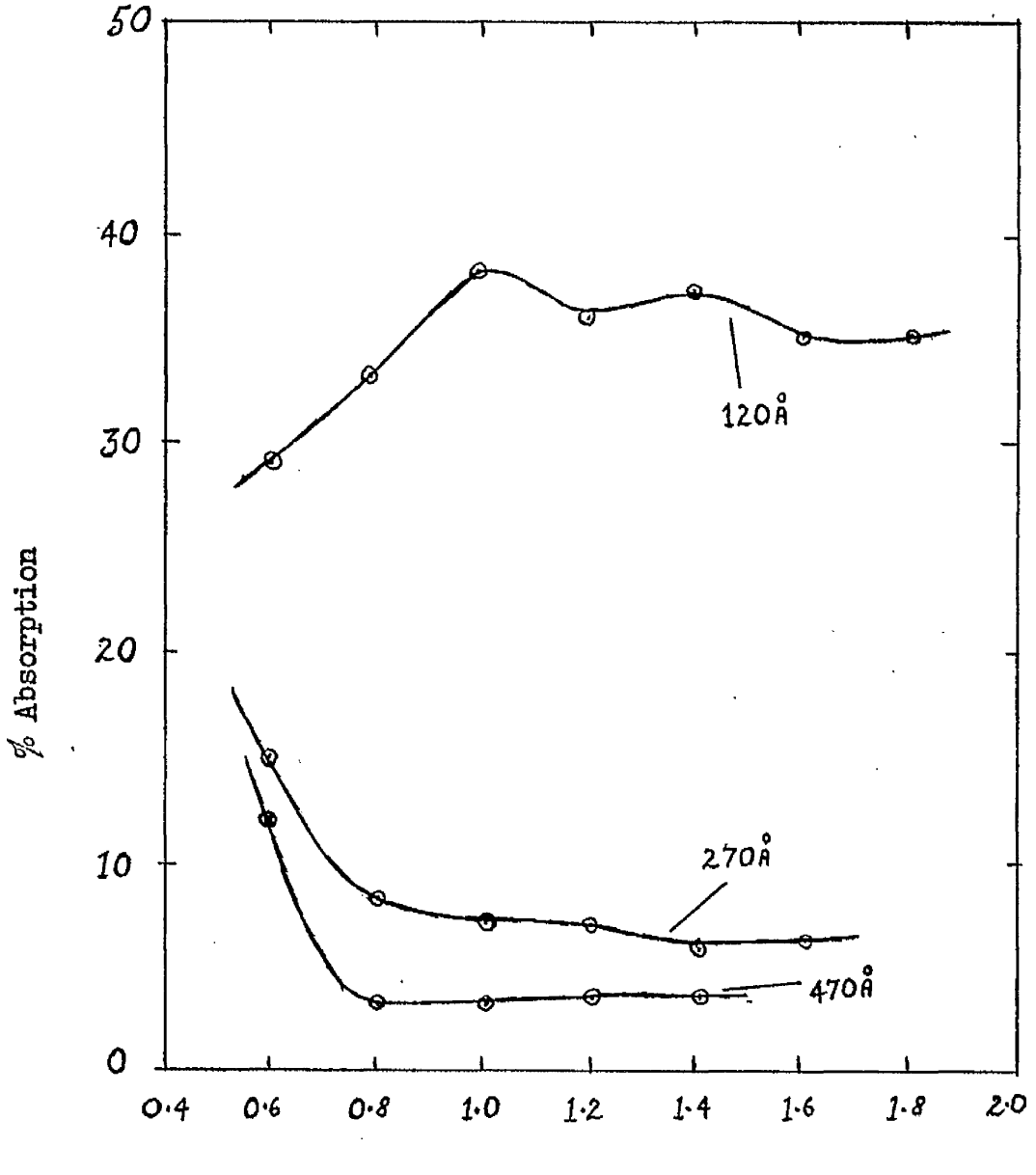
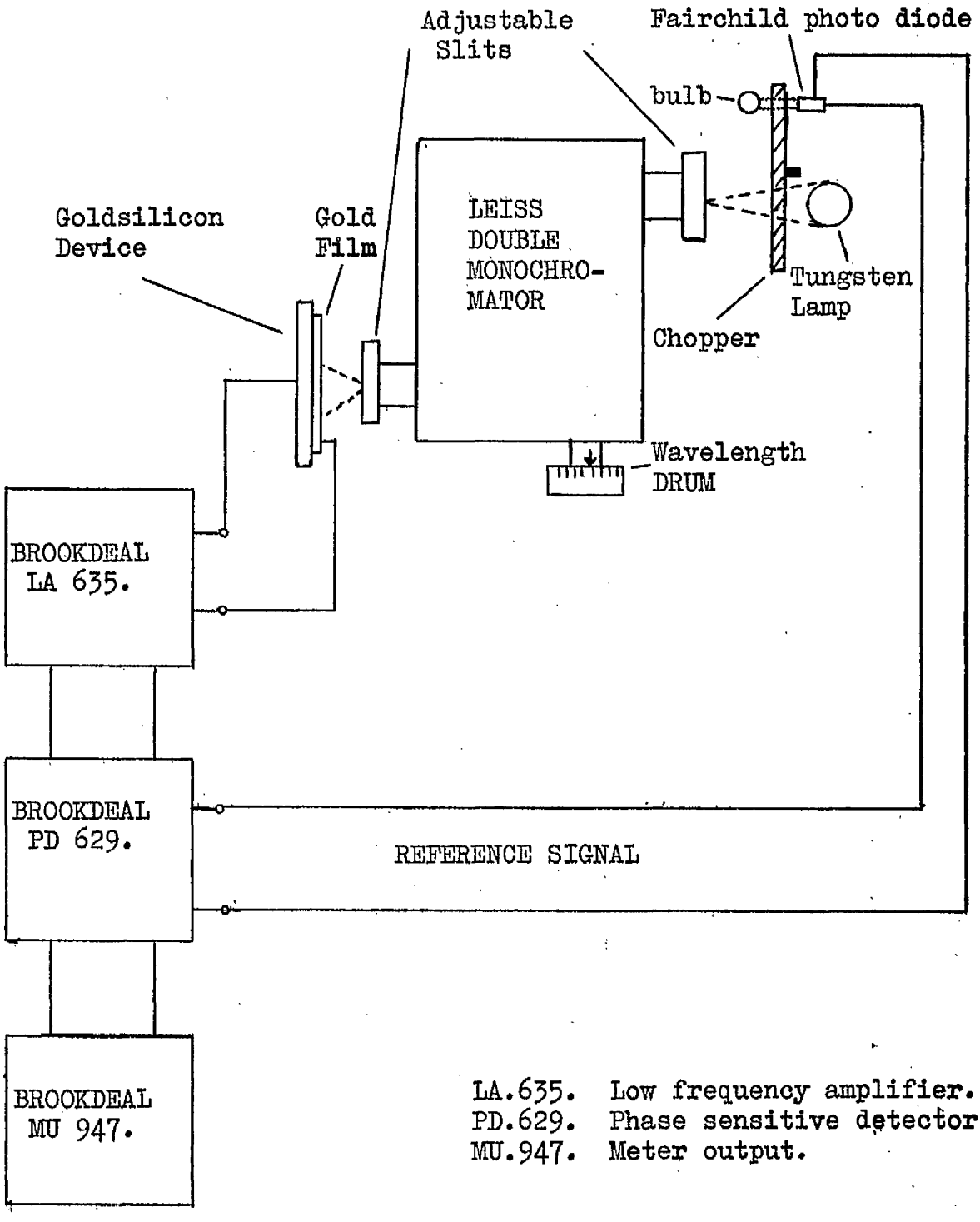


Fig. 8.1. The Absorption in Gold Films as a Function of Thickness and Wavelength.



LA.635. Low frequency amplifier.
PD.629. Phase sensitive detector.
MU.947. Meter output.

Fig. 8.2. Experimental arrangement for barrier height measurement.

Screened cables were used throughout and the device shielded to keep the noise to a minimum. On the most sensitive range 10^{-7} V could be detected across the input which corresponded to a current of 2×10^{-13} A flowing through the device.

The energy incident upon the device was monitored after every set of readings by replacing the gold-silicon junction with a Hilger-Schwartz FT.101 linear thermopile. The thermopile had a SiO_2 window and a response time of 0.01 sec. The d.c. sensitivity was $40 \mu V/\mu W$. The thermopile was connected to the Keithley microvolt-ammeter 150 A, the output of which was fed to a Beckman potentiometric recorder. A chain drive was connected from the recorder directly to the wavelength drum and so a wavelength scan of energy was plotted automatically. An energy-wavelength plot is shown in Fig. 8.3.

The resolution of the monochromator $\delta \lambda'$ is given by:

$$\delta \lambda' = \frac{S_1 + S_2}{\text{linear dispersion at particular wavelength}} \qquad (8.2)$$

For wavelengths greater than 1μ the linear dispersion was constant and so $\delta \lambda'$ depended solely on $S_1 + S_2$, the entrance and exit slit widths respectively. The slit widths could be adjusted to 0.01 mm. For the experiments S_1 and S_2 were set so that there was just sufficient sensitivity of the devices at the long wavelength end of the scan, i.e. at 1.6μ. In general $S_1 = 0.25$ mm and $S_2 = 0.26$ mm, giving $\delta \lambda' = 250$ Å for wavelengths greater than 1.0μ.

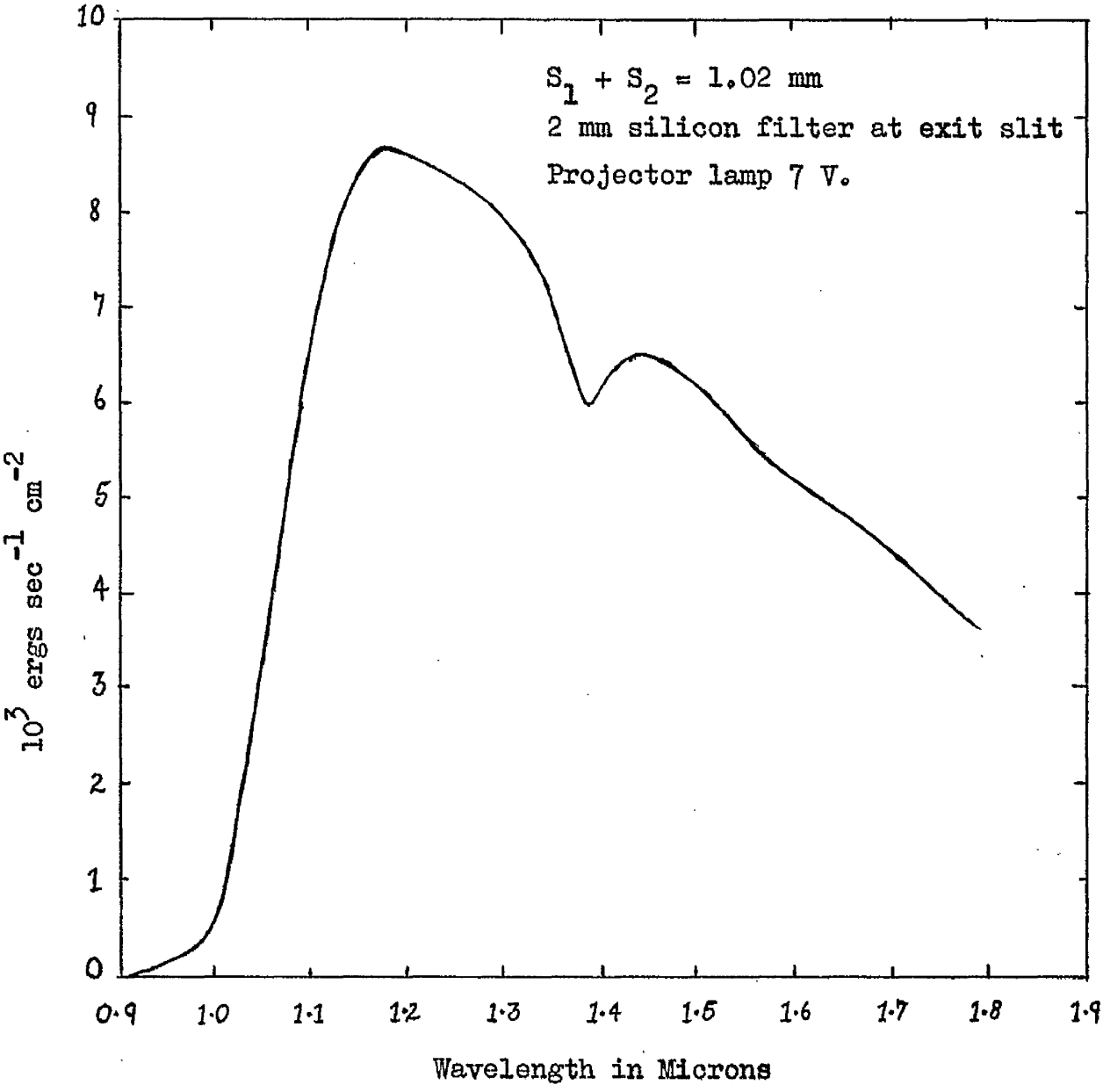


Fig. 8.3. Energy Distribution from Monochromator with Tungsten Source.

In order to check that in fact it was a hot electron effect we were observing the photoresponses of both a diffused high resistivity p-n junction and a gold-silicon junction were determined, Fig. 8.4. A silicon filter was placed over the exit slit of the monochromator to ensure no scattered light reached the diodes. (This was done in all the experiments.)

From Fig. 8.4 it is evident that at photon energies around 0.98 eV the response due to bulk absorption in the silicon (phonon assisted transitions) is comparable with the electron emission current. In order to reduce this effect so that the $Y^{\frac{1}{2}}$ versus $h\nu$ curve would be a straighter line it was decided to attempt measurements at lower temperatures.

8.3 Low temperature measurements

Some slices of 4,000 Ω cm n-type silicon were prepared as usual with alloyed back contacts and etched in a solution of 50 cc HNO_3, 20 cc CH_3COOH and 15 cc HF for seven minutes. After etching, the slices were put in the vacuum chamber and three 8 x 3 mm areas of gold evaporated on each slice. The three areas were of thicknesses 150 Å, 300 Å and 500 Å (all evaporated at 3 Å/sec).

These slices were then mounted on gold plated nickel strip using air drying silver paint and fast setting amine-free epoxy resin. The nickel strip was then soldered to a piece of vero-board, Fig. 8.5.. Contact to the gold areas was made by phosphor bronze suspension wire and a touch of the silver paint. The phosphor bronze wire was

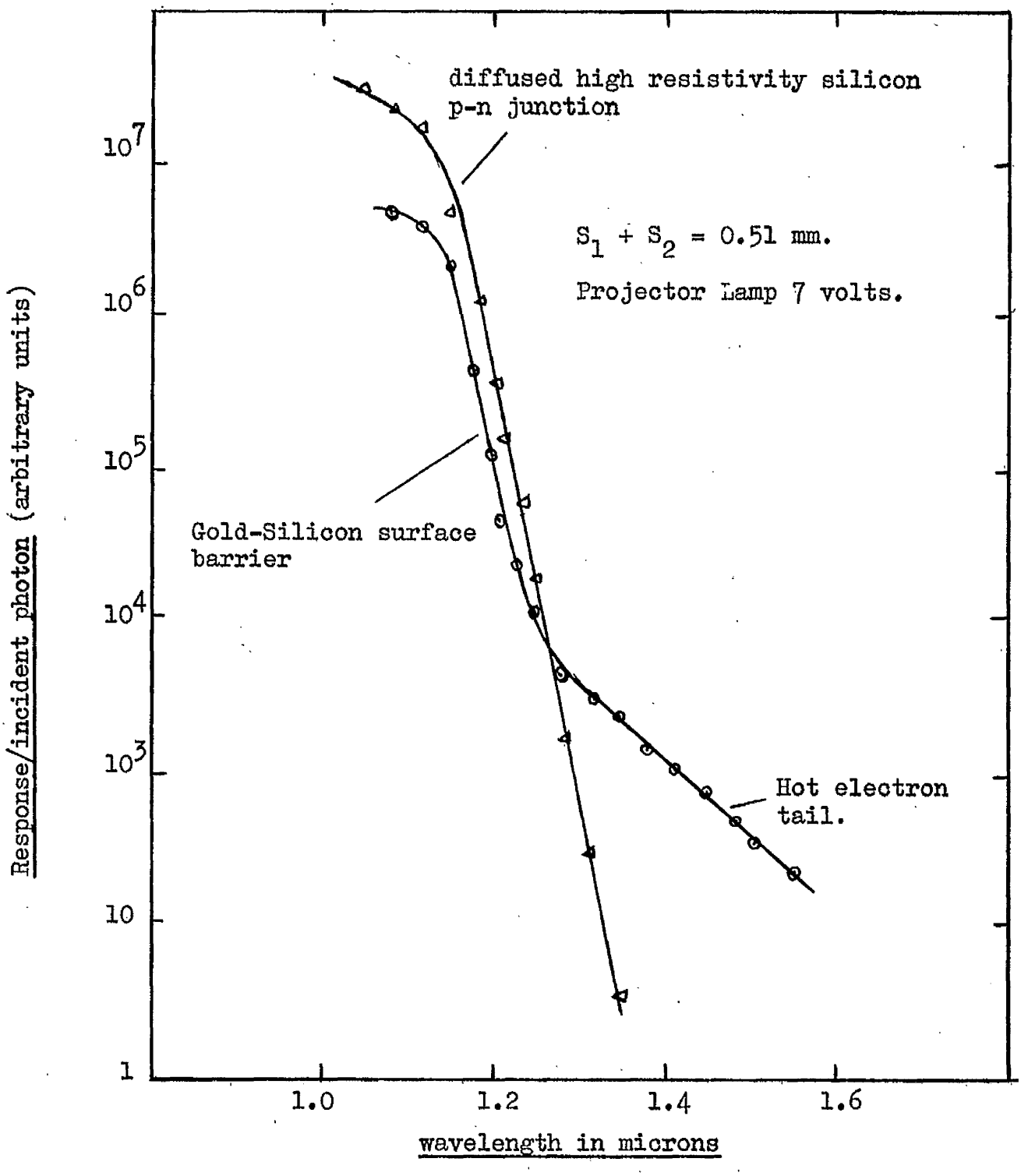


Fig. 8.4. Photoresponse curves of a silicon p-n junction and surface barrier diode at room temperature.

held rigid by a drop of the quick setting epoxy resin. As a result these contacts were robust and could be soldered to the vero-board and later unsoldered from it without disturbing the gold film. The board with specimen then slotted into an end connector which was the lid of an expanded polystyrene box coated with aluminium foil (Fig. 8.5). A recess was made in the polystyrene and a piece of microscope slide fitted in this recess which allowed light to fall on any selected gold area. This face of the box fitted flush up to the exit slit of the monochromator. A hole was made through the bottom of the polystyrene box which allowed a copper tube to pass into it. The whole assembly was then fitted on a set of micromanipulators and brought up to the exit slit.

A spiral of copper tubing which acted as a heat exchanger was attached to the polystyrene box via rubber tubing and placed in a vacuum jar of liquid nitrogen. Nitrogen gas was passed through the heat exchanger and into the cryostat. The rate of flow of gas and the level of liquid nitrogen in the dewar both controlled the temperature of the specimen, which was monitored by an iron-constantan thermocouple alongside the specimen. The above design was based on an idea of A. Brünnschweiler[9] . The operating temperature was around 140^{o}K. The glass window did not frost up if it was coated with a thin layer of Teepol before the experiment, thereby dispensing with elaborate de-misting techniques.

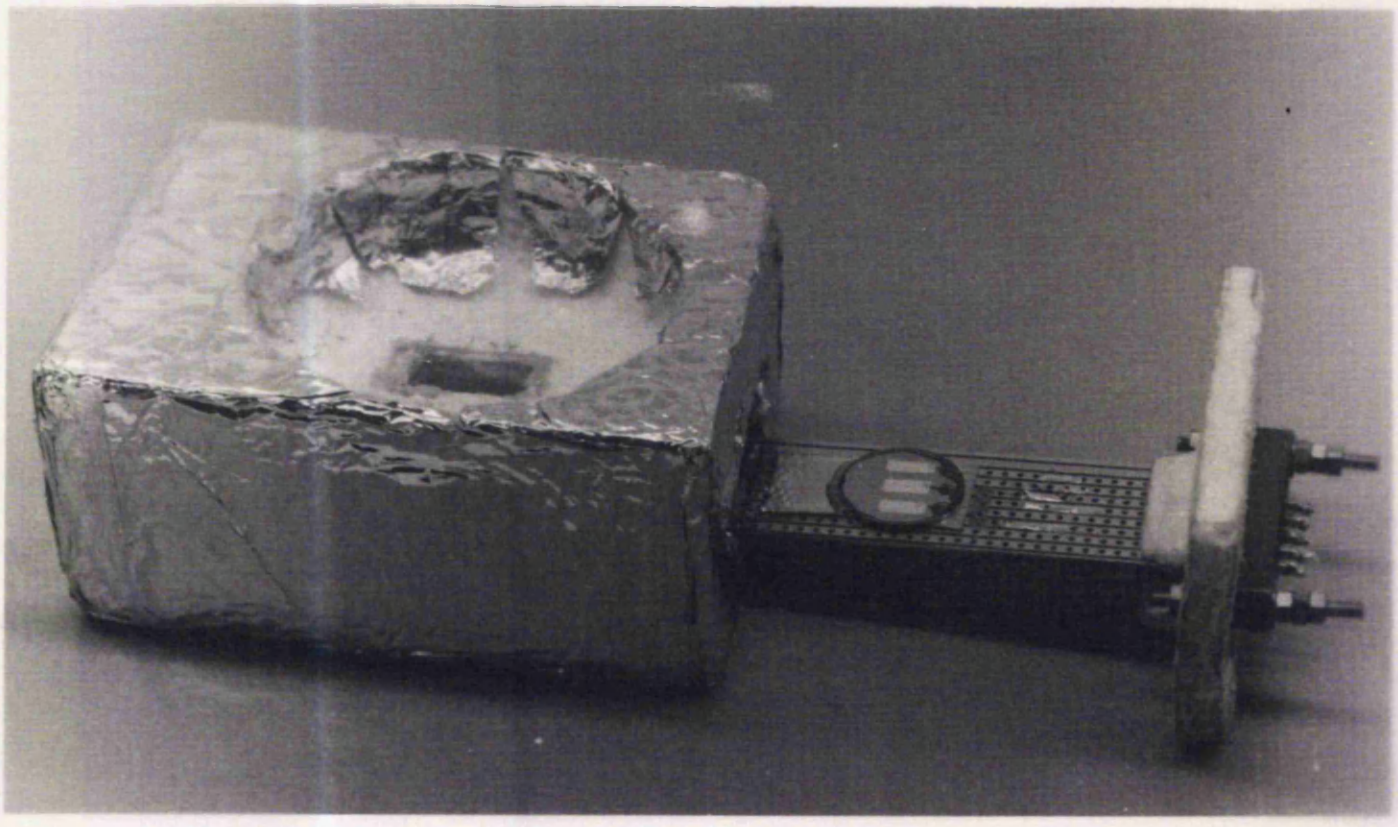


Fig. 8.5 Low temperature jig.

8.4 Experimental procedure

The specimens were mounted as above and sets of readings of photocurrent versus wavelength taken at room temperature for the various film thicknesses. It was important to ensure that the response was due to the light being incident on the film proper and not the edge of the film. This was achieved by scanning the specimen across the exit slit by means of the manipulators and observing that the signal would increase to a maximum, decrease to a minimum, and increase back to a maximum as the light fell on one edge of the film, the film proper and then the other edge of the film. Readings were taken at the minimum position.

Ideally one would like to measure the short circuit photocurrent but in practice one measures a photovoltage, V_{Ph}. So long as V_{Ph} is less than about 10^{-3} V this does not affect the readings. (See Appendix B.) However, at lower temperatures the dynamic resistance of the diode at the operating point changes considerably (typically 200 KΩ at 300°K to 10 MΩ at 140°K) and this has a profound effect on the measured value of V_{Ph}. This change in resistance has been corrected for in the results that follow in order that $Y^{\frac{1}{2}}$ can be plotted on the same arbitrary scale for the two temperatures. A full explanation is given in Appendix B. As a result it was necessary to measure the current-voltage characteristics at both temperatures besides the photoresponses.

Measurements were made as soon as the devices were fabricated (or within one day if possible), one week or so later and then before and after annealing the devices at 100°C for about half an hour as described previously for the gold films.

8.5 Results

Typical $Y^{\frac{1}{2}}$ versus $h\nu$ curves are shown in Figs. 8.6, 8.7 and 8.8 for 150 Å, 300 Å and 500 Å thick gold films respectively. Only one set of room temperature data is plotted on each graph because the low temperature plots give better lines. The value of $h\nu_o$ at room temperature is readily obtained from these graphs as follows. The Fermi level at the metal-semiconductor interface is pinned in relation to the valence band edge[10] and so the change in the value of the band gap energy for silicon over the temperature range of interest has merely to be subtracted from the value of $h\nu_o$ obtained at the low temperature. The change in Eg from 300°K - 140°K is 0.034 eV. There is also a correction to be made for the image force lowering of the barrier (section 2.2.1.), $\Delta \phi_{MS}$. From equations (2.2) and (3.1) this is given by:

$$\Delta \phi_{MS} = \left[\frac{e^7 N_D (V_A + V_D)}{8\pi^2 \epsilon_o^3 \epsilon_d^2 \epsilon} \right]^{1/4} \qquad (8.3)$$

where ϵ_d is the image force dielectric constant (for silicon ϵ_d = 12[11]).

For the above specimens at zero bias $\Delta \phi_{MS} = 1.48 \times 10^{-3}$ eV and so this has to be added to the experimental values. The results from the typical plots shown in Figs. 8.6, 8.7 and 8.8 are summarised in Table 8.1.

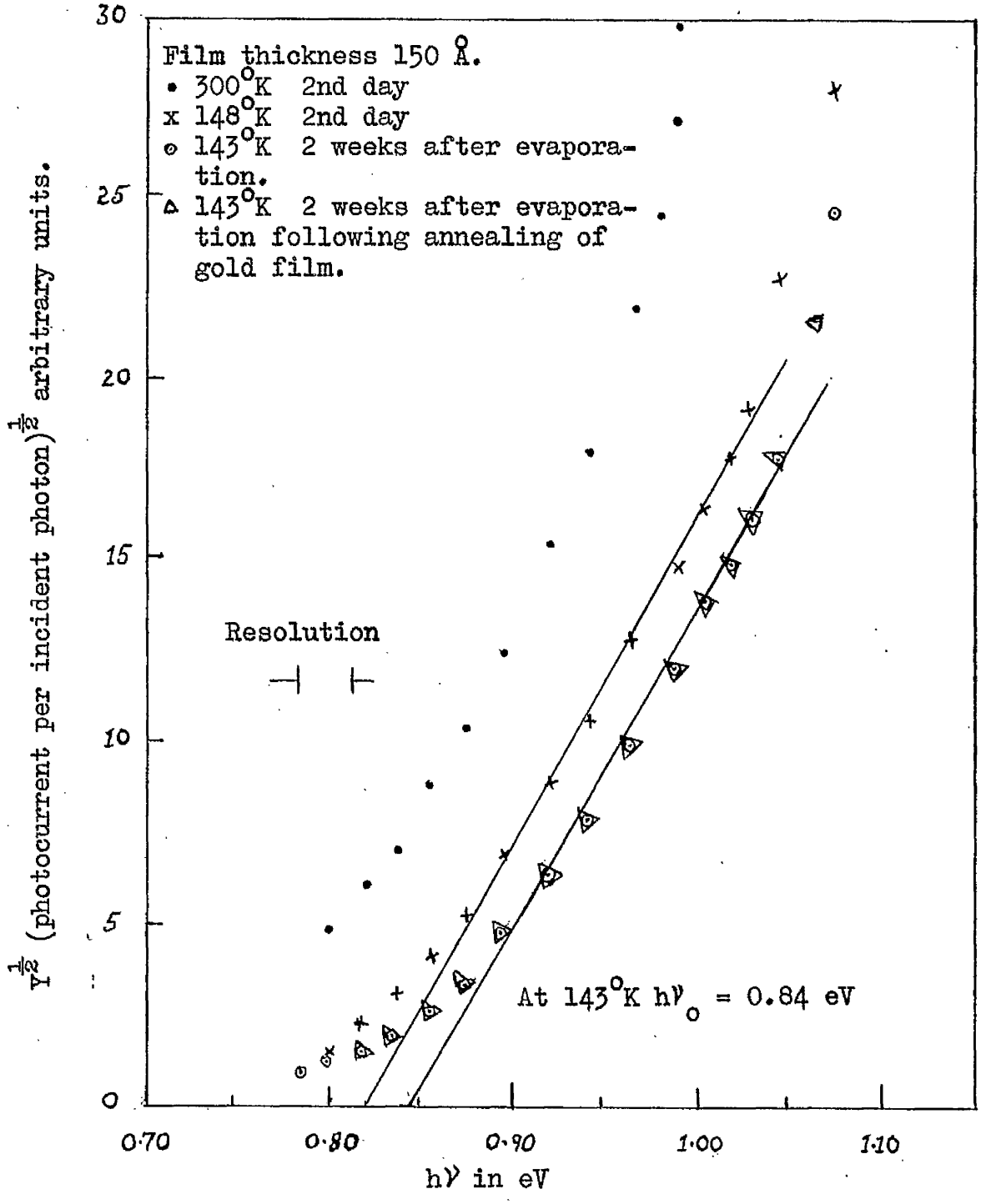


Fig. 8.6. Threshold plot for 150 Å gold film on silicon.

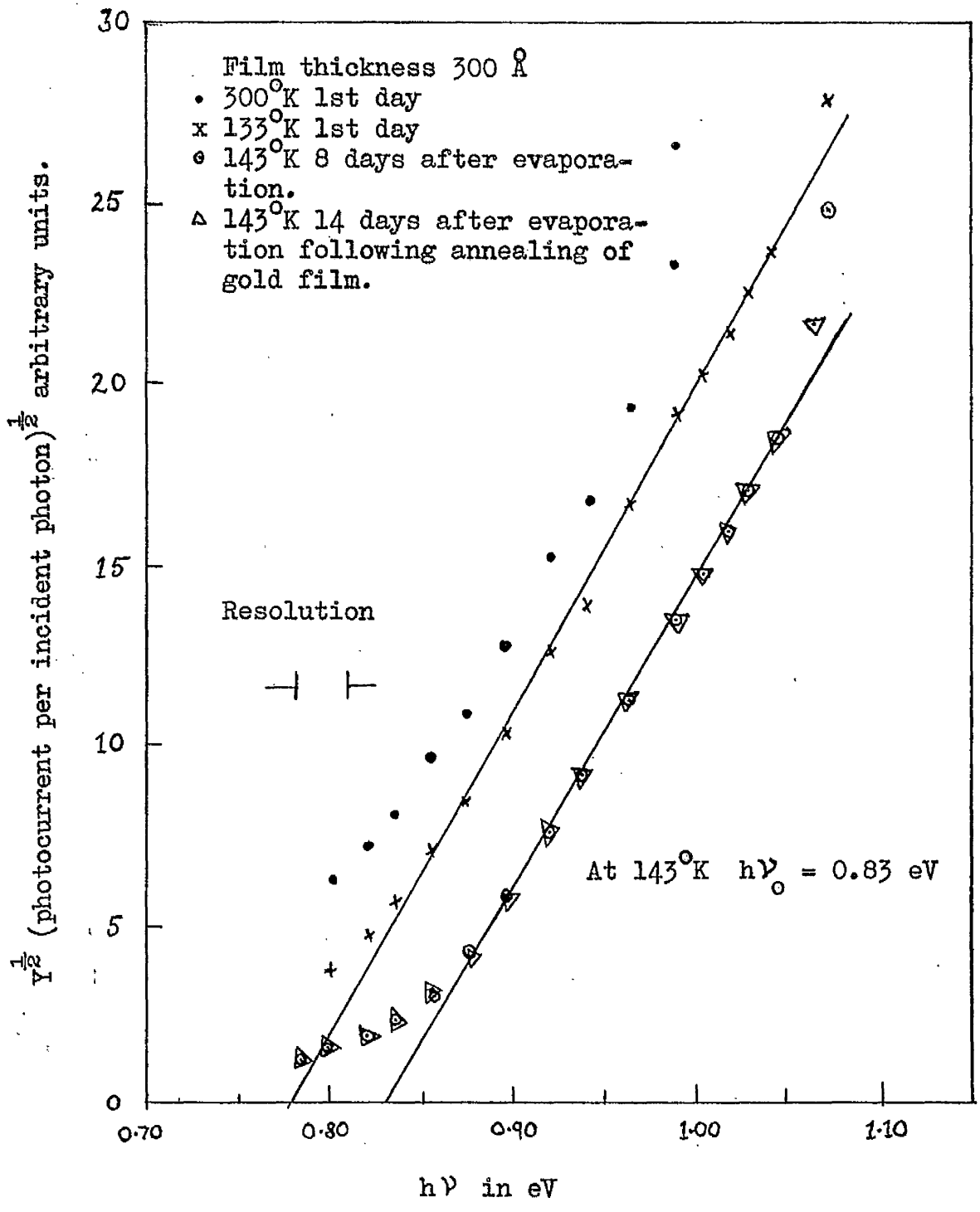


Fig. 8.7. Threshold plot for 300 Å gold film on silicon.

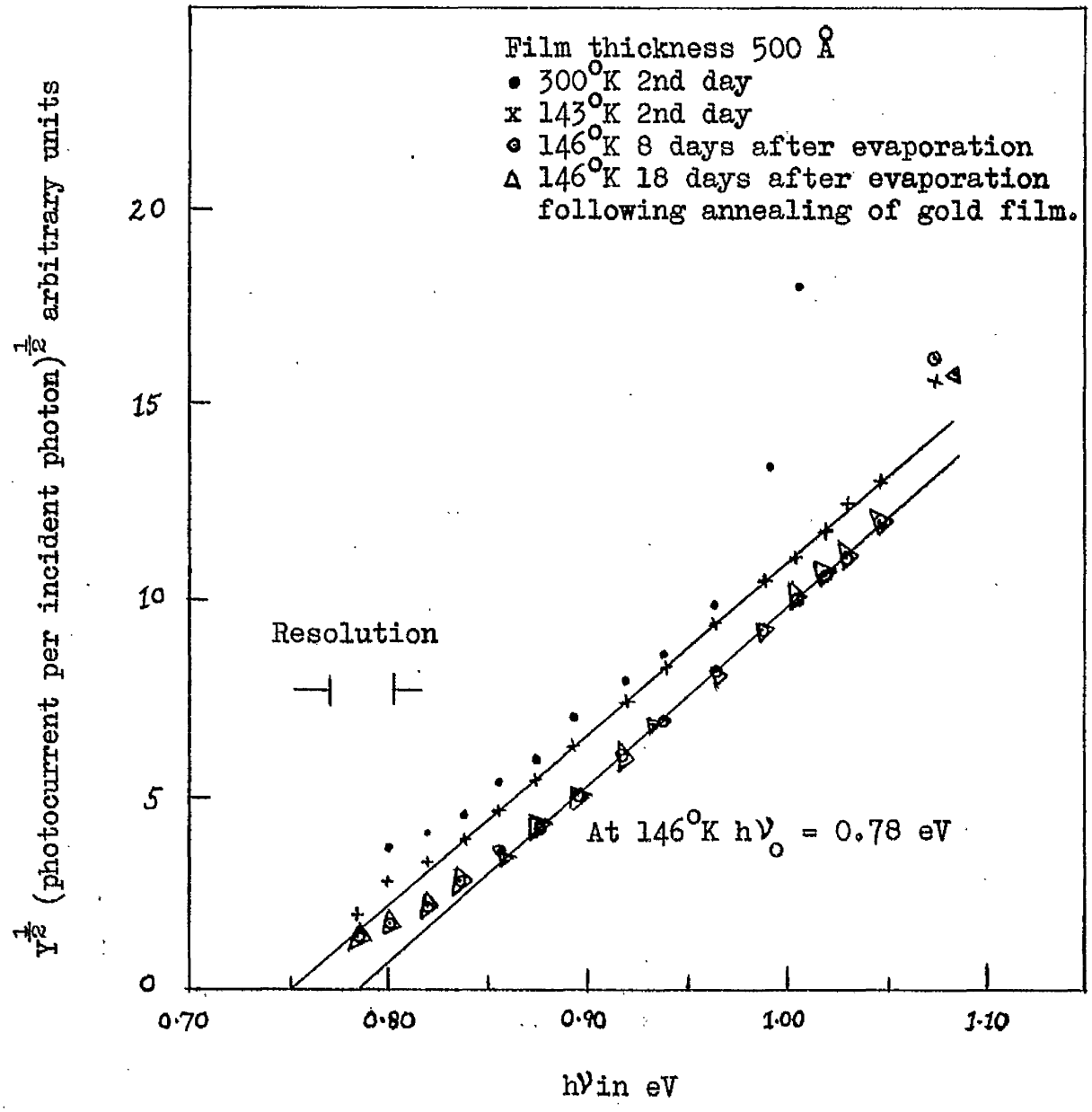


Fig. 8.8. Threshold plot for 500 Å gold film on silicon

Film Thickness	Barrier Height ϕ_{MS} at Room Temperature. In eV.		
	1st day 2nd day	Before and after annealing film 2 weeks later.	Average of final values
150 Å	0.79	0.81 ± 0.01	
300 Å	0.75	0.80 ± 0.01	0.79 ± 0.01
500 Å	0.72	0.75 ± 0.01	

Table 8.1

8.6 Discussion

The average values of ϕ_{MS} derived from the photo-threshold plots for gold-silicon barriers agree very favourably with those obtained by Turner[3] [0.79 ± 0.02 eV] for gold on low resistivity silicon using capacity measurements. Two points arise when comparing the capacity method with the optical threshold plots. First, for freshly evaporated metal films deposited on chemically prepared surfaces, capacity plots could not be satisfactorily obtained until the specimen had "aged" - this ageing can be accelerated by gently annealing the specimen for half an hour at 100°C. Consequently the magnitude of the barrier change with time cannot be ascertained. The optical measurements could be made immediately following the deposition of the metal and it was

found that the barrier height changed by about 0.05 eV during the first week - little change taking place after this period. Secondly, there is a scatter of the values of ϕ_{MS} for the different film thicknesses on each slice of silicon which is outside the experimental error - this has been a feature of threshold plots by other workers[6,8]. Capacity plots showed ϕ_{MS} to be independent of film thickness.

From Figs. 8.6, 8.7 and 8.8 it can be seen that there is a decrease in the relative response of the gold-silicon diodes at the low temperature compared with the response at room temperature. The reason for this reduction is partly because the barrier threshold energy has increased and partly because the solid angle of collection of electrons scattered by phonons is reduced at the lower temperature. On the other hand the electron-phonon mean free path increases at the low temperature and so the hot electron attenuation length should increase resulting in a larger yield of photo electrons (Appendix A). However, we have seen in Chapter 7 that the predominant scattering mechanism is imperfection scattering, thus the increase in yield due to the reduction in temperature will be negligible. It is interesting to note that the tail of the $Y^{\frac{1}{2}}$ versus $h\nu$ curves (i.e. the yield near the threshold energy where the abridged Fowler analysis is not valid) is larger for the low temperature plots than for the room temperature curves. One would anticipate the opposite to be the case.

At room temperature the threshold plots were not as good as expected and the yield increased rapidly at lower values of $h\nu$ than

for films deposited in ion pump systems[5,6,8]. This may be attributed to a much reduced hot electron current arising from a short electron attenuation length. Hence the contribution to the total current from absorption in the silicon becomes dominant at smaller values of $h\nu$. The resistivity measurements and the failure of Turner[3] to observe hot electron effects in semiconductor-metal-semiconductor devices support the view that the electrons in our films possess a much shorter mean free path than that measured by other workers.

Finally we should note that there were no observable effects on the barrier height measurement following annealing of the specimens although we know structural changes take place in the gold films during the annealing process.

References to Chapter 8

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Chapter 9

Surface Barrier Detectors with Alloyed Back Contacts

9.1 Introduction

The basic requirements of surface barrier detectors and some manufacturing techniques have been described in Chapter 3. Although evaporated aluminium back contacts are notoriously unreliable and non-reproducible it has been demonstrated in Chapter 5 how reproducible, long lasting, evaporated aluminium contacts can be obtained when the silicon surface is suitably prepared. The resolution and behaviour of nuclear detectors fabricated using aluminium back contacts, some of which deteriorated with time, have been documented elsewhere[1]. There is no reason to suppose that detectors fabricated using the oxide removal technique (Chapter 5) would not behave satisfactorily since evaporated gold forms a good rectifying contact when the silicon surface is prepared in this way.

The evaporated aluminium contact has many advantages (low resistance and non-injecting when the detector is fully depleted) and it would be advantageous if a method of forming a similar contact could be adopted which is 100% reproducible.* I have made preliminary investigations into an alloyed back device in which I have endeavoured to keep the alloyed region very thin. If the gold-silicon alloy region

* Recently Owen[2] has adopted a phosphorus diffusion technique.

is very thin there is reason to believe that the strain introduced due to the lattice mismatch will be very much reduced. Consequently the noise associated with the contact will also be very much reduced. The technique aimed at producing a device with such a contact is described below and does not entail masking the slice with wax or varnish at any stage in the process.

9.2 Experimental procedure

Both sides of 4,000 ohm cm n-type silicon slices, about 1 mm thick, were lapped and then etched in a mixture consisting of 50 cc HNO_3, 20 cc CH_3COOH and 15 cc HF as described in section 4.4.2. After washing the slice thoroughly in deionised water it was blown dry in a nitrogen ambient and immediately transferred to the evaporator where it was placed in a clean outgassed molybdenum heater fitted with a lid and which had a 3/8" diameter hole machined in its base. A chromel-alumel thermocouple was attached to the heater and the system evacuated to its operating pressure (4×10^{-6} torr). The heater and silicon slice were held at a temperature of 410°C, just above the gold-silicon eutectic (370°C) and a 200 - 300 Å thick layer of gold-antimony deposited at about 10 Å sec^{-1} on the hot silicon. The temperature of the molybdenum heater was then decreased slowly through the gold-silicon eutectic and eventually reduced to room temperature. Upon removal from the chamber the silicon slice was mounted in pyrophyllite rings using the techniques described previously (section 3.6.3 and in more detail in reference (1)) excepting that quick setting epoxy resin was used throughout the encapsulation process. A 300 Å layer of gold was then deposited on the front face

at 3 Å sec^{-1}. Contact to the alloyed region was also made by an evaporated metal film. Typical detectors are shown in Fig. 9.1.

9.3 Current-voltage characteristic

I-V measurements were made with the detectors in situ immediately following the gold deposition and changes noted when different ambients were admitted to the coating unit. The admission of oxygen to the system produced a reduction in the value of the reverse current but these changes have never been of the magnitude reported by others[3,4]. The admittance of nitrogen had no effect on the characteristics. However, once nitrogen had been admitted to the system re-pumping was necessary in order to effect an immediate change upon re-exposure of the diode to oxygen.

A typical I-V characteristic for a device fabricated as above is shown in Fig. 9.2. (Note that there is a change in scale on both the current and the voltage axes.) Fig. 9.3 shows the change in the device characteristic when oxygen was admitted to the system immediately following the gold deposition. These changes were reversible - the initial characteristic being obtained if the system was immediately re-evacuated. In fact one diode was left at roughing pressure for two days after which the changes could still be reproduced. However, once the diode was exposed to the atmosphere for about one day no further reversible changes took place. The forward characteristics were unaffected.

9.4 Noise measurements

Unfortunately we have not been able to make a proper assessment of our diodes as nuclear detectors because we do not possess a

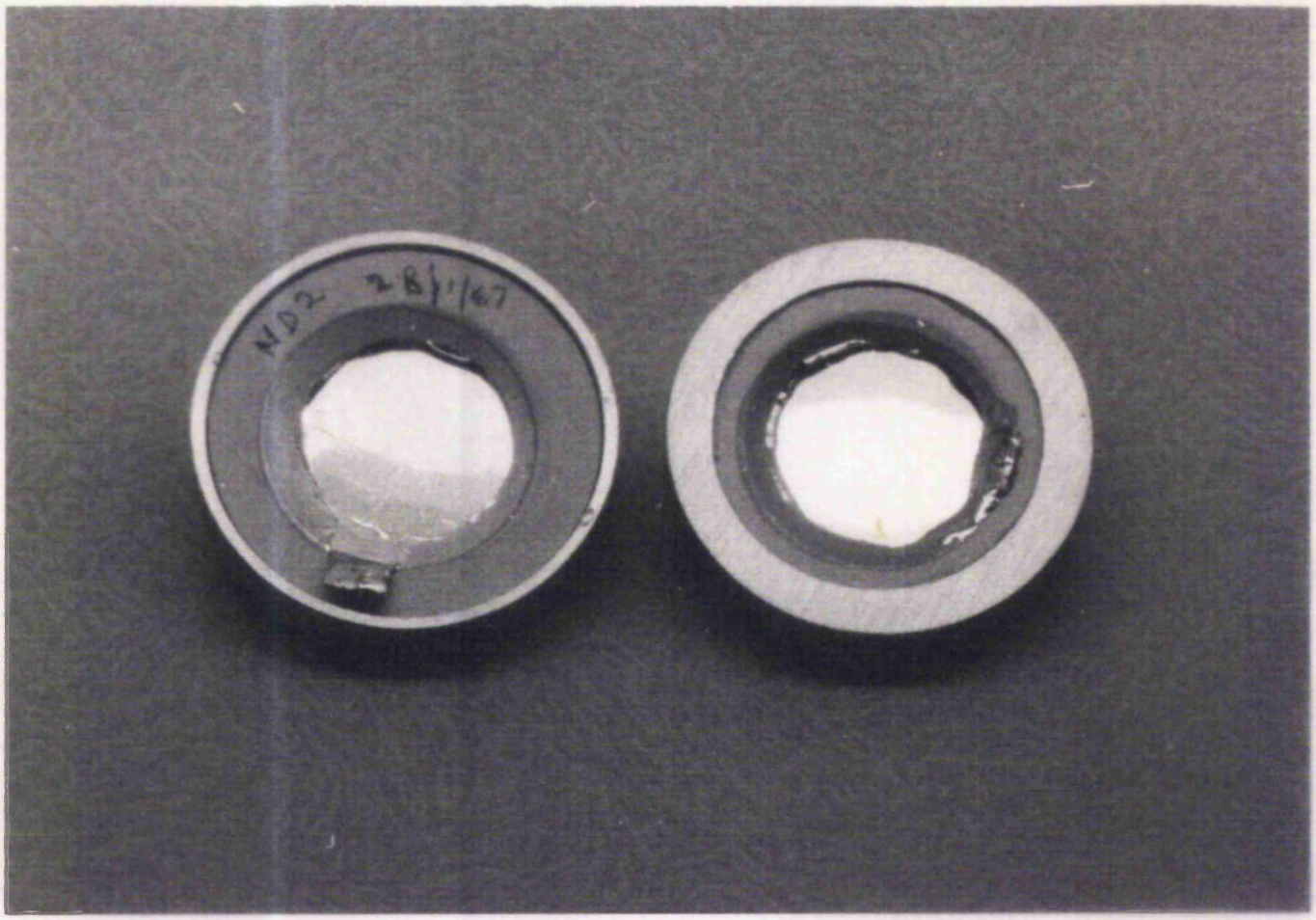

Fig. 9.1 Illustrating detector mounting.

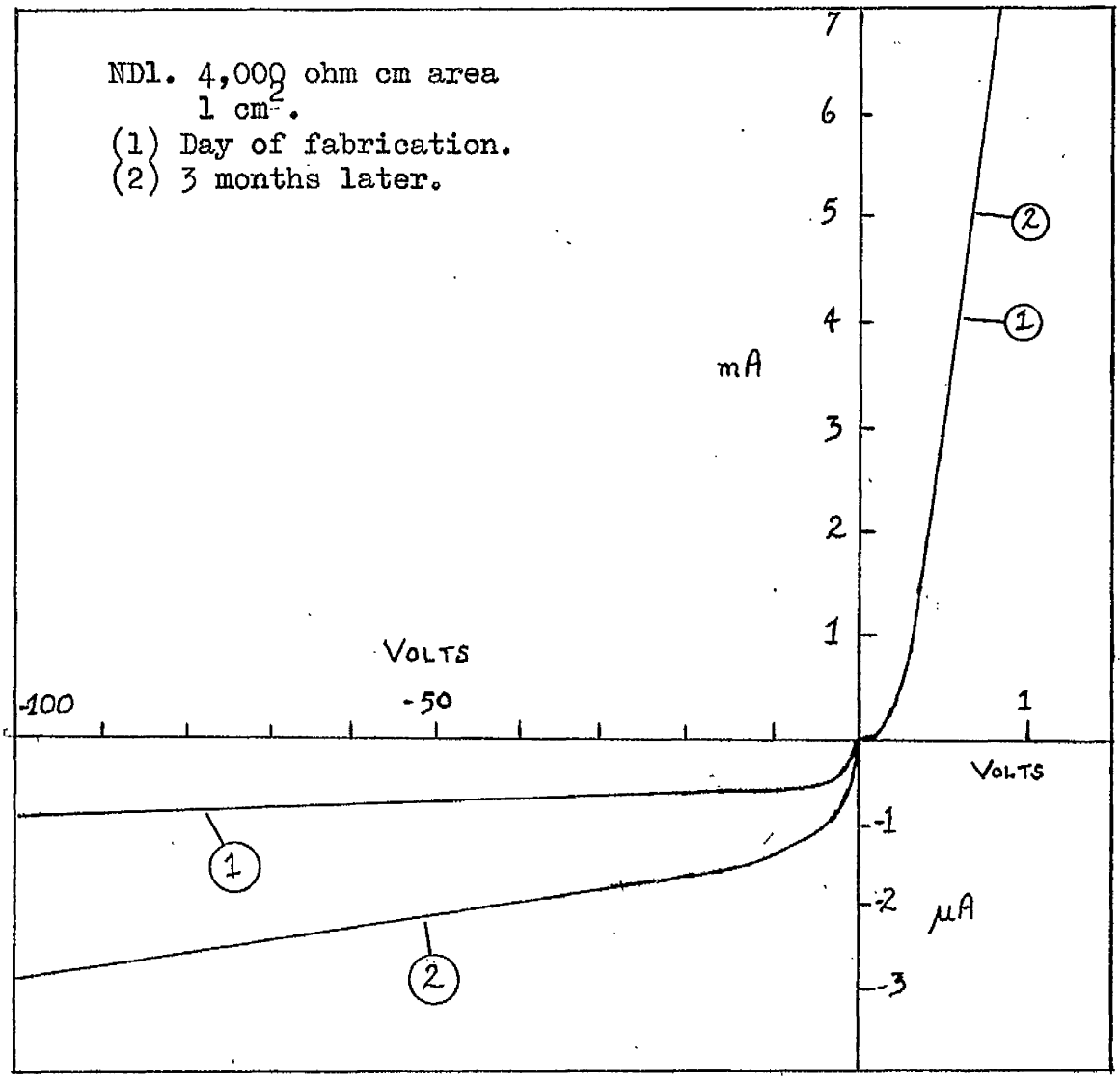

Fig. 9.2. Typical diode characteristic.

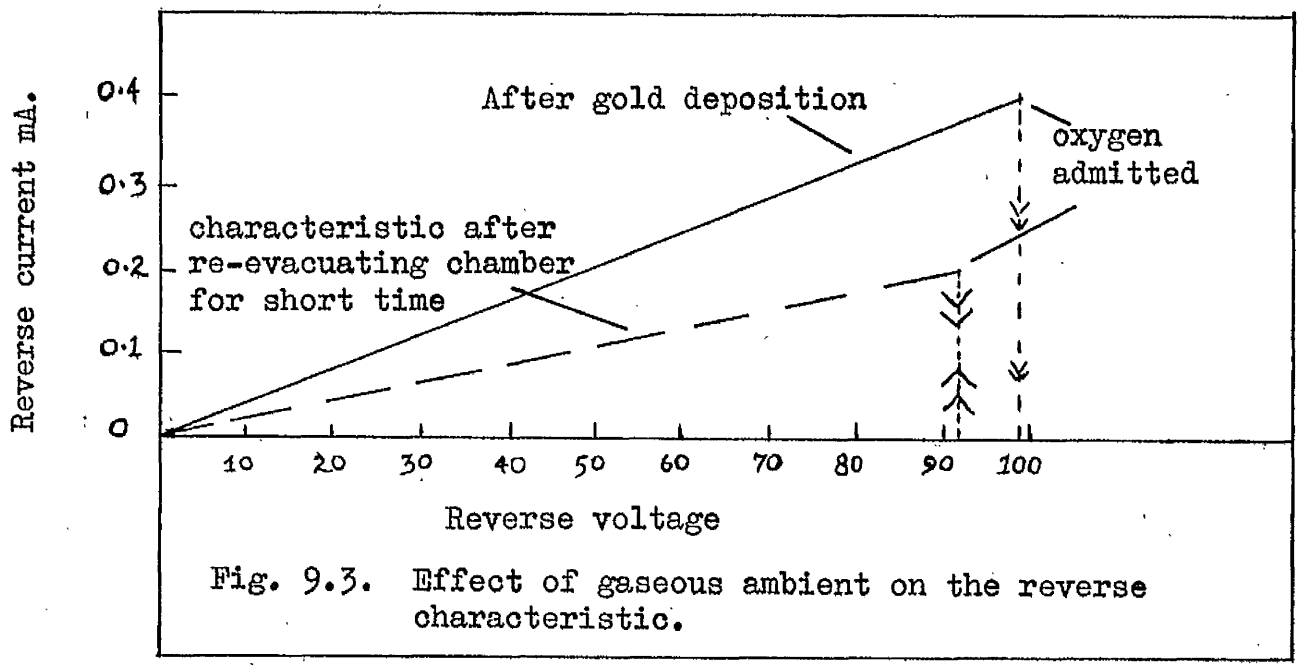

Fig. 9.3. Effect of gaseous ambient on the reverse characteristic.

suitable radioactive source. An evaluation of the noise of the detectors was made as follows. A test signal was fed to a charge sensitive pre-amplifier and the output signal fed via a pulse amplifier (U.K.A.E.A. Type 1430 A) to a pulse height analyser (U.K.A.E.A. Type 1363 D). The magnitude of the test pulse was chosen such that the charge on the standard condenser corresponded to that which a 6 MeV particle would liberate in a silicon detector if the charge collection efficiency was 100%. A diode was then connected across the input of the pre-amplifier and the spread in the pulse height spectrum recorded as a function of reverse bias. A typical spread is shown in Fig. 9.4. The F.W.H.M. spread at 100 V is about 84 KeV.

9.5 Discussion

The preliminary investigation seems to indicate that an alloyed back device may well prove a practical proposition for ordinary alpha particle detection where large depletion regions are not required. It would be advantageous to manufacture some thinner diodes in order to assess their performance when fully depleted - although they may well prove too noisy for stacking in arrays.

The decrease in reverse current of the diodes upon exposure to the atmosphere may be attributed to adsorbed oxygen producing changes in surface potential and surface recombination velocity around the edge of the silicon. Only very small changes have been observed in the forward characteristic when devices were exposed to the atmosphere which seems to indicate that a barrier is formed immediately the gold is deposited.

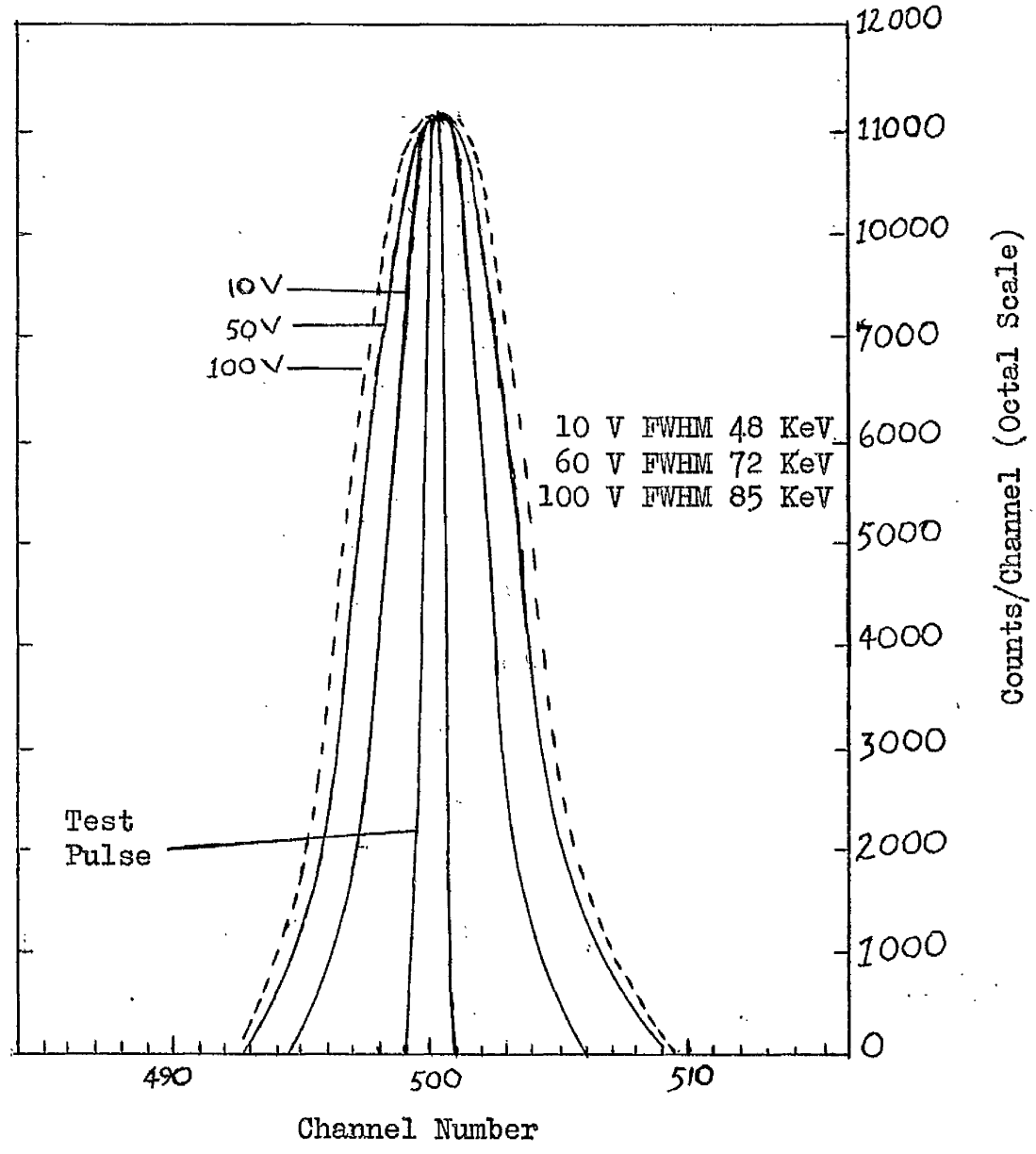

Fig. 9.4. Pulse height spread of test pulse due to diode noise.

Hence, the reverse current is first of all dominated by excess current mechanisms until oxygen stabilises the surface. This view is supported by the observation that the changes in reverse current are initially reversible. (It is worth noting that experiments have also been carried out on thermal oxide protected devices with windows etched through the oxide for the formation of the ohmic contact and the surface barrier. In all cases only very small changes in the reverse current were observed when such devices were subjected to an oxygen environment immediately following the gold deposition. This again supports the view that the environmental changes are due to surface effects around the edge of the slices and not due to barrier height changes at the gold-silicon interface arising from the diffusion of oxygen atoms through the metal film.)

The value of reverse current obtained for the gold-silicon diodes was slightly greater than that predicted in section 3.4. We conclude that the predominant source of reverse current was due to an excess current mechanism, which was almost certain to have been introduced during the heating stage of the detector fabrication. Aluminium back contact detectors have reverse currents slightly less than the alloyed devices.

References to Chapter 9

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Chapter 10

Conclusions

The behaviour of evaporated aluminium-silicon contacts depends primarily on the surface treatment of the silicon prior to the deposition process. Oxide removal techniques which tend to leave the silicon surface n-type favour the formation of an ohmic contact, whereas surface treatments which leave the surface slightly inverted favour the formation of rectifying contacts. The introduction of the aluminium does not seem to have a great deal of influence regarding the magnitude of the barrier formed. There is definite evidence that an interfacial layer exists at the aluminium-silicon junction but the part this plays in the ageing of the current-voltage characteristic is not at all clear. The ageing of metal-semiconductor contacts can be explained by ionic drift processes within the interfacial layer which ultimately affect the surface state density* but in the case of aluminium on silicon it is difficult to see why this may be a relatively fast or slow process depending on the surface treatment of the silicon. Moreover the magnitude of the barrier height change must be quite substantial to account for the large changes observed in the I-V characteristics. The electron microscope studies have shown that the aluminium film is decidedly metallic and crystalline despite previous conjectures to the contrary, although we have

* M. J. Turner, Ph.D. Thesis, U.M.I.S.T., Dec. 1966.

obtained no information at all regarding the size or composition of the aluminium-silicon interfacial layer.

It was shown that the type of film which is formed when gold is evaporated on etched silicon depends on several factors. For the experiments described gold was deposited such that well oriented, hole-free films were grown and there is good reason to believe that the gold is in intimate contact with the silicon. However, when the silicon surface is coated with an oxide layer, which is the type of surface generated by some workers during the manufacture of their surface-barrier detectors, the structure of the gold does not seem to be influenced by the substrate. It is not surprising, therefore, that the evaporated metal does not control the magnitude of the surface barrier when detectors are fabricated using the oxide inversion technique.

The highly oriented gold films deposited on chemically etched silicon possess a resistivity greater than the bulk value. Once the gold films are annealed they fit the Fuchs-Sondheimer equation fairly well provided the films are continuous (i.e. their thickness is greater than 100 Å). However, the primary scattering mechanism appears to be imperfection scattering (l_i = 300 Å) and this is readily attributed to gas or impurities from the vacuum being trapped in the films and many imperfections being locked in the films due to the condensation process taking place on a cold substrate. An investigation of both the film structure and the resistivity-thickness relationship of gold deposited on etched silicon held at elevated temperatures could prove that well-ordered gold-films can be achieved on silicon substrates. The low

yield of photo-excited carriers across the gold-silicon junction seems to support the view that the films possess a high imperfection density compared with films deposited by other workers in ion pump systems.

The photo-threshold plots indicate that the magnitude of the metal-semiconductor barrier is 0.79 $\pm$ 0.01 eV for gold evaporated on chemically prepared silicon. The change in barrier height with time was about 0.05 eV over a period of one week and no changes were observed when the samples were annealed.

A preliminary investigation of the alloyed back radiation detector showed that the pulse height spread due to diode noise was equivalent to less than 90 KeV FWHM at 100 V. The initial large reverse current of the diodes was interpreted in terms of excess currents but once the device was stabilised by an oxygen ambient the reverse current was only slightly larger than that predicted by metal-semiconductor junction theory for ϕ_{MS} = 0.79 eV. However, if the alloyed back detector is to be considered as a practical proposition a more intense investigation is recommended.

Appendix A

Hot Electrons in Thin Metal Films

When a photon flux is incident at a metal-semiconductor junction the collection of hot electrons is analogous to photoemission from a metal into a vacuum. On the basis of the conventional Fowler analysis[1] the photoresponse, Y, is proportional to $h^2(\nu - \nu_o)^2$, provided $E_F \gg h(\nu - \nu_o) \gg kT$. The basic ideas involved in arriving at this result are twofold. First, that the electrons within the metal obey Fermi-Dirac statistics and secondly that the number of electrons emitted from the metal surface per absorbed photon of energy $h\nu$, is proportional to the number of electrons per unit volume within the metal which have a velocity component u, normal to the surface, greater than the critical value u_o, such that

$$\tfrac{1}{2} m u_o^2 + h\nu = \phi_B$$

where ϕ_B is the barrier energy measured from the bottom of the conduction band.

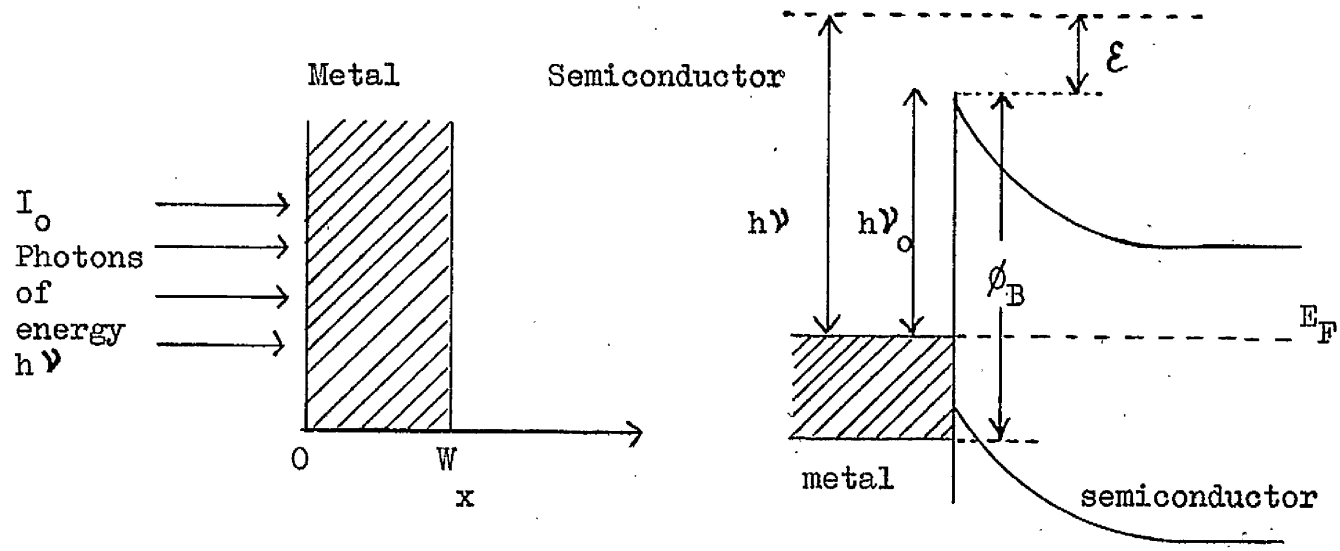
The above analysis does not take into account the origin of the photocarriers or scattering processes within the metal.

Free electrons do not completely absorb photons without a third agency being involved. In fact photo-electrons can be generated

(1) R. H. Fowler. Phys. Rev., 38, p. 45 (1931).

either at the surface of a metal where the surface itself acts as a source or sink of momenta, or in the bulk of the metal (volume photoelectric effect) where phonon interaction takes place. Provided the electrons can reach the surface without undergoing collision processes then the Fowler relationship still holds.

In the case of the metal-semiconductor junction there is a distinct possibility of the excited electrons undergoing electron-electron, electron-phonon or electron-imperfection scattering processes before reaching the semiconductor where they are collected. The transport of hot electrons produced by photoexcitation in metals has been discussed elsewhere[2,3]. It is convenient to define the range, L(E), of hot electrons with energy E relative to the Fermi level, as the electron attenuation length which characterises the scattering processes involved in the metal film at that energy.



(2) C. N. Berglund and W. E. Spicer. Phys. Rev., 136, 4A, p. A1030 (1964)
(3) R. Stuart, F. Wooten and W. E. Spicer. Phys. Rev., 135, A495 (1964)

Consider the case illustrated above in which monochromatic radiation of frequency ν and intensity I_o is incident upon a metal-semiconductor junction the thickness of the film being W and for which the photon absorption coefficient of the film, α, is energy independent. If multiple reflections in the film are neglected then the photocurrent per absorbed photon Y is given by:

$$Y = \frac{B\int_0^{h(\nu - \nu_o)}\int_0^W I_o\alpha \exp.(-\alpha x)\exp\left[-(W - x)/L\right].dx.\mathcal{E}d\mathcal{E}.}{\int_0^W I_o\alpha\exp.(-\alpha x)dx.}$$

$$= \frac{B'\alpha}{1-\exp.(-\alpha W)}\int_0^{h(\nu - \nu_o)} \frac{\exp.(-W/L) - \exp.(-\alpha W)}{(\alpha - 1/L)}\,\mathcal{E}\,d\mathcal{E}$$

provided $\phi_B \gg h(\nu - \nu_o) \gg kT$ where B and B' are constants and $\mathcal{E}$ is the energy of the state into which an electron is excited measured from the top of the potential barrier.

If L is relatively energy independent in the region $h(\nu - \nu_o)$ then the above equation reduces to:

$$Y \sim \frac{\alpha}{\alpha - \frac{1}{L}}\left[\frac{\exp.(-W/L) - \exp.(-\alpha W)}{1 - \exp.(-\alpha W)}\right]\left[h(\nu - \nu_o)\right]^2.$$

For gold films $\frac{1}{\alpha} = 120$ Å and $L \approx 350$ Å for $h\nu = 0.95$ eV[4], therefore $\alpha L > 1$ and if $\alpha W > 1$, then

(4) R. W. Soshea and R. C. Lucas. Phys. Rev., 138, 4A, A1182 (1965).

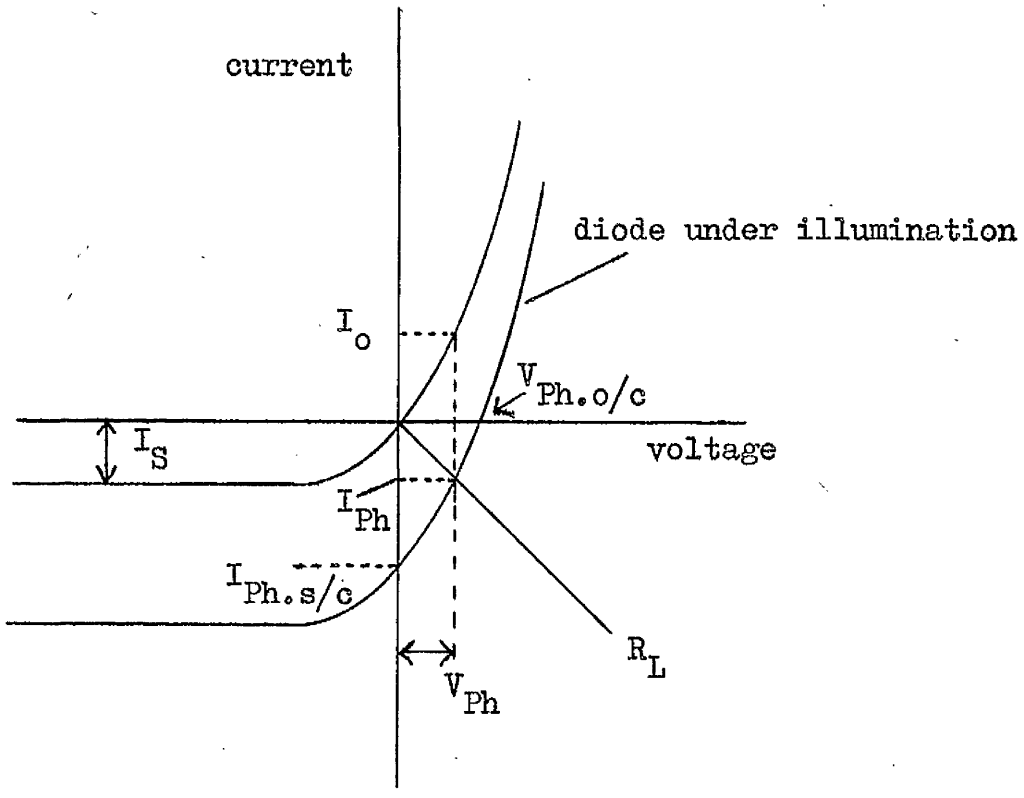
$$Y \sim e^{-W/L} \left[h(\nu - \nu_o) \right]^2$$

These electrons which cross from the metal into the semiconductor are the ones whose trajectories are within a few degrees of the perpendicular to the metal-semiconductor interface.

Appendix B

The Effect of Temperature on the Threshold Plot

First of all we must consider the photoemission current in relation to the photovoltaic effect. Ideally one would like to measure the short circuit photocurrent but in practice one masures a photovoltage developed across a load resistor. Secondly we must see how the magnitude of the photovoltage is affected by temperature changes.



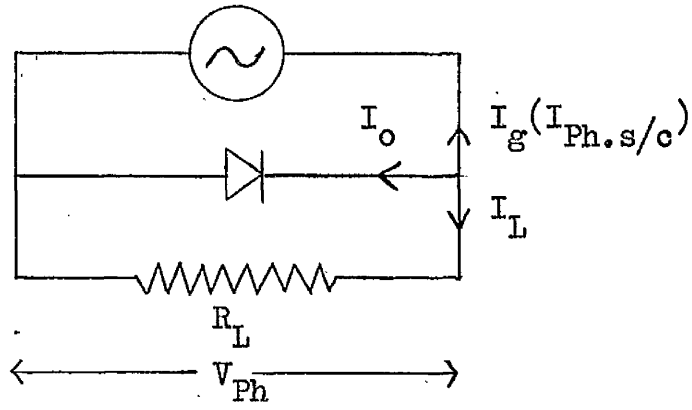
Consider the above situation in which a metal-semiconductor junction is illuminated and the photovoltage is measured across the load resistor R_L.

Now $I_{Ph.s/c} = I_{Ph} + I_o$, assuming diode theory

$$= \frac{V_{Ph}}{R_L} + I_s\left[\exp\left(\frac{eV_{Ph}}{nkT}\right) - 1\right]$$

$$= V_{Ph}\left[\frac{1}{R_L} + \frac{I_s e}{nkT}\right] \quad \text{provided } \frac{eV_{Ph}}{nkT} \ll 1.$$

Therefore, with a given diode the measurement of V_{Ph} is directly proportional to the short circuit photocurrent $I_{Ph.s/c}$ which we would like to measure. The conventional method of arrving at the above result would be to regard the photodiode as a current generator.



$I_{Ph.s/c} + I_o + I_L = 0$ and $I_{Ph.s/c}$ depends on the incident energy cm^{-2} sec^{-1}.

Now

$$I_s\left[\exp.\left(\frac{eV_{Ph}}{nkT}\right) - 1\right] + \frac{V_{Ph}}{R_L} = I_{Ph.s/c}.$$

For small V_{Ph}

$$I_s \frac{eV_{Ph}}{nkT} + \frac{V_{Ph}}{R_L} = I_{Ph.s/c}.$$

i.e. $$V_{Ph} = \left(\frac{R_D R_L}{R_D + R_L} \right) I_{Ph.s/c.}$$

where R_D is the dynamic resistance of the diode at the origin.

Hence, in order to compare the yields at various temperatures (provided the illuminating conditions of the diode are the same) we need to measure R_D at each temperature.

For our instruments, R_L = input impedance of Brookdeal LA635

$$= 5 \times 10^5 \text{ ohm.}$$

Also in the limit at low temperatures $R_D \approx 10$ M ohm, so $\frac{R_D R_L}{R_D + R_L}$ becomes R_L, therefore,

$$V_{Ph}' = R_L \times I_{Ph.s/c.}$$

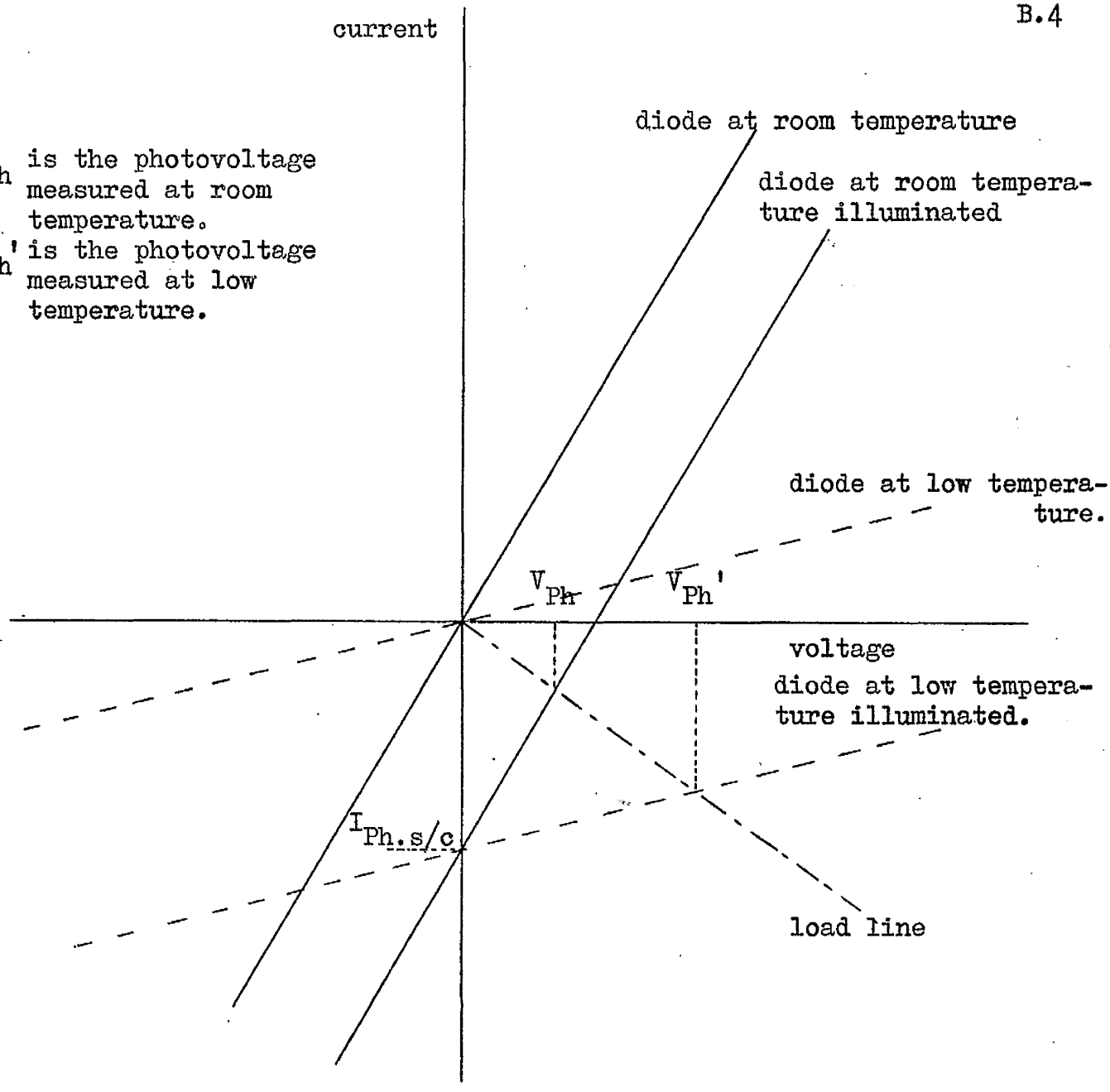
$$= 5 \times 10^5 \, I_{Ph.s/c.}$$

At room temperature $10^5 < R_D < 3 \times 10^5$ ohm, depending on the diode, therefore, $\frac{R_D R_L}{R_D + R_L} \approx 1.3 \times 10^5$ ohm, hence,

$$V_{Ph} = 1.3 \times 10^5 \, I_{Ph.s/c.}$$

Thus we appear to get larger yields at low temperatures and this has to be taken into account when plotting the yields for different temperatures on the same arbitrary scales.

This effect is illustrated on the I-V characteristic overpage.



V_{Ph} is the photovoltage measured at room temperature.

V_{Ph}' is the photovoltage measured at low temperature.