MMIC BROADBAND LOW NOISE AMPLIFIERS FOR THE SQUARE KILOMETRE ARRAY RADIO TELESCOPE

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List of Symbols

Symbol	Description	Unit
a	Lattice constant	Å
B	Noise bandwidth	Hz
C_{gd}	Gate-drain (channel) capacitance	pF
C_{gs}	Gate-source (channel) Capacitance	pF
C_{ds}	Drain-source capacitance	pF
C_{pd}	Drain bond bad capacitance	pF
C_{pg}	Gate bond bad capacitance	pF
E_C	Energy at the top of the conduction band	eV
E_F	Fermi level	eV
E_g	Band gab energy	eV
E_V	Energy at the top of the valence band	eV
F_M	Noise measure	-
f_{max}	Unity power gain maximum frequency of oscillation	GHz
F_n	Noise factor	-
f_T	Unity current gain cut-off frequency	GHz
g_m	Transconductance	S
G_T	Amplifier transducer power gain	dB
G_{TU}	Unilateral transducer power gain	dB
h_{21}	Short circuit current gain	dB
h_c	Critical thickness of hetero-epitaxy	Å
I_{DS}	Drain-source current	A
I_{DSS}	Maximum (open channel) drain saturation current	A
$\overline{i_n^2}$	Noise current spectral density	A^2/Hz
K	Boltzmann's constant (1.38×10^{-23})	J/K
K	Rollett's stability factor	-
K_1	Fukui's constant of noise figure	-
K_2	Fukui's constant of noise resistance	-
L_d	Drain metallization inductance	pH

L_G	Gate length	µm
L_g	Gate metallization inductance	pH
L_s	Source metallization inductance	pH
NF	Noise figure	dB
NF_{min}	Minimum noise figure	dB
P_{1dB}	1 dB compression point output power	dBm
R_d	Series parasitic resistance of the drain	Ω
R_{ds}	Drain-source resistance	Ω
R_g	Series parasitic resistance of the gate	Ω
R_{gm}	Gate metallization resistance	Ω
R_i	Intrinsic channel resistance	Ω
R_n	Noise resistance	Ω
R_s	Series parasitic resistance of the source	Ω
R_{sh}	Sheet resistance	Ω/□
T_e	Equivalent noise temperature	K
V_{BDG}	Drain-gate breakdown voltage	V
$\overline{V_n^2}$	Noise voltage spectral density	V^2/Hz
V_{on}	Turn-on Voltage	V
V_p	Pinch-off Voltage	V
V_{TH}	Threshold voltage	V
W_G	Gate width	µm
μ_n	Electron mobility	cm^2/Vs
μ_p	Hole mobility	cm^2/Vs
ΔE_C	Conduction band offset	eV
ΔE_g	Band gap discontinuity	eV
ΔE_V	Valence band offset	eV
χ	Electron affinity	eV
ε	Heterostructure strain	-
ε_r	Relative permittivity	-
Γ_{opt}	Optimum source reflection coefficient that results in minimum noise figure	-

Abbreviations

2DEG	Two-Dimensional Electron Gas
2-PAD	Dual Polarization All-Digital
ADS	Advanced Design System
AlGaAs	Aluminum Gallium Arsenate
BJT	Bipolar-Junction Transistor
CAD	Computer-Aided Design
CPW	Coplanar Waveguide
DC	Direct Current
DR	Dynamic Range
DRC	Design Rule Check
DUT	Device Under Test
EMD	Empirical Device Model
eV	Electron Volt
ENR	Excess Noise Ratio
FET	Field-Effect Transistor
FOV	Field of View
GaAs	Gallium Arsenate
GDB	Gate-Drain Breakdown
Ge	Germanium
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HJ-FET	Heterojunction Field-Effect Transistor
HP	Hewlett-Packard Company
HPA	High Power Amplifier
HTSC	High Temperature Superconductivity
IC-CAP	Integrated Circuit Characterization and Analysis Program
InAlAs	Indium Aluminum Arsenate
InGaAs	Indium Gallium Arsenate
InGaP	Indium Gallium Phosphate

InP	Indium Phosphate
LNA	Low Noise Amplifier
MAG	Maximum Available Gain
MASER	Microwave Amplification by Stimulated Emission of Radiation
MBE	Molecular Beam Epitaxy
MESFET	Metal Semiconductor Field-Effect Transistor
mHEMT	Metamorphic High Electron Mobility Transistor
MIC	Microwave Integrated Circuits
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuits
MOCVD	Metal Organic Chemical Vapour Deposition
MODFET	Modulation Doped Field-Effect Transistor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NiCr	Nickel Chromium
PAE	Power Added Efficiency
Paramp	Parametric Amplifier
PBM	Physical Based Model
PEL	Parameter Extraction Language
pHEMT	Pseudomorphic High Electron Mobility Transistor
PPC	Persistent photo-conductivity
QW	Quantum Well
RA	Radio Astronomy
RX	Receiver
RF	Radio-Frequency
TX	Transmitter
Si	Silicon
Si_3N_4	Silicon Nitride
SKA	Square Kilometer Array
SKADS	Square Kilometer Array Design Study
SNR	Signal-to-Noise Ratio
SOI	Second Order Intercept

SRF	Self Resonance Frequency
TaN	Tantalum Nitride
TCR	Temperature Coefficient of Resistance
TFE	Thermionic Field Emission
TLM	Transmission Line Model
TOI	Third Order Intercept
VCO	Voltage Controlled Oscillator
VCR	Voltage Coefficient of Resistance
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Ratio

ABSTRACT

In the last few years, enormous progress has been achieved in the design and implementation of MMICs employing compound semiconductors. One of the most exciting applications of this technology is the upcoming Square Kilometer Array (SKA) radio telescope which is now internationally planned. The main objective of this work is the design of an MMIC InP-based pHEMT broadband LNA in the L-band (0.3-2 GHz) with a maximum room temperature noise figure of 0.5 dB and flat gain response and the realization of the circuit in a coplanar waveguide form (CPW), as part of the European SKA design study (SKADS).

Accurate linear small-signal and nonlinear large-signal models have been extracted for two different generations of a novel in-house fabricated high breakdown 1μm strained channel InGaAs/InAlAs/InP pHEMT based on extensive experimental on-wafer device measurements and complete agreements have been obtained between the modeled and measured data. Furthermore, MMIC passive components including spiral inductors, MIM capacitors and thin-film resistors have been designed, fabricated, and accurately modeled.

All of the extracted models for active and passive components have been used for the design, simulation, and circuit mask generation of an L-band MMIC CWP InP-pHEMT LNA. The designed circuits satisfy most of the desired specifications providing a room temperature noise figure as close as possible to NF_{min} with adequate gain and return loss properties especially for the large gate width and multi-gate finger devices.

The key finding of this work was that the high breakdown and very low leakage of the newly developed pHEMT was instrumental in designing very large gate width (up to 800 μm) devices with very low noise resistance and noise figure at the low frequency end. This is a situation that is impossible to reproduce in conventional InGaAs-InAlAs pHEMT because of their large leakage currents which places severe limitations on how large a gate width can be used. Indeed, many difficulties were found during the design of MMIC broadband LNAs at such low frequency band using commercial foundry small gate width (< 400 μm) and short gate length (< 0.5 μm) devices due their poor noise resistance and input impedance characteristics.

Declaration

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

Copyright

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I am indebted to many people for their advice, encouragement and assistance throughout the preparation of this thesis. First, I would like to express my deepest thanks and sincere gratitude to my supervisor, ***Prof Mohamed Missous,*** not only for his useful supervision, sincere advice and guidance, but also for his unlimited assistance, valuable consultation, helpful comments and critical remarks while reviewing the manuscript. Also, I am deeply indebted to him for his patience, dedication and encouragement throughout the course of this project. I really feel so lucky to have him as my supervisor.

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A tribute to all my sincere friends and colleagues, who enhanced my work with their kind assistance during my stay in Manchester.

Finally, this work would not have been possible without the never-ending love of my beloved family.

Ayman

Publications

[1] A. Bouloukou, **A. Sobih**, D. Kettle, J. Sly, and M. Missous, "Novel high-breakdown InGaAs/InAlAs pHEMTs for radio astronomy applications", Proceedings of the 4th ESA workshop on Millimeter-Wave Technology and Applications (7th MINT Millimeter-Wave International symposium), pp. 221-226, Espoo, Finland, 2006.

[2] **A. Sobih**, A. Bouloukou, D. Kettle, J. Sly, and M. Missous, "Microwave characterization and device modeling of 1μm strained InGaAs/InAlAs pHEMTs for radio astronomy applications", Proceedings of the 15th European Workshop on Heterostructure Technology, HE-TECH-06, Manchester, UK, 2006.

[3] A. Bouloukou, **A. Sobih**, D. Kettle, J. Sly, and M. Missous, "Improved device performance of narrow gate recessed high-breakdown InGaAs/InAlAs pHEMTs for radio astronomy applications", Proceedings of the 15th European Workshop on Heterostructure Technology, HE-TECH-06, Manchester, UK, 2006.

[4] **A. Sobih**, B. Boudjelida, A. Bouloukou, S. Boulay J. Sly, and M. Missous, "Characterization and modelling of novel large gate periphery InGaAs/InAlAs pHEMT for ultra low noise radio astronomy applications", Proceedings of the 16th European Workshop on Heterostructure Technology, HE-TECH-07, Frejus, France, 2007.

[5] A. Bouloukou, **A. Sobih**, B. Boudjelida, S. Boulay J. Sly, and M. Missous, "Low NFmin and low Rn InGaAs/InAlAs pHEMTs for low frequency LNAs", Proceedings of the 16th European Workshop on Heterostructure Technology, HE-TECH-07, Frejus, France, 2007.

Dedication

To my Father's Soul,

My Mother,

My Wife,

And my Lovely Daughters

I Dedicate This Thesis

Ayman

CHAPTER-1

INTRODUCTION

1-1 Background and Overview

Monolithic microwave integrated circuit (MMIC) technology is extensively used in modern communication systems, radio telescopes, satellite earth stations, radar systems and space-born applications. Their small size, light weight, low power consumption, and high reliability make MMICs very attractive in cutting-edge applications. Moreover, to obtain wide frequency band characteristics with high reproducibility and uniformity, MMIC technology is by far the best candidate **[1]**.

One of the most demanding and exciting applications of MMIC technology, employing compound semiconductors, is instrumentation for radio astronomy. The design of a unique array-based radio telescope, the Square Kilometer Array (SKA) is now being internationally planned. This so called international radio telescope for the 21st century is intended to have an effective collecting area of one million square meters, increasing its sensitivity 100 times more than today's best radio telescopes such as the Very Large Array (VLA) **[2]** or Arecibo **[3]** for example.

To provide a million square meters of aperture at an acceptable cost, the SKA must make a revolutionary break with current radio telescopes designs. Institutions participating in the SKA, representing more than 15 countries from Europe, plus the

USA, Australia, Canada, China, India and South Africa are now designing and building prototype systems and many different technological solutions will be selected and integrated into the final instrument **[4]**.

1-1-1 SKA objectives

It is well known that increasing a telescope's collecting area increases its sensitivity. Thanks to higher sensitivity, weaker signals emitted by more distant or fainter celestial objects, can be received. Over the past several years, discussions have been taking place in several countries about the next logical step in radio astronomy instrumentation following the up-coming construction of large millimeter arrays such as ALMA (Atacama Large Millimeter Array). An initiative has thus emerged to develop a telescope able to provide over two orders of magnitude increase in sensitivity over existing facilities at meter to centimeter wavelengths. Achieving this goal will require a telescope with one square kilometer of collecting area - one hundred times more collecting area than the Very Large Array (VLA). The Square Kilometer Array (SKA) would probe the gaseous component of the early Universe, thereby addressing fundamental questions in research on the origin and evolution of the Universe (Big Bang). It will enable astronomers to see the formation of the early Universe, including the emergence of the first stars, galaxies' structures like the Milky-Way as well as the formation and distribution of planets. This will shed light on the birth, and eventual death, of the cosmos. The most important goal of the SKA is to receive signals from the early Universe (the most distant objects that can be observed). These signals are very faint and hence require a very sensitive telescope so that they can be detected. This means the SKA needs to be very large (one million square meters) **[5]**.

1-1-2 Difference between SKA and today's radio telescopes

Covering frequencies of 0.1–25 GHz, the SKA will make a revolutionary break with today's radio telescopes and will:

•Have a collecting area of almost one million square meters, giving it 100 times the sensitivity and 10,000 times the survey speed of today's best radio interferometers(see Figure1.1).

•Be the first aperture synthesis telescope with multiple independent fields of view (up to 100 at one time).

•Integrate computing hardware and software on a massive scale, in a way that captures the best benefits of these exponentially developing technologies.

•Use new technology antennas, signal transport, signal processing and computing in a merger between radio frequency (RF) technology and information and communication technology (ICT)

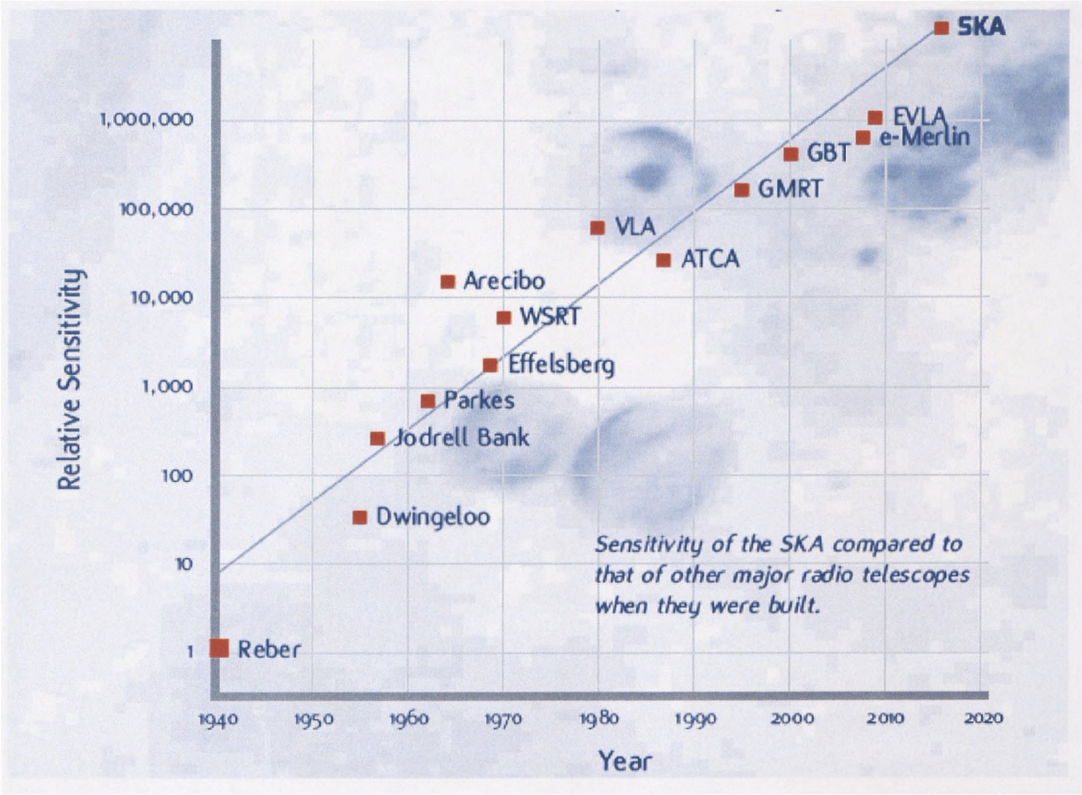


Figure 1.1 SKA's sensitivity relative to the world major telescopes [4].

1-1-3 SKA reference design

The SKA will be an interferometric array of individual antenna stations, synthesizing an aperture with diameter of up to several kilometers. A number of configurations are under consideration to distribute the 1 million square meters of collecting area. These include 30 stations each with the collecting area equivalent to a 200 meters diameter telescope, and 150 stations each with the collecting area of a 90 m telescope. For comparison, Arecibo (in Puerto Rico) is the world's largest radio telescope with a diameter of 305 m

(although not steerable), followed by the Green Bank Telescope (GBT) (100 x 110 m) in Virginia, USA , and the Effelsberg telescope (100 m) in Germany.

The reference design is composed of planar aperture arrays for the low frequency band 0.3 to ~1.4GHz and small steerable dishes with "smart feeds" for the intermediate and high frequency bands. The "smart feeds" comprise Focal Plane Arrays for the intermediate frequencies and wide-band feeds at higher frequencies.

Signals from separated antennas will be combined digitally to simulate a telescope having a diameter equal to the largest antenna separation - more than 3000 km for the SKA Figure1.2. That will give an extremely high angular resolution, so that the SKA will produce the sharpest pictures of the sky of any telescope. The SKA will also have a very large field-of-view (FOV). The goal is a FOV at frequencies below 1 GHz of 200 square degrees, and a FOV of 1 square degree (about 5 full moons) at higher frequencies **[6]**.

One exciting development being explored is the use of phased-array technology to provide multiple FOVs. This would dramatically increase the survey speed of the SKA or enable multiple users to observe different pieces of the sky simultaneously. The goal of achieving large sky coverage with multiple FOVs is a major driver of the challenging signal processing and computing specifications for the SKA. The combination of a very large FOV with enormous sensitivity and diverse operation modes means that the SKA will provide nothing less than a revolution in the way that people explore the universe.

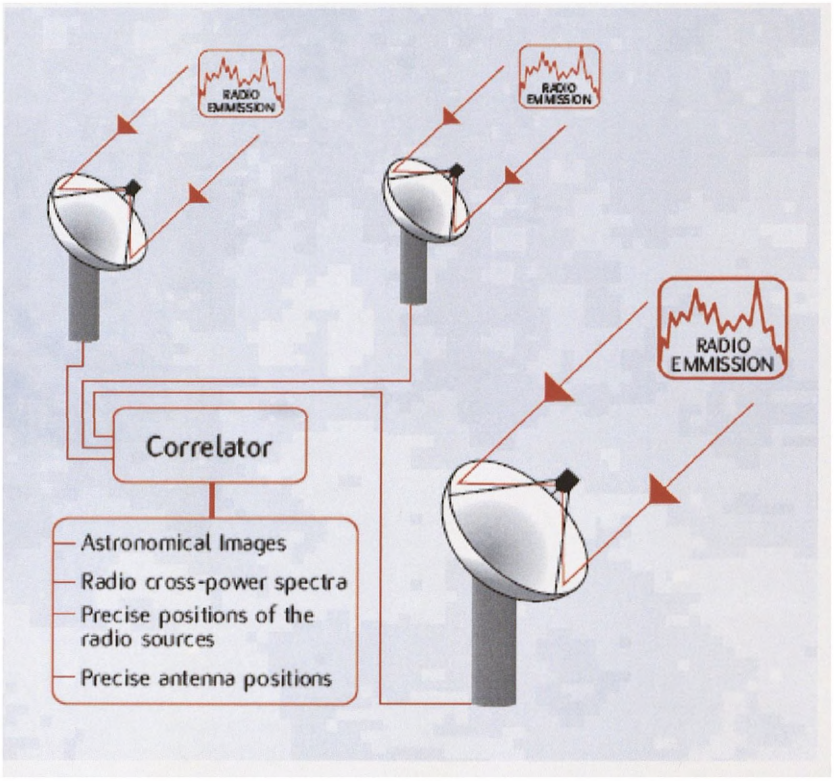


Figure 1.2 SKA's basic design concept [4].

At the present time, the international Square Kilometer Array Design Study (SKADS), a collaboration of many different research institutions all over the world (29 institutes) are working on theoretical and practical design studies to meet the SKA requirements. A decision on the technologies that the international SKA steering committee will adopt is planned for the middle of 2009.

The European SKA technology development programme focuses on the development of an all-electronic Aperture Plane Phased Array demonstrator covering the lower frequency band requirements of the SKA. The entire collector will be composed of large areas of low-cost, low-noise phased arrays, with beam formation carried out electronically. This demonstrator is known as the Dual Polarization All-Digital (2-PAD) tile, Figure 1.3. The total area of the 2-PAD has not been finally specified yet but it ranges between $1x1m^2$ to $3x3m^2$ **[7, 8]** and it will be the basic building block for the low frequency SKA band.

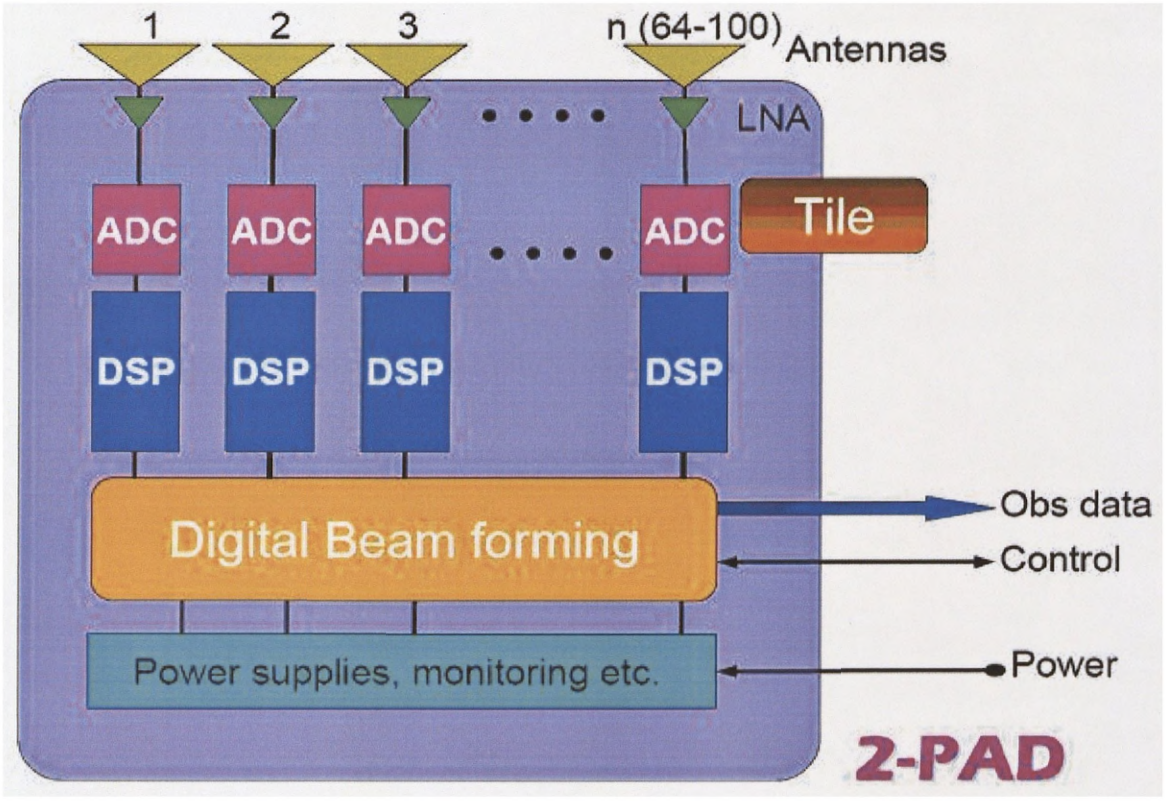


Figure 1.3 Dual polarization all-digital (2-PAD) tile configuration [8].

Finally, the critical task of the €38M European SKADS programme is to demonstrate that large numbers of electronic arrays can be built cost effectively - so that dreams of radio cameras and radio fish-eye lenses can be turned into reality **[9]**.

1-2 Motivations and Work Objectives

Generally in radio astronomy and SKA observations of radio wavelengths, Low-noise amplification is part of a crucial step to detect the small signals from the sky **[10]**. As a part of the European SKA design study (SKADS), the work presented here is focused on designing MMIC broadband LNAs based on InP material system that are tailored to the low frequency SKA telescope requirements. These amplifiers circuits should satisfy the requirements of rugged, low power consumption, and high performance room-temperature operation. There is also a requirement for low cost because, in the aperture array concept of the SKA, millions of amplifiers would be needed and while existing commercial devices are able to fulfill some of the

requirements of the SKA, their cost and breakdown fragility precludes their use in this particular application.

So, the main target in this work is to produce InP-pHEMT based MMIC broadband LNA in L-band (300-2000 MHz) with the lowest possible noise figure (< 0.5 dB) and as flat a gain response as possible and the realization of the circuits in a coplanar waveguide form (CPW). To achieve this target the following strategies are being pursued:-

►Device modeling and microwave characterization of novel (in-house) fabricated 1μm InP-based InGaAs-InAlAs pHEMTs, extraction of suitable linear and nonlinear transistor models, and comparison of DC, RF, and noise characteristics with the experimentally measured data.

►Design, fabrication and measurement of MMIC passive elements used in the LNA circuit such as spiral inductors, MIM capacitors, and thin film resistors then extraction of suitable physical models for these components based on their geometrical dimensions and comparison with experimental data.

►Using the accurate active and passive device models extracted, the design, simulation, and circuit mask generation of an MMIC broadband low noise amplifiers in the frequency range (0.3-2 GHz) in CPW format, is developed.

1-3 Thesis Organization

In this thesis, an elaborate survey of the Hetero-junction Field Effect Transistors, HEMTs and pHEMTs, history, epitaxial structure, theory of operation and their advantages over the traditional MESFETs are introduced in **Chapter-2** together with a detailed description of our in-house fabricated GaAs and InP pHEMTs.

Chapter-3 discusses the characterization of noise in microwave systems, explaining the basic concept of noise, different types of noise associated with semiconductor devices, noise parameters, and different techniques used in the noise measurements. Also, a discussion of the fundamentals of low noise amplifiers, their basic parameters, different topologies, and advances that have been achieved to date is presented.

Chapter-4 describes the microwave characterization and experimental device modeling of the InP-pHEMTs fabricated in-house. Techniques used for extracting linear small-signal and nonlinear large-signal models, of the transistors are introduced. A noise

figure characterization of the fabricated devices, based on the linear and nonlinear models parameters extracted, is also discussed.

In **Chapter-5**, the history, applications, and design methodologies of MMICs is reviewed. The advantages and disadvantages of MMICs, compared with hybrid microwave integrated circuits, will be discussed. Also, the design, fabrication, modeling, and practical measurements of the passive components used in the MMICs will be described in details.

In **Chapter-6**, the design, simulation, and realization in CPW form of an MMIC InP-pHEMT broadband LNA circuits (300-2000 MHz) based on the active and passive components models extracted before and aided by one of the most powerful CAD tools, the Advanced Design System (ADS) is introduced. Finally, the physical layout of the amplifier (circuit mask) is generated as an intermediate stage between design and processing.

Chapter-7: gives the conclusion and suggestions for further work.

CHAPTER-2

Heterojunction Field Effect Transistors

2-1 Introduction

The Heterojunction Field Effect Transistor (**HJFET**), also called Modulation Doped Field Effect Transistor (**MODFET**), is a type of field effect transistors that the Japanese Lab of Fujitsu invented and successfully commercialized at the beginning of the 1980's as a direct and real application of the new theory of hetero- structures discovered a few years earlier.

The ability of providing very high levels of performance at microwave frequencies combined with excellent noise performance make the HJFETs superior devices for low noise applications. Although only twenty five years have elapsed since HJFETs were first invented, they are now widely used as extremely low noise devices in terrestrial and space telecommunications systems, radio telescopes in the area of astronomy, direct broadcasting satellite television (DBS) receivers and car navigation receivers **[11, 12]**. In this chapter, a detailed discussion of all fundamental issues concerning the HJFETs (HEMTs and pHEMTs) is undertaken. Heterostructures will be discussed in terms of their properties, crystal growth requirements, and their use in the formation of quantum wells. The design principles, Epitaxial layer structures, theory of operation, and different breakdown mechanisms of HJFET devices will be discussed in details. Finally, the

Epitaxial structures and the measured DC and RF characteristics of the in-house fabricated InP-based InGaAs/InAlAs pHEMTs will be highlighted.

2-2 Hetero-Structures

Prior to 1980, most semiconductor devices used single-material structures formed with either silicon or GaAs. Advances in material-growth technology, such as molecular-beam-epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD) systems, led to the fabrication of devices composed of different combinations of semiconductors. The interface between two different semiconductor materials brought into contact is called a heterojunction and it is the simplest form of heterostructures. Modern high speed devices commonly contain more than one heterojunction. The main advantage of heterostructures is their ability to precisely control the motion and states of charge carriers. Also, the ability to confine charge carriers (electrons) in an extremely thin sheet and under certain conditions, the confined electron layer will exhibit quantum effects and the term two-dimensional electron gas (2DEG) is sometimes used to describe this confined-carrier layer **[13]**. Hetero-junctions are very attractive structures since a whole new group of exciting high speed devices, (HEMTs, pHEMTs, and HBTs), become potentially possible once a high quality junction between semiconductors of different band gaps can be formed.

2-2-1 Heterojunctions materials

When two dissimilar semiconductors are joined together the atoms at the hetero-interface have to form chemical bonds. As the lattice constants of these materials are different, atoms at the hetero-interface have to adjust their positions by developing strain. If this strain exceeds a certain critical value, it results in crystal dislocations which are crystal imperfections propagating through many crystalline layers. These dislocations act as scattering centers for electrons and holes, limiting their mobilities, and as recombination centers, limiting the electrons and holes lifetimes. The result may be very poor device properties. One possible way to avoid this problem is to use materials with nearly equal lattice constants, such as **GaAs** and **AlAs** (or the ternary compound $\mathbf{Al_xGa_{1-x}As}$). For some other material systems, when the lattice-mismatch is very large, such as the **GaAs/InAs** and the ternary $\mathbf{In_xGa_{1-x}As}$, hetero-epitaxial growth

in this case is achieved by using alloys of certain compositions that result in nearly lattice-matched structures. The ternary alloys $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ that are lattice matched to the InP are good examples. Another approach is to use thin periodic alternating layers producing a structure that is called a superlattice. This approach reduces the strain and the number of dislocations and is extensively used for **Si-Ge** hetero-structures **[14, 15]**.

In fact, the majority of semiconductor materials have different lattice constants and hence, most of the hetero-epitaxy processes are formed between lattice-mismatched pairs forming what is called strained layers (Pseudomorphic systems). It is also found that the strain energy produced by this type of epitaxial growth always increases as the thickness of the strained layer increases. Therefore, it is only possible to grow certain critical thickness of epitaxial layer before dislocations are generated. The strain between two lattice-mismatched layers (ε) and the critical thickness (h_c) are given by the approximate following expressions, where a_S and a_L are the lattice constants of the substrate and the epilayer respectively.

$$\varepsilon = \frac{a_L - a_S}{a_S} \tag{2.1}$$

$$h_c = \frac{a_S}{2\varepsilon} \tag{2.2}$$

2-2-2 Band discontinuities

At the hetero-interface, the abrupt changes in the conduction and valence band energies, on going from one semiconductor to the other, is of paramount importance in determining the electrical and optical properties of the hetero-junction. The distribution of the band gap discontinuity (ΔE_g) between the conduction band offset (ΔE_c) and valence band offset (ΔE_v) is of particular interest to the basic physicist as well as to the device designer. To the later it provides an extra degree of freedom in the control of flow of electrons and holes across the hetero-structure by changing the band gaps (conduction and valence band discontinuities) of the participating semiconductors. This process is known as band-gap engineering and it is key to the operation of all hetero-structure devices.

The energy band diagram of a hetero-junction is much more complicated than that of a homo-junction and, in many cases, one must rely heavily on experiments to construct it

accurately. However, the first model for a hetero-junction was developed by Anderson, 1962 **[16]**. In this model, there are two basic assumptions in the construction of the energy band diagram; firstly, the Fermi level must be the same on both sides of interface in thermal equilibrium and secondly, the vacuum level must be continuous and parallel to the band edges. Because of these assumptions, ΔE_c and ΔE_v will be unaffected by doping as long as the band gap, E_g, and the electron affinity $q\chi$ are not functions of doping (non-degenerate semiconductors). As shown in Figure 2.1 ΔE_c and ΔE_v are given by:-

$$\Delta E_c = \chi_A - \chi_B \quad (2.3)$$

$$\Delta E_v = \Delta E_g - \Delta Ec \quad (2.4)$$

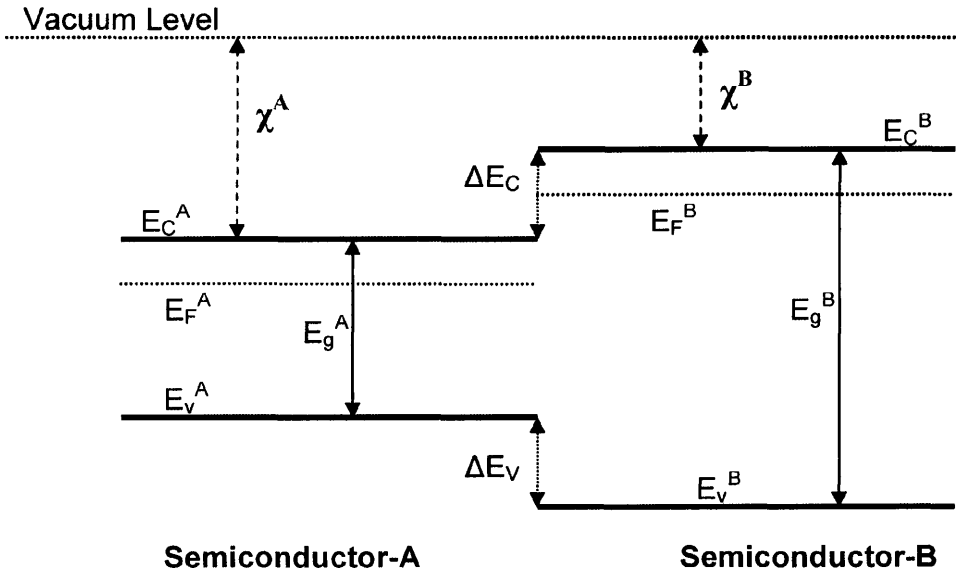


Figure 2.1 Energy band diagram of a heterojunction before contact.

Because of the uncertainties in the values of the electron affinities (or even their availability), it is not always possible to predict accurate values of the band edge discontinuities using Anderson model. Therefore many other alternative models have been proposed for band line-up prediction such as Harrison (1978) **[17]** Kroemer (1983) **[18]** and Tersoff (1984) **[19]**. In all cases, the difficulty in determining the band alignment of hetero-junctions has led to significant uncertainties in the band parameters reported for various hetero-structure systems. However, recent analysis of C-V profiling

of heterojunctions and optical measurements of confined quantum states in QWs stated that the conduction band discontinuity is nearly 60 % of the band gap offset, while the valence band is 40% in the **GaAs/$Al_xGa_{1-x}As$** material system for $0 < x < 0.4$.
Finally, the attractive property of the heterojunctions is in the different barriers seen by electrons and holes when forward voltage is applied. This would enable only one type of carriers to be injected. The barrier to holes trying to transfer from P-type to N-type would be much larger than for electrons transferring into the opposite direction. Such a property is very important and useful for modern hetero-junction based devices.

2-2-3 Quantum wells

If one makes a hetero-structure with sufficiently thin layers, quantum interference effects begin to appear prominently in the motion of the charge carriers. The simplest structure in which these may be observed is a quantum well (QW), which simply consists of a thin layer of a narrower-gap semiconductor **(e.g. GaAs)** sandwiched between two identical larger band-gap materials **(e.g. AlGaAs)**, then discontinuities in the conduction and valence band edges occur at the hetero-junction interface and QWs are generated for both electrons and holes. No quantization exists parallel to the hetero-interface and carriers are free to move along the interface forming a 2DEG. This two-dimensional world affects the energy of the electron as compared to a "free" electron in the three-dimensional case **[15]**. The effects of quantum confinement take place when the quantum well thickness becomes comparable to the de Broglie wavelength of the charge carriers leading to energy levels called "energy sub-bands", i.e., the carriers can only have discrete energy values that depend on the height and width of the barrier and can be calculated by means of fundamental quantum mechanics as follows **[20]**:

$$E = E_n + \left(\frac{h^2}{2m^*}\right)\left(k_x^2 + k_y^2\right) \tag{2.5}$$

With

$$E_n = \left(\frac{h^2\pi^2}{2m^*}\right)\left(\frac{n}{L_z}\right)^2 \tag{2.6}$$

In these equations, n is an integer denoting the sub-band index and L_z is the thickness of the potential well.

Carriers in the QW can be supplied by dopants in the wider band-gap layers. If the energy levels of the donors are above and, at least, the lowest energy level in the QW is below the Fermi level, electrons are then transferred into the QW where they establish a quasi 2DEG. Due to the space charges, band bending occurs and, consequently, a spatial separation (barrier) generated between the 2DEG and ionized impurity donors limiting the carrier transfer and representing the most basic principle of the HJ-FETs as will be discussed later.

A potential well can also exist using a single hetero-junction of GaAs-AlGaAs. Even though potential well of a single hetero-structure has an almost triangular shape (if band bending due to residual space charge in the GaAs is neglected), a quantization perpendicular to the interface and a 2DEG still exist (Figure 2.2). In this case, the quantized energy levels can be calculated using the following expressions **[21]**:

$$E_i=\left(\frac{h^2}{2m^*}\right)^{\frac{1}{3}}\left(\frac{3\pi}{2}q\xi_s\right)^{\frac{2}{3}}\left(i+\frac{3}{4}\right)^{\frac{2}{3}} \quad i = 0, 1, 2,..... \qquad (2.7)$$

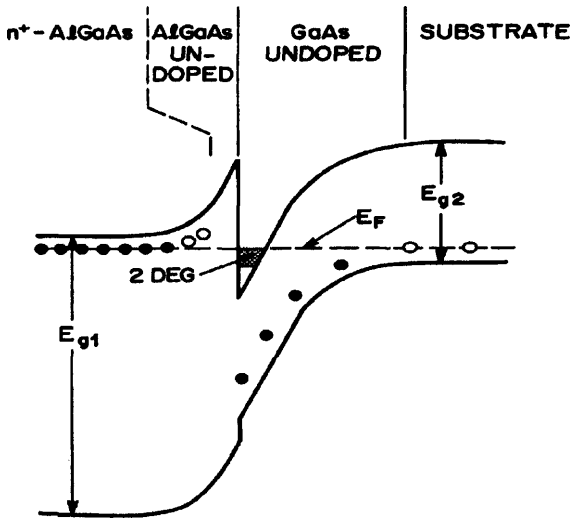


Figure 2.2 Band diagram of n^+ -AlGaAs/GaAs heterojunction [22].

2-2-4 Delta-doped layers

Delta-doping (δ-doping), also referred to as planar, pulse, atomic layer, or spike doping consists doping the semiconductor layer on a single-atomic plane rather than uniformly.

This different technique of doping can be used for improving carrier transfer and overall device performance.

In δ-doping technique, usually the doping is concentrated in a very thin region of the supply layer (3-4 mono-layers thick) with a very high doping density (typically > $2x10^{12}$ cm^{-2}). Figure 2.2 shows the band diagrams of the δ-doped and homogeneously doped structure for GaAs/$Al_xGa_{(1-x)}As$ material system. For the δ-doped structure (Figure 2.3a) energy quantization, denoted as E_0^{δ}, occurs in a quantum well generated by the built-in electrostatic potential difference in the supply layer. Size quantization in the bulk-doped structure is much smaller and is therefore neglected. If no parallel conduction occurs in the $Al_xGa_{(1-x)}As$ layers, then the Fermi level is at the bottom or below the bottom of the conduction band in the $Al_xGa_{(1-x)}As$, that is $E_F \leq E_0^{\delta}$ and $E_F \leq E_C$ for the δ-doped and bulk-doped hetero-structure respectively.

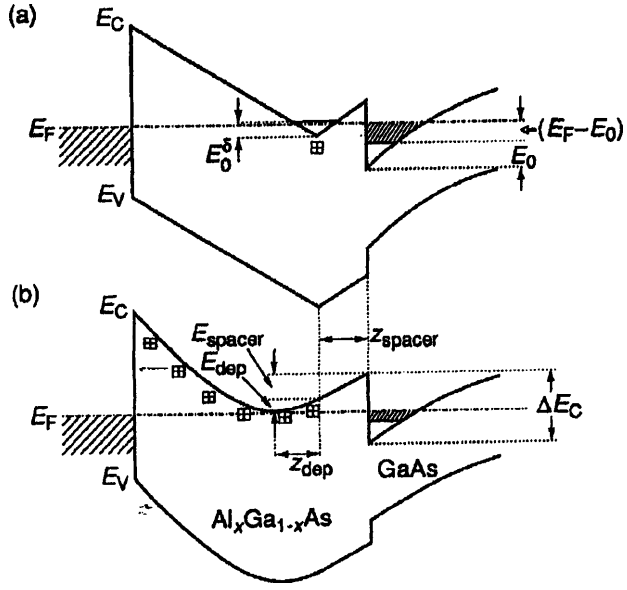


Figure 2.3 Energy band diagram (a) δ-doped AlGaAs/GaAs heterostructure. (b) Bulk-doped AlGaAs/GaAs heterostructure.

However, parallel conduction can occur in both bulk and δ-doped donor layer. δ-doping provides for higher 2DEG carrier densities compared with similar bulk doping level, allowing for the incorporation of less dopants and thus avoiding the unwanted parallel conduction effect. This is mainly due to two physical attributes; firstly, a reduction of the effective band discontinuity by E_0^{δ} increases the probability of a carrier transferring into

the 2DEG channel and secondly, the absence of depletion layer potential-drop due to the highly localized doping.

2-3 High Electron Mobility Transistors (HEMTs)

Almost three decades have now passed since the 1980 announcement of the high electron mobility transistor (HEMT) and its technology has certainly opened the door for new contributions in ultrahigh speed large-scale integration, very large-scale integration, and very high frequency applications. The evolution of high-speed, low power and ultra-low noise HEMT devices is the result of the continuous technological progress utilizing the superior electronic properties due to the very high mobility of the GaAs-AlGaAs hetero-junction structure.

According to semiconductor theory, the speed and noise performance of FETs are limited by the presence of dopant atoms in the highly-doped transport channel. These atoms, which supply the necessary charge carriers, also contribute to electron scattering due to random collisions with the ionized impurity donors used to generate them in the same region. HEMT is a smart device that was designed to resolve this contradiction **[23]**. HEMT accomplishes this by use of high mobility electrons generated using the hetero-junction of a highly doped n-type AlGaAs thin supply layer and a non-doped GaAs channel. The electrons generated in the n-type AlGaAs drop completely into the adjacent GaAs layer to form a depleted AlGaAs layer, because the hetero-junction created by different band-gap material forms a steep canyon (QW) in the GaAs side where the electrons can move quickly without colliding with any impurities **[24]**.

In fact, the short gate-channel spacing, the high mobility and effective velocity of the 2DEG and the good confinement of the 2DEG in the quantum well provide the HEMT with a significant performance again edge over the MESFET for high-speed and high frequency applications **[25]**.

2-3-1 Brief history of the HEMT

In 1977, Dr. Takashi Mimura, the inventor of the HEMT, was working in the compound semiconductor device research section of Fujitsu Laboratories. His research activities were then confined to high power GaAs FETs, GaAs MOSFETs, and GaAs ICs. In the spring of 1979, interesting work of a somewhat different technical field was brought to

his attention. This was the modulation-doped hetero-junction super-lattice developed by Dingle et al. at Bell Laboratories **[26]**.

For the next few months, Dr. Mimura concentrated his thoughts on the super-lattice structure hoping for creative ideas. He came up with the idea of using a field effect to control electrons at the interface of a single hetero-junction consisting of a pair of undoped GaAs and n-type AlGaAs; the field from a Schottky gate placed on the AlGaAs surface controls the electrons at the interface, which was the magic key to the HEMT world. In the fall of 1979, Dr. Mimura et al. submitted the first HEMT paper to the Japanese Journal of Applied Physics and it was accepted and published in May of 1980 **[27]**. Late in June, he made a presentation concerning HEMT at the DRC meeting in the United States, then, Fujitsu decided to inform the news media via a news release about the HEMT invention on June 20.

In 1985, the HEMT was announced as a unique microwave semiconductor device with the lowest noise characteristics in the world. Initially, the HEMT was used for the NRO radio telescope (45 meters in diameter) in Nobeyama Japan, where it replaced the parametric amplifier that had been used up to then. When the HEMT was cooled to liquid-helium temperature, it was able to pick up a signal from an interstellar molecule in NGC2024, which is 1,000 light years away from the earth. After discovery of the new interstellar molecule at NRO, HEMTs were successfully installed in radio telescopes throughout the world **[28]**.

Commercialization of HEMTs increased significantly in Japan and Europe around 1987 when HEMTs began to replace GaAs MESFETs in broadcasting satellite receivers. HEMTs made it possible to reduce the size of parabolic antenna by one-half or more. This particular opportunity for commercialization, however, was not in the original plan. Early HEMT technology was still in a primitive stage of development, thus, it had many weak points, especially from the standpoint of cost performance. However, later marketing studies had led to decide that HEMTs were best suited for applications in the microwave satellite communications field **[29]**.

Soon after being introduced to the marketplace, HEMT technology started to receive feedback from customers. Demand was for higher performance and less expensive HEMTs. Responding to these demands, many electronics companies invested in the

technology and, eventually, the cost-performance of the HEMT improved. Since then, the HEMT has found wider and wider applications.

2-3-2 HEMT Epitaxial layer structure

The typical layer structure of HEMT, as shown in Figure 2.4, consists of an active channel formed on the top surface of the undoped GaAs buffer layer, which is grown on a GaAs semi-insulating substrate using MBE technique. Typically this layer's thickness is approximately 0.5 to 1 μm. On top of the active channel, a thin (30 to 60 Å) layer of undoped AlGaAs (spacer) is grown. Above the spacer is the doped AlGaAs layer, which supplies the electrons for channel conduction.

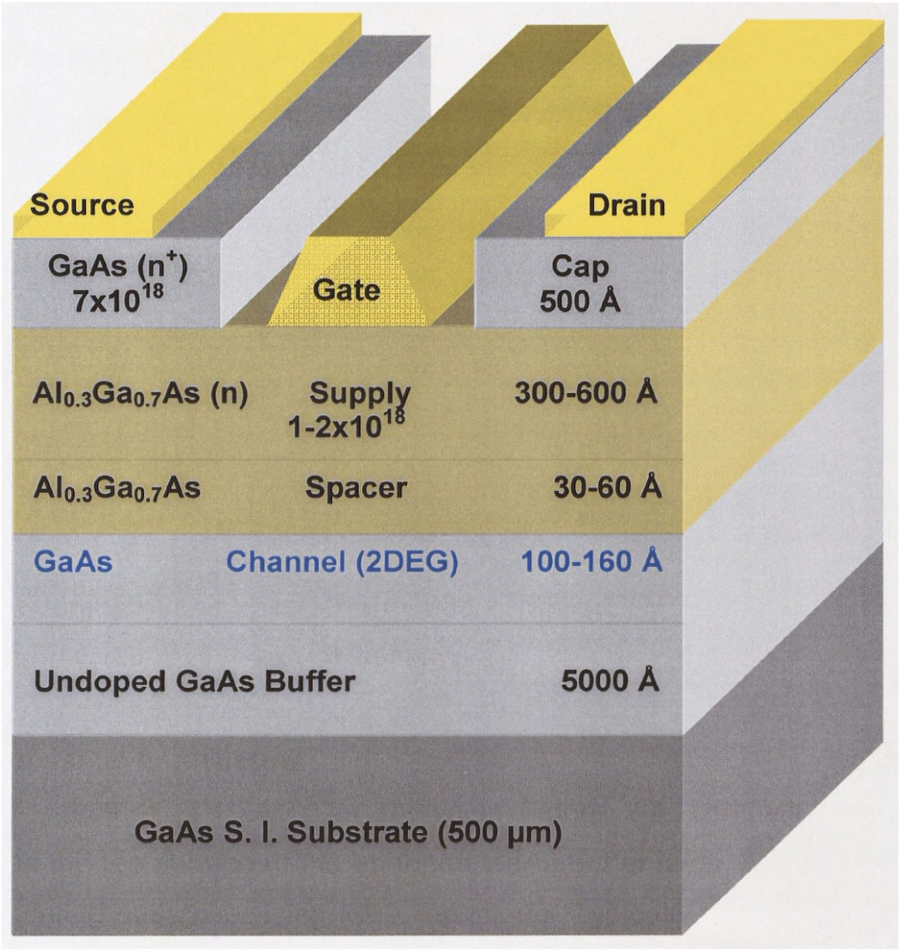


Figure 2.4 Basic epitaxial layer structure of AlGaAs/GaAs HEMT.

The electrons contributed by the n-doping in the AlGaAs are free to move through the entire crystal until they fall into the lowest energy states allowed for them in the quantum well. The width of the well is approximately 100 Å, which is more than an order of magnitude smaller than de Broglie wave length of the electron. Therefore, the electron wave function in the direction perpendicular to the interface is quantized to form the two-dimensional gas system **[30]**.

A layer of highly doped GaAs that passivates the AlGaAs and facilitates ohmic contact to the 2DEG caps the HEMT structure. The conduction in the 2DEG can be modulated and controlled by placing a Schottky gate on top of the doped AlGaAs layer to form a FET structure. In a typical HEMT structure, the AlGaAs supply layer, which is 250-600 Å thick doped at 1-2 x 10^{18} cm-3, is fully depleted otherwise a parasitic AlGaAs MESFET will be paralleling the 2DEG.

2-3-3 HEMT theory of operation

By placing a Schottky barrier (metal-semiconductor) gate above the doped AlGaAs supply layer, a depletion region of the thickness d_D is created as shown in the conduction band edge diagram of HEMT, Figure 2.5. The application of a bias voltage to the gate modulates the charge in the 2DEG and thus the channel current, thereby giving rise to the field effect action.

The pinch-off voltage of a HEMT, V_p, is defined as the gate voltage required to fully deplete the supply layer and can be expressed as:

$$V_p = \frac{qN_D d_d^2}{2\varepsilon_0 \varepsilon_S} \qquad (2.8)$$

One of the most important parameters of the HEMT is the threshold voltage, V_{TH}, defined as the voltage which the Fermi level is equal to E_C (bottom of the conduction band edge) at the HJ interface. V_{TH} is negative for depletion mode (normally on) devices while it is positive for enhancement mode devices.

Gate voltages higher than V_{TH} induce charge carriers in the channel that is modulated by V_{GS}. The 2DEG sheet carrier density along the gate length can be obtained using Gauss's law and Poisson's equation as follows **[31]**:

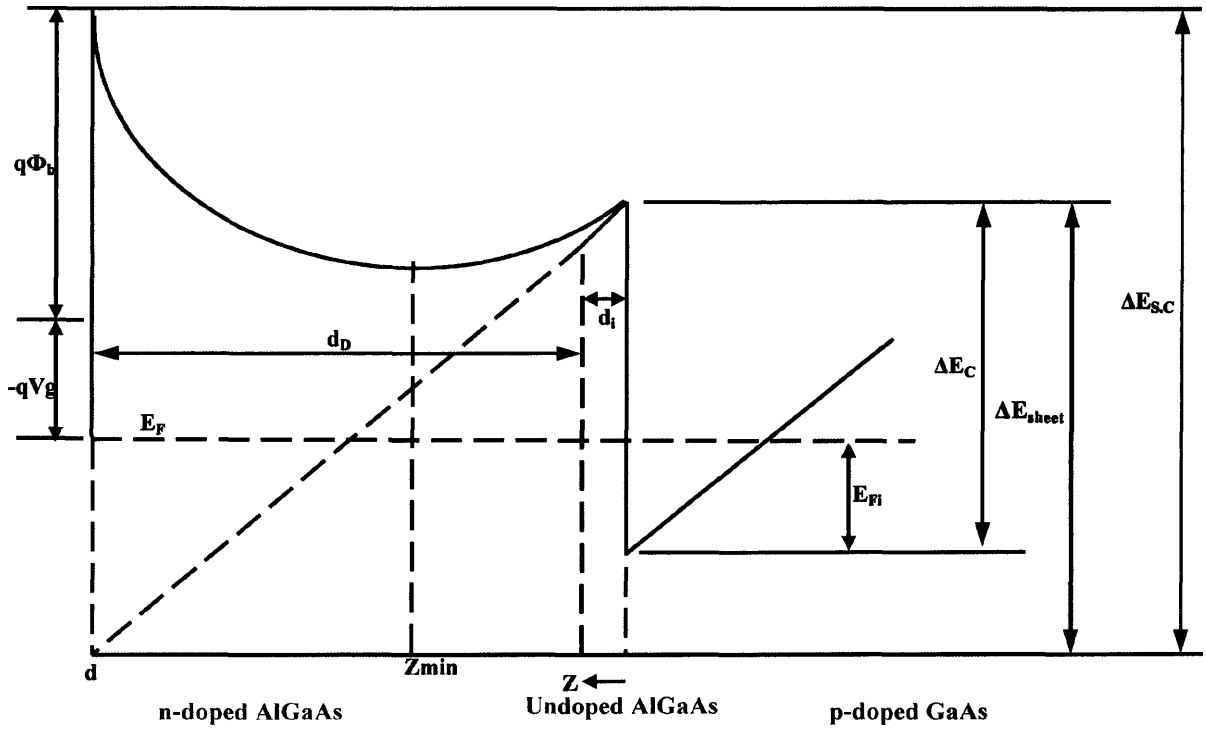


Figure 2.5 Band diagram of an AlGaAs-GaAs HEMT.

$$n_s(y)=\frac{C_i\left[V_{GS}-V_{TH}-V_{DS}(y)\right]}{q} \tag{2.9}$$

$$C_i=\frac{\varepsilon_0\varepsilon_s}{d_d+d_i+\Delta d} \tag{2.10}$$

C_i is depletion layer capacitance, d_d is thickness of the doped AlGaAs region, d_i is thickness of the undoped AlGaAs region, and Δd is the effective width of the 2DEG, given by:-

$$\Delta d=\frac{\varepsilon_0\varepsilon_s a}{q} \tag{2.11}$$

The 2DEG carrier concentration is independent of dopant concentration. Thus, in contrast to any other kind of semiconductor devices, the carriers' concentration and mobility can be optimized. Since the product of the two values determines the current and transconductance of transistors, high values of magnitudes are expected and these are indeed achieved. The spatial separation between the 2DEG and the ionized donors

in the wide band-gap material (AlGaAs) reduce the Coulombic electron-donor interaction and enhances the low-field mobility of the electrons. The ability to obtain a large sheet concentration of conduction electrons without setting off a large impurity scattering rate is one of the major advantages of HEMT structure over all other types of FETs.

2-3-3-1 Supply layer thickness and doping level

The donor (supply) layer is depleted at the interface by the hetero-junction and at the surface by the Schottky barrier. It is desirable that the two depletion regions overlap each other over the whole range of gate voltage. If the AlGaAs layers are not fully depleted, a conduction channel develops between the gate electrode and the 2DEG. This channel shields the 2DEG from potential changes in the gate, interfering with the field effect action, and degrading the performance of the HEMT. Figure 2.6 shows the depletion of the donor layer and 2DEG as functions of donor layer thickness and doping level **[32]**. When the donor layer is too thick or the doping level too high, the donor layer is not fully depleted and poor field effect action is expected in this regime.

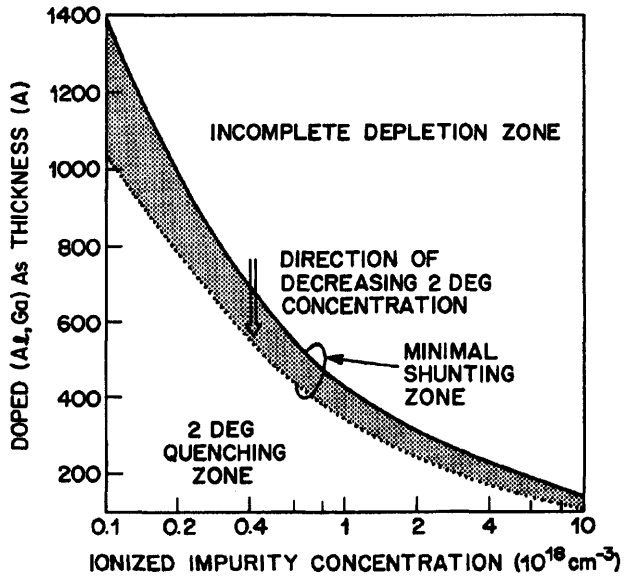


Figure 2.6 Dependence of the depletion of donor layer and 2DEG on the doping level and donor layer thickness [33].

2-3-3-2 Spacer layer thickness

The insertion of an undoped AlGaAs layer between the supply layer and the 2DEG increases the spatial separation between the electrons in the 2DEG and doping impurities in the donor layer and further enhances the electron mobility of the 2DEG. However, the density of the 2DEG and hence, the current level and the trans-conductance are reduced as the thickness of the spacer layer is increased **[34]**. Figure 2.7 illustrates the dependence of the maximum transconductance as a function of the spacer layer thickness. For HJ-FET with no spacer layer, a maximum transconductance of 250 and 400 mS/mm has been achieved at 300 and 77, respectively. But the improvement of the transconductance is offset by the reduction in mobility when the spacer layer is thinner than 2 nm. A reasonable compromise is ≥ 2 nm and is widely used for both low-noise devices and digital integrated circuits.

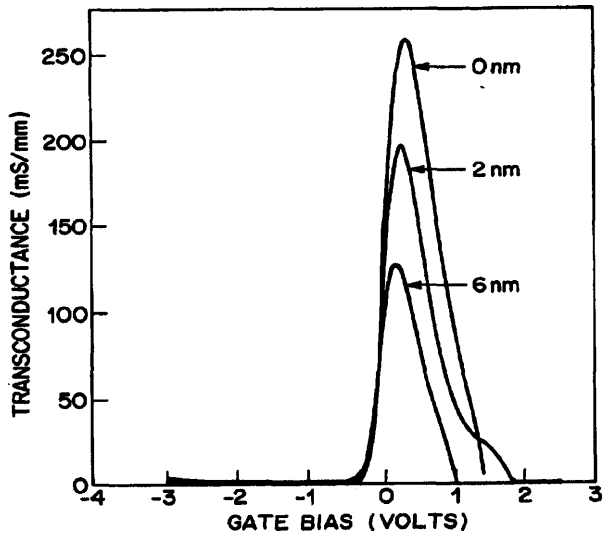


Figure 2.7 Dependence of the HEMT's Transconductance on the spacer layer thickness [33].

2-3-3-3 Effect of gate length on HEMT characteristics

The early reports of the device behavior included gate length dependence of trans-conductance and output conductance of the devices (Figure 2.8) **[35, 36]**.

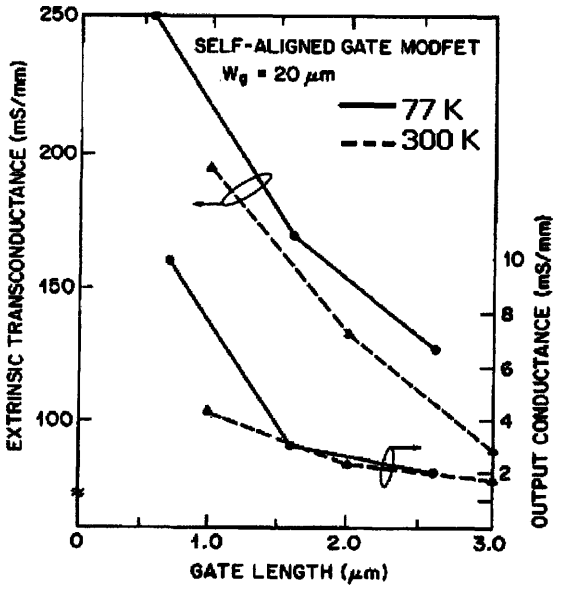


Figure 2.8 Dependence of the HEMT's transconductance and output conductance on the gate length [35].

In a HEMT, as in a MESFET, the gate length greatly influences the maximum operating frequency of the device. Gate lengths of 0.15 μm allow operation up to frequencies as high as 94 GHz, but for lower frequency applications, a large gate length is more appropriate. A compromise is made between the improved performance of short gates and higher yields possible with longer gates. For most applications of up to 20 GHz, for example, gates of 0.25 to 0.5 μm lengths are preferred. While reduced gate length is needed for best high-frequency and low noise performance, care must be taken to ensure that the gate series resistance remains acceptably low. One solution to lower gate series resistance is the use of a mushroom structure gate. The mushroom gate has another benefit as well, and which is that under RF drive, appreciable gate current can flow through the device. If the current density is excessive, electro-migration of the gate metal will occur, but the large cross-sectional area of the mushroom gate reduces the gate current density **[23]**.

2-3-4 HEMT figures of merits

All definitions relating to transconductance (G_m), parasitic resistances, unity current gain cut-off frequency (f_T) and unity power gain maximum frequency (f_{max}) of the

traditional MESFET are applied in the same manner to the HEMT and they are widely discussed in the literature **[37-39]**. All these definitions as well as all expressions defining the 2DEG charge density, 2DEG effective width, threshold voltage and the pinch-off voltage of the HEMT are given in appendix-A.

The main difference with the MESFET is the HEMT's much higher mobilities in the 2DEG (~6500 for GaAs-AlGaAs compared with 3500 cm^2/Vs for the GaAs FET) and hence lower noise figures (NF) are obtained from different noise models that will be discussed in details in the next chapter of this thesis.

Finally, the HEMT can be improved further because this device still has a number of unresolved problems **[40]**. For example, the electrons have to surmount the hetero-junction energy barrier in order to flow into the ohmic contacts. This produces additional parasitic resistance, which decreases the extrinsic device transconductance. In the HEMT, the 2-DEG layer charge density is partially determined by the doping in the AlGaAs layer below the gate. Higher current density in the 2-DEG requires greater doping density, with the subsequent degradation of the device's breakdown voltage.

2-4 Pseudomorphic High Electron Mobility Transistors (pHEMTs)

Lattice matched AlGaAs/GaAs HEMT has offered both high gain and excellent noise and power performance at microwave and millimeter-wave frequencies (0.3-300 GHz). However, despite these impressive results, the $Al_xGa_{(1-x)}As$ material system suffers from inherent problems such as shift in threshold voltage, drain current-voltage (I-V) saturation collapse and persistent photo-conductivity (PPC) due to DX centers defect in AlGaAs layer and this has capped the real potential of high 2DEG carrier density and mobility in HEMT applications.

One way to avoid the I-V collapse and PPC effects is to substitute the GaAs epitaxial layer with another compound layer $Al_xGa_{(1-x)}As$, and to keep the Al concentration below 0.22. However, choices of the compound materials are severely limited due to the lattice-matched constraint for epilayer to be successfully grown on the GaAs substrate. However, provided the epitaxial layer does not exceed a certain critical thickness it is possible to grow layers that have widely differing lattice constants, the mismatch being accommodated as strain.

The compound $In_xGa_{(1-x)}As$ is widely grown as the conducting channel in form of $In_{0.15}Ga_{0.85}As$ on GaAs. This layer is not lattice matched to the substrate. However, with the advent of MBE growth technique, the lattice-mismatched layer can be grown sufficiently thin so that the mismatch is accommodated entirely as elastic strain. The interface between the materials is essentially free from dislocations, and the layer is **Pseudomorphic [22]**.

Another way to use materials of different lattice constants is to place a buffer layer between them. This is done in the mHEMT or metamorphic HEMT, an advancement of the pHEMT developed in recent years. In the buffer layer made of InAlAs, the indium concentration is graded, so that it can match the lattice constant of both the GaAs substrate and the InGaAs channel. This brings the advantage that practically any Indium concentration in the channel can be realized, so that the devices can be optimized for different applications (low indium concentration provides low noise, high indium concentration gives high gain).

2-4-1 InGaAs-AlGaAs pHEMTs

The typical layer structure of the basic InGaAs-AlGaAs pHEMT, as shown in Figure 2.9, consists of an active channel of $In_xGa_{(1-x)}As$ with composition 0.15-0.2 and thickness 100-160 Å, formed on the top surface of the undoped GaAs buffer layer of typical thickness 0.5-1 μm, which is grown on a semi-insulating substrate. On top of the active channel, there is a thin layer (30-60 Å) of undoped $Al_{0.2}Ga_{0.8}As$ spacer. Above the spacer is the δ-doped $Al_{0.2}Ga_{0.8}As$ layer, which supplies the electrons for channel conduction.

Generally the main advantages of using the Pseudomorphic InGaAs in HEMT are the enhanced electron transport (mobility & velocity), improved carrier confinement and large conduction band discontinuity at the AlGaAs/InGaAs hetero-interface. This in turn allows even higher 2DEG carrier density, which implies higher current density and transconductance than ever possible with the conventional AlGaAs/GaAs HEMT.

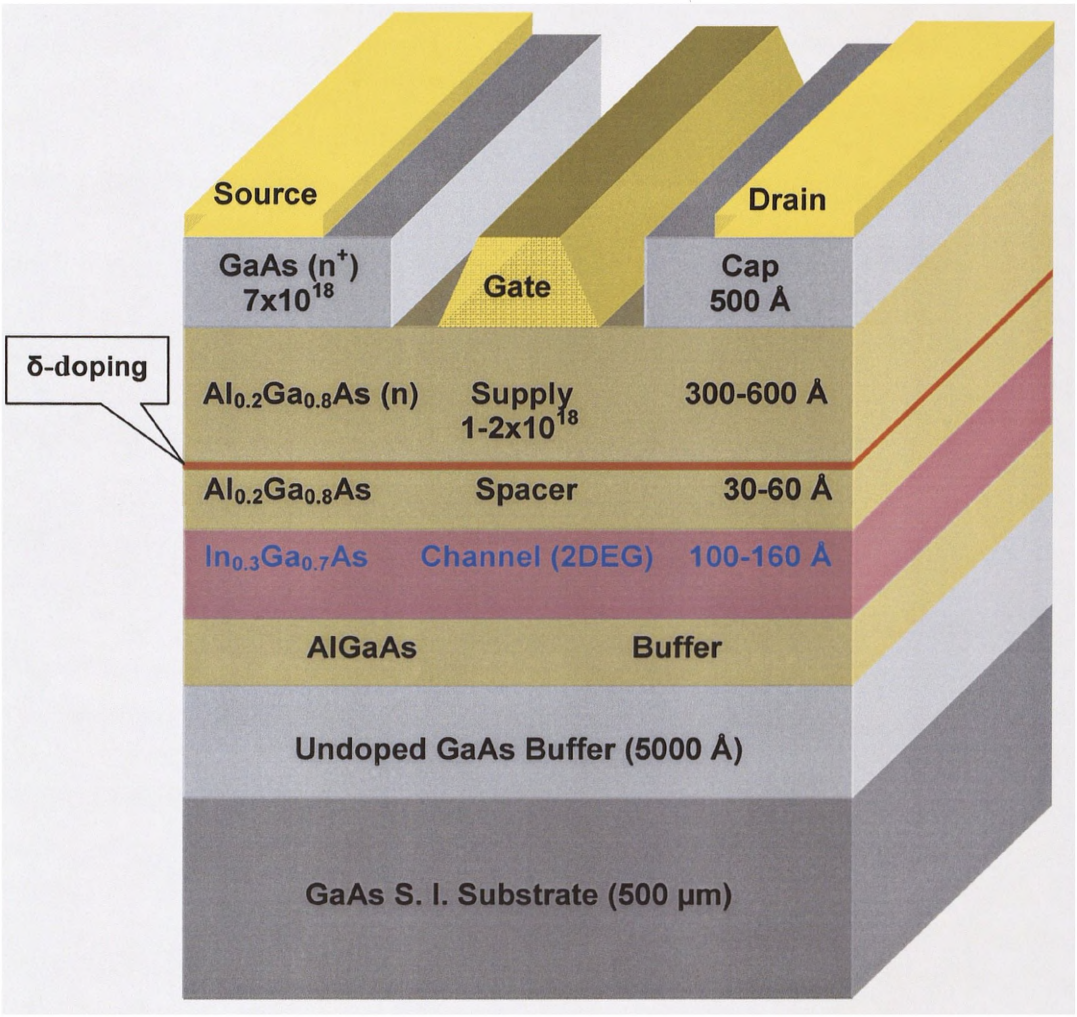


Figure 2.9 Basic InGaAs-AlGaAs pHEMT Epitaxial layer structure.

In addition, δ-doped hetero-structures not only provide higher 2DEG carrier density but also higher carrier mobility, which in turn reduces the parasitic resistance from source-gate and source-drain contacts because parasitic resistance is inversely proportional to the carrier mobility. As a result, the transconductance, gm, and noise behavior of the device can be further improved. Generally, δ-doped HJ-FETs compared with conventional HJ-FETs have shown to exhibit all of the following characteristics **[22]**:-

(1) Higher breakdown voltages.

(2) Higher 2DEG carrier density.

(3) Lower parasitic resistances.

(4) Higher intrinsic transconductance.

(5) Better control of threshold voltage.

(6) Improved linearity on pHEMT I-V transfer characteristics.

2-4-2 InGaP-InGaAs pHEMTs

The use of the ternary compound $In_{0.48}Ga_{0.52}P$ lattice matched to GaAs has attracted a greater attention as possible replacement for the AlGaAs in many electronic and optoelectronic devices since it has almost the same band gap as $Al_{0.35}Ga_{0.65}As$ (≈ 1.9eV). Its advantages over AlGaAs are :-

- Higher breakdown voltages and improved power performance **[41]**.
- Higher crystal quality due to the absence of Al which is very active material.
- Relatively inert-surface which is not easily oxidized prior to gate formation.
- DX problems related such as persistent photoconductivity (PPC), I-V collapse at low temperature and threshold voltage shift are virtually eliminated.
- low surface recombination velocity of InGaP, which will reduce the low frequency noise in the pHEMT.
- High etching selectivity between GaAs and InGaP, which implied high uniformity and reproducible device characteristics **[42]**.

All these features make $In_{0.48}Ga_{0.52}P$ a favorable material to replace AlGaAs in the AlGaAs/InGaAs structure. The growth of $In_{0.48}Ga_{0.52}P$ as a high performance device has always been dominated by metal organic chemical vapour deposition (MOCVD). The main reason for this domination is that the quality of the $In_{0.48}Ga_{0.52}P$ layer grown using MBE has been put off by problems associated with the high vapour pressure of white phosphorus. However, in recent years high quality $In_{0.48}Ga_{0.52}P$ growth has been possible by producing phosphorus molecules (P_2) from heating up the compound GaP at high temperature (P_2 decomposition source). This source yields not only high quality material but also compatible with MBE in the sense that high vapour pressure associated with phosphorous are avoided making for a safer source to use **[43]**.

2-4-3 InGaAs-InAlAs pHEMTs

InP-based InGaAs-InAlAs pHEMTs, our main concern during this work, have demonstrated the highest cut-off frequencies (Figure2.10) and the lowest microwave noise of all three terminal semiconductor devices **[44]**.

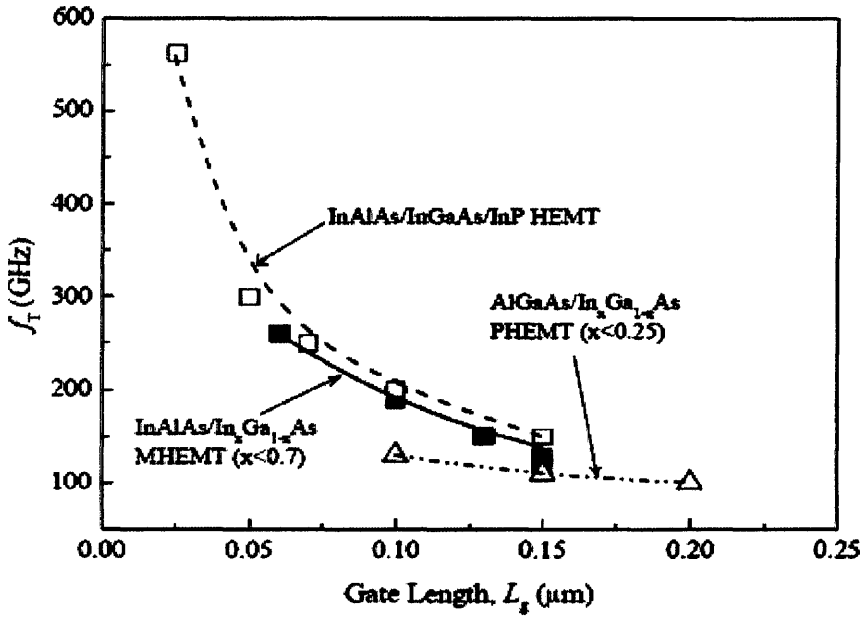


Figure 2.10 Cut-off frequency versus gate length for reported GaAs and InP pHEMTs [45].

These high performances are attributed to the excellent electrical properties of this material system such as low-field high electron mobility, high saturation velocity, high sheet carrier density, and reduced parasitic resistances.

Chen et al **[46]** investigated the characteristics of the lattice-matched Pseudomorphic and graded Pseudomorphic InAlAs/$In_xGa_{1-x}As$, and found improved device linearity was achieved by using graded channel layer due to the improved carrier confinement. Overall the highly-strained pHEMT system exhibited the highest transconductance and current driveability due to the high indium composition **[47]**. In general, The InGaAs-InAlAs devices have the following advantages over the conventional GaAs/AlGaAs pHEMTs;

- Higher conduction band discontinuity allowing more efficient carrier transport and confinement in the channel.

•Higher carrier mobility in the 2DEG due to smaller effective mass and better carrier confinement due to deeper quantum well formation.

•Higher peak velocity due to higher Γ-L valley separation leading to better noise performance and higher cut-off frequency.

However, there are many problems associated with this material system such as poor breakdown, gate leakage, and sub-threshold drain characteristics with the inherent small bandgap of the channel layer in the structure **[48]**.

At the University of Manchester, there have been considerable efforts on the improvement of the breakdown characteristics, leakage current, and all parameters that are closely related to the breakdown and noise performance through modification of the epitaxial layer structures and fabrication processes as will be discussed in the last section in this chapter.

2-5 Breakdown Mechanisms in HJ-FETs

Gate-drain breakdown (GDB) is the main factor limiting the current (power) handling capability of compound semiconductor hetero-structure FETs, which are biased in the saturation region in most analog applications. In the HEMT's I-V characteristics, the maximum value of the drain current at certain gate voltage is restricted by the gate-drain junction breakdown at high levels of the applied drain voltage. The two basic breakdown mechanisms in HEMTs are the tunnelling effect of the gate electrons and the avalanche multiplication due to impact ionization process **[49]**.

2-5-1 Tunneling effect

Tunneling breakdown usually occurs in fairly highly doped semiconductors when the maximum electric field in the depletion layer approaches values of the order of 1000 kV/cm. Under such conditions the width of the depletion layer is so narrow that electrons may tunnel from their occupied states in the valence band of the p-type region into empty states of the conduction band in the n-type region. This phenomenon is called thermionic field emission and it is one of the three basic mechanisms of current transport in semiconductors **[31]**.

2-5-2 Impact ionization

In the impact ionization process, an electron (or hole) gains so much kinetic energy from the applied high electric field that it initiates a transition of another electron from the valence band into the conduction band. Newly created carriers are, in turn, accelerated by the electric field and create new electron-hole pairs by the same phenomena. If the applied voltage is high enough, this will lead to an uncontrolled rise in the current until it is either limited by an external load or the device is destroyed. A crude estimate of the critical voltage V_{BR} may be obtained by assuming that avalanche breakdown occurs when the electric field in the reverse biased junction exceeds a certain critical value (F_{BD}) for impact ionization process to start.

$$V_{BD} = \frac{\varepsilon F_{BD}^2}{2qN_D} \tag{2.12}$$

Typical values reported for F_{BD} are 100 kV/cm for Ge, 300 kV/cm for Si, 400 kV/cm for GaAs, and 2300 kV/cm for silicon carbide **[50]**.

2-5-3 Off-state breakdown

The off-state breakdown is mainly due to the very high gate leakage current because of the high levels of applied reverse bias voltage ($V_{GS}<V_{TH}$). In this case, the channel is pinched-off and the electrical behavior of the device can be represented by a simple diode circuit with two diodes in parallel, as shown in Figure 2.11. From this figure, it can easily be noticed that the off-mode breakdown is mainly determined by the breakdown behavior of the gate-drain and gate-source diodes. Therefore the first attempt to understand the breakdown physics is to investigate the two terminal characteristics of these diodes. However, the off-state breakdown in the two-terminal case is defined as the gate-drain voltage at which the gate leakage current reaches 1mA/mm, as reported by the majority of researchers and they also believe that the thermionic-field emission (TFE) or tunneling is the dominant mechanism in case of the off-state breakdown **[51-54]**.

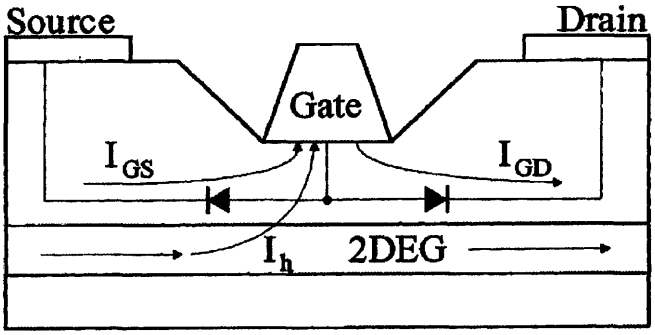


Figure 2.11 Simplified model of the device in the off-state mode [54].

2-5-4 On-state breakdown

Typically the on-state breakdown is defined as a significant upturn in the drain current, or as increase in the output conductance in the case of open channel bias conditions ($V_{GS}>V_{TH}$). However, this definition is rather ambiguous due to the significant output conductance typically present in short gate length HEMTs. An alternative approach is to use a burnout criterion in which the device is biased at a given gate voltage, and the drain voltage is increased until the device is destroyed. While such a definition is precise, it is undesirably destructive.

Experimental data for HEMTs generally indicated that the drain breakdown voltage, BV_{ds} increases as the gate bias, V_{gs}, increases towards pinch-off. A model that explained the measured breakdown performance has been reported by Trew and Mishra **[55]**. They showed that TFE is the dominant leakage current generation mechanism in on-state (open channel) operation, where the electric field is not so high, while combined effects of TFE and Avalanche multiplication (impact ionization) dominate the breakdown characteristics near pinch-off **[56-58]**.

2-6 In-House Fabricated HJ-FETs

For the upcoming international SKA radio telescope, discussed in Chapter-1, rugged (i.e. high breakdown), high-performance (i.e. low noise and high gain), room temperature operation is paramount. There is also a requirement for low cost because, in the aperture array concept of the SKA, millions of LNAs would be needed and while the existing commercial devices (mainly 0.1 μm-gate, InP–based pHEMTs) are able to

fulfill some of the requirements of SKA, their cost and breakdown fragility precludes their use in this particular application.

The SKA project team in the School of Electrical and Electronic Engineering at the University of Manchester, has the responsibility of designing, fabricating, and testing of a prototype MMIC broadband LNAs for potential use in this international project as a part of the European SKA design study. For this purpose, a family of 1μm InP-based InGaAs/InAlAs high power high breakdown pHEMTs has been developed to investigate the optimum device features suitable for the best breakdown characteristics and noise performance in the SKA frequency band of operation (0.3-2 GHz). All Epitaxial growth and fabrication processes have been developed by other coworkers (Prof M. Missous "Growth" and Dr A. Bouloukou "Fabrication") while the author of this thesis was responsible for measurements, analysis and modeling of the fabricated devices and then the design of complete LNA circuits using the newly developed devices.

In this section, some light will be shed upon these devices, their epitaxial layers structures, DC, and RF characteristics. All details about design principles, processing technique, and all other technological issues can be found in **[59]**.

Also, a family of the in-house fabricated GaAs/AlGaAs devices will be introduced in Appendix-D and their measured DC and RF characteristics as well as predicted noise performances will be compared with the InP devices introduced here.

2-6-1 Epitaxial layer structures of the fabricated samples

The epitaxial growth of all samples under investigation has been done in-house using the MBE-technique. All structures incorporate an identical highly strained (~70% In) undoped InGaAs channels to utilize the enhanced carrier transport properties of such materials. The main layer varied among these samples is the supply layer to check its effect on the threshold voltage, leakage current, RF and noise performance. The epitaxial structures of all samples are shown in table 2.1, with the VMBE prefix indicates samples grown on the V90H MBE machine while the XMBE denotes growth on the V-100 system.

For different compositions shown in the table, the supply layer varies in terms of doping, thickness, and indium concentration. Considering the baseline supply layer to lattice-

matched InAlAs donor of thickness 300 Å and δ-doping density of $3.6x10^{12}$ cm^{-2} (VMBE-1831), the variations among the other samples are:-

Sample	VMBE-1831	VMBE-1832	VMBE-1841
Cap	$In_{0.53}Ga_{0.47}As$ (50 Å)		
Supply	$In_{0.52}Al_{0.48}As$ (300 Å)	$In_{0.26}Al_{0.74}As$ (280 Å)	$In_{0.52}Al_{0.48}As$ (150 Å)
δ-doping	3.6×10^{12} cm^{-2}		
Spacer	$In_{0.52}Al_{0.48}As$ (100 Å)		
Channel	$In_{0.7}Ga_{0.3}As$ (140 Å)		
Buffer	$In_{0.52}Al_{0.48}As$ (4500 Å)		
S. I. Substrate	InP (350 μm)		
Sample	**XMBE-22**	**XMBE-34**	**XMBE-106**
Cap	$In_{0.53}Ga_{0.47}As$ (50 Å)		
Supply	$In_{0.52}Al_{0.48}As$ (300 Å)	$In_{0.26}Al_{0.74}As$ (150 Å)	$In_{0.52}Al_{0.48}As$ (300 Å)
δ-doping	3.6×10^{12} cm^{-2}	3.76×10^{12} cm^{-2}	2.6×10^{12} cm^{-2}
Spacer	$In_{0.52}Al_{0.48}As$ (100 Å)		
Channel	$In_{0.7}Ga_{0.3}As$ (140 Å)	$In_{0.7}Ga_{0.3}As$ (154 Å)	$In_{0.7}Ga_{0.3}As$ (160 Å)
Buffer	$In_{0.52}Al_{0.48}As$ (4500 Å)		
S. I. Substrate	InP (625 μm)		

Sample	XMBE-38
Cap	$In_{0.53}Ga_{0.47}As$ (50 Å)
Supply	$In_{0.52}Al_{0.48}As$ (150 Å)
Δ-doping-1	3.76×10^{12} cm^{-2}
Spacer-1	$In_{0.52}Al_{0.48}As$ (100 Å)
Channel	$In_{0.7}Ga_{0.3}As$ (150 Å)
Spacer-2	$In_{0.52}Al_{0.48}As$ (100 Å)
Δ-doping-2	1×10^{12} cm^{-2}
Buffer	$In_{0.52}Al_{0.48}As$ (4500 Å)
S. I. Substrate	InP (625 μm)

Table 2.1 Epitaxial layer structures of different samples under investigation.

•A 50% thinner (150 Å) supply layer has been incorporated aiming to provide better charge control of the channel, lower threshold voltages, and higher transconductances of the devices (Samples VMBE-1841 and XMBE-34, 38).

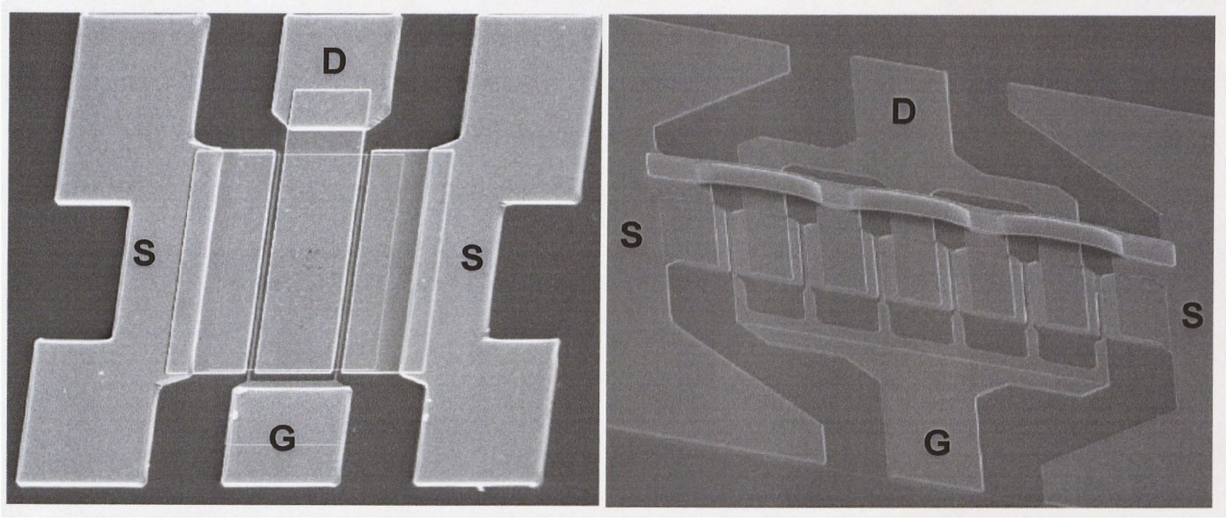
•A wider band-gap supply layer of strained $In_{0.26}Al_{0.74}As$ (280 Å), has been used for the purposes of larger Schottky barrier to the channel, lower tunneling gate leakage current, and hence better breakdown characteristics (VMBE-1832).

Based on these compositions, different gate geometries have been developed with two, four, and six gate-figures of widths 50-400 μm each providing total gate widths from 200 μm up to 1.2 mm.

During the Schottky gate contacts formation, two different metallization schemes have been applied to the InAlAs supply layer after opening the required gate recesses;

(1) Thin gate metallization scheme with total metal thickness of 150 nm (50 nm Ti/100 nm Au). This process has been applied to only four samples (VMBE-1831, 1832, 1841, and XMBE-22). Devices fabricated by this process used two gate fingers **(Figure 2.12a)** with total gate sizes from 20 μm to 200 μm and for simplicity this process will be referred to as "The old process".

(2) Thick gate metallization scheme with total metal thickness of 450 nm (150 nm Ti/300 nm Au). This "New process" has been applied to samples XMBE-106, 38, and VMBE-1841. Larger devices have been fabricated by the new process not only the simple two gate finger structure devices but also the multi (four and six) gate fingers employing air-bridges technique **(Figure 2.12b)** providing transistors with gate sizes up to 1.2 mm for the first time for such kind of material systems.



(a) (b)

Figure 2.12 SEM images of the fabricated devices
(a) Two gate fingers (old process). (b) Six gate fingers (new process).

All devices were fabricated with the same gate length (1 μm) so no mention of the gate length will be made any more during this work and all devices will be expressed in the form (N x Wg) while N is the number of gate fingers and Wg is the finger width.
Hall Measurements of the 2DEG carrier concentration and mobility for all samples are given in table 2.2. The obtained mobilities and sheet carrier densities compare favourably with reported values of similar structures in the literature **[60-62]**.

Sample ↓	n_H (x10^{12} cm^{-2})		μ_H (cm^2/V.s)	
	RT	77 K	RT	77K
VMBE-1831	1.9	2.1	13200	51300
VMBE-1832	1.45	1.7	10700	48100
VMBE-1841	1.2	1.65	13000	57800
XMBE-22	1.8	2	11800	49100
XMBE-106	1.16	1.64	12300	54000
XMBE-38	2.5	2.75	11658	34244

Table 2.2 Hall measurement results of the fabricated samples.

2-6-2 Measured DC and RF characteristics of the old process samples

The forward and reverse Schottky diode characteristics for the old process samples are shown in Figure 2.13. The forward diode characteristics of VMBE-1831 and XMBE-22 are quite similar which was expected for two samples having the same epitaxial structure and doping profile but grown on different MBE systems. Turn-on voltages (calculated at Ig = 0.1 mA/mm **[63, 64]**) have been obtained at 0.435 V and 0.45 for these two samples respectively. Due to its thinner InAlAs supply layer, much smaller turn-on voltage (0.24 V) has been obtained for VMBE-1841, while sample VMBE-1832 exhibits a V_{on} of 1.1 V because of the much large band gap material in the supply layer. This sample also exhibited the lowest leakage current. In all cases breakdown voltages well in excess of 10V are obtained, compared with 4 to 5V for conventional devices.

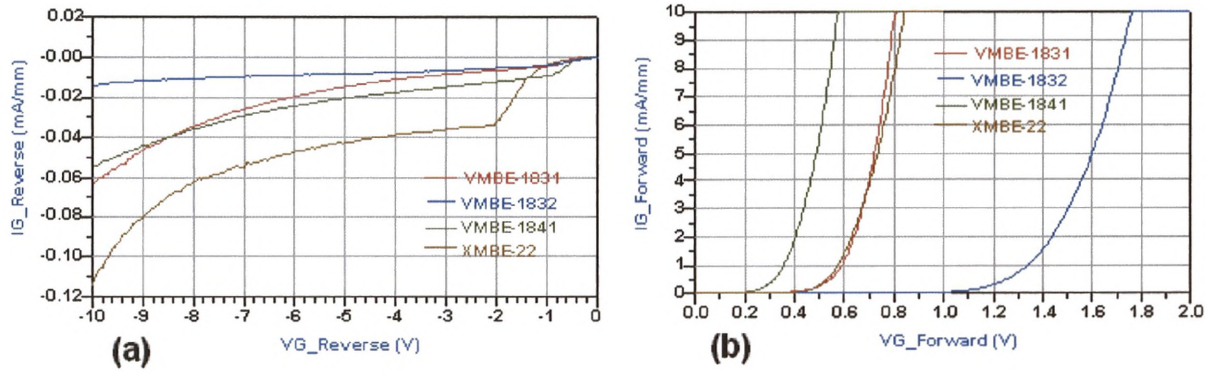


Figure 2.13 Schottky diode characteristics of the high breakdown old process devices (a) Reverse (b) Forward.

The most important advantage of our In-House fabricated devices is their excellent breakdown behavior, reporting the highest off-state breakdown voltages for such type of material systems. As shown in Figure 2.13b, the off-state leakage current is well below 1mA/mm up to -10 V for all samples.

The on-state leakage current densities are shown in Figure 2.14. They exhibit the well known bell-shape behavior of impact ionization **[65, 66]**. A maximum leakage of approximately 35 μA/mm (at V_{DS} = 1.5 V) has been measured for sample VMBE-1841. A significant reduction in the on-state leakage is observed for VMBE-1832, only 1μA/mm at V_{DS} = 1.5 V, that is one order of magnitude less than all other samples.

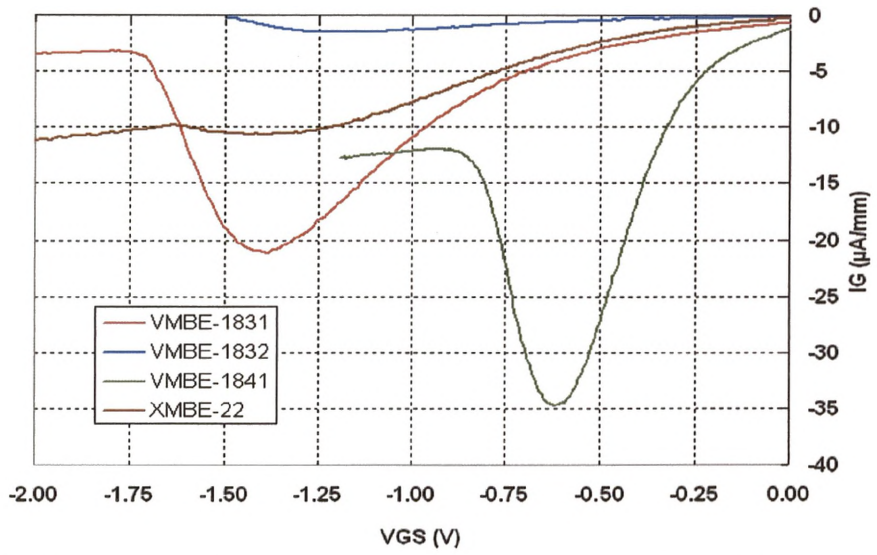


Figure 2.14 On-state leakage current of the old process samples at V_{DS} = 1.5 V.

The transconductance characteristics shown in Figure 2.15, exhibit a sharply defined pinch-off. The highest maximum g_m (≈ 450 mS/mm @ V_{DS}=1.5 V) has been observed for VMBE-1841, compared with all other samples and that may be attributed to the better modulation efficiency of the shallower channel. Note the very high value of g_m despite the relatively large gate length of 1 um. It should also be noted that the peak g_m for samples VMBE-1841, 1831, and XMBE-22 have been achieved at gate voltages very close to the pinch-off. This distinct property for our devices gives a great advantage when designing LNAs because in that case, the optimum DC bias point for the lowest possible noise performance can be chosen at very low current levels and hence high efficiency LNAs can be provided.

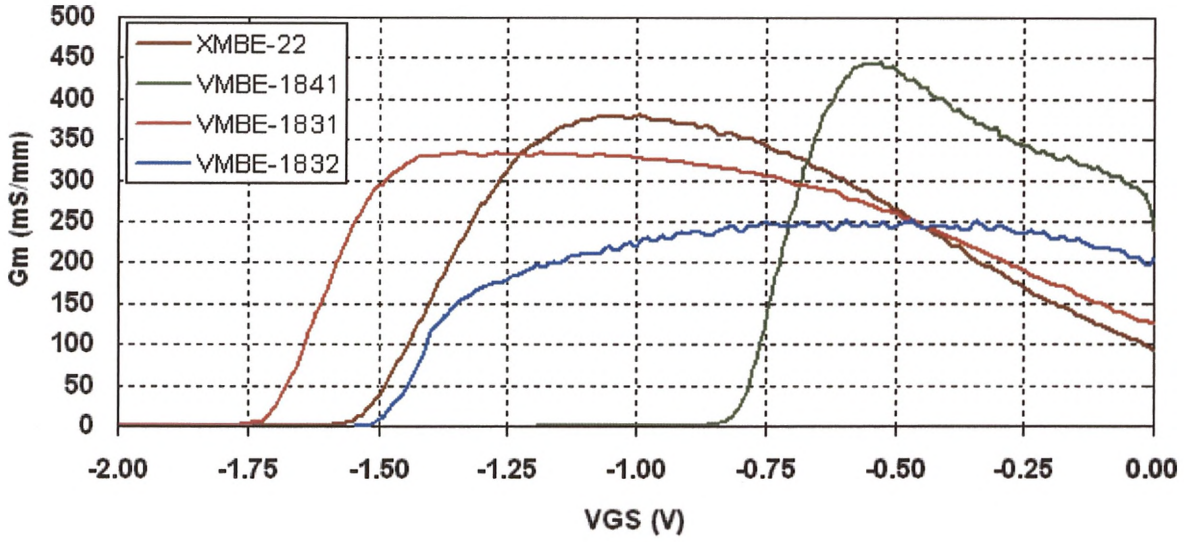


Figure 2.15 Transconductance characteristics of the old process samples at (V_{DS} = 1.5 V).

The lowest pinch-off voltage (-0.78 V) has been obtained for the sample with the thinnest supply layer (VMBE-1841) and in contrast the highest pinch-off (-1.6 V) has been obtained for the thickest supply layer sample (VMBE-1831), as shown in Figure 2.16.

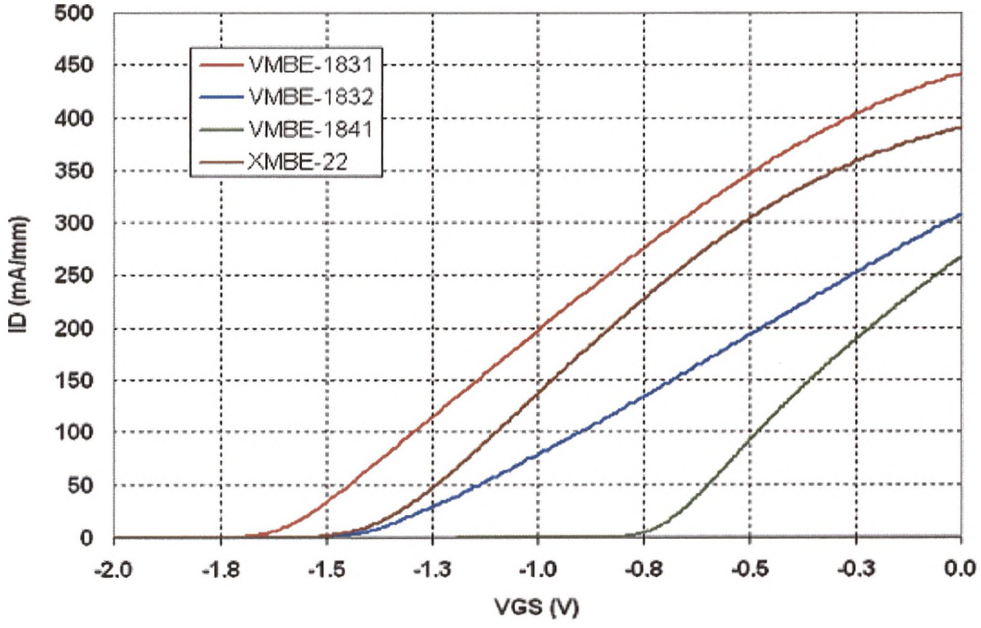


Figure 2.16 I_D-V_{GS} curves used the extraction of V_{TH} of the old process samples at (V_{DS} = 1.5 V).

Figure 2.17 shows the measured common source output characteristics of all samples from which it can again be noticed sharply defined pinch-offs. A small amount of kink is observed for all samples with the highest current (I_{DSS} = 450 mA/mm @1.5 V) being obtained for sample VMBE-1831 and the lowest current (I_{DSS} = 290 mA/mm @1.5 V) for VMBE-1841 because of the higher carrier sheet densities in the former.

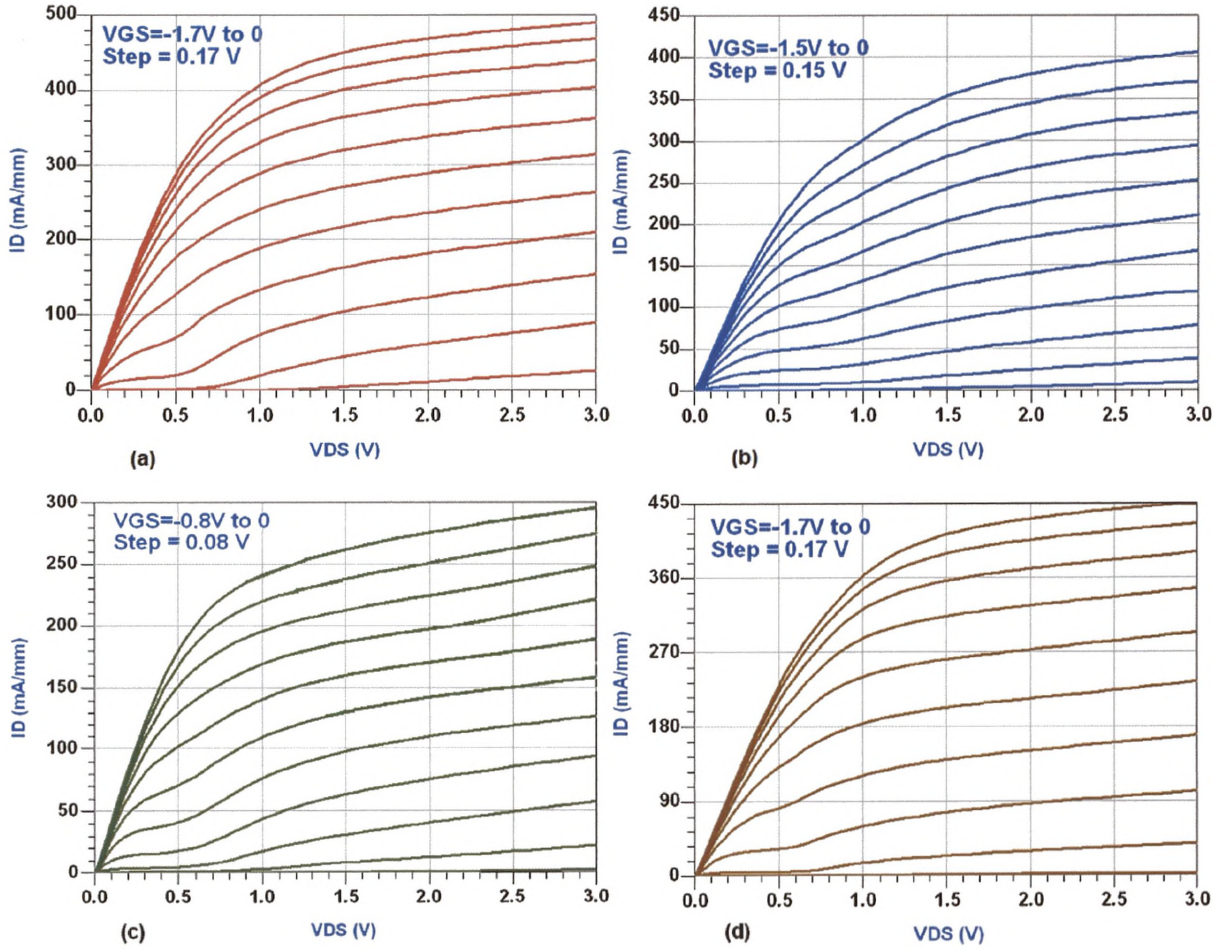


Figure 2.17 Common source IV-curves for the old process samples (normal size 2x100 µm) (a) VMBE-1831 (b) VMBE-1832 (c) VMBE-1841 (d) XMBE-22.

The common source output conductance characteristics are shown in Figure 2.18, with all devices biased for maximum transconductance. From this figure can be noticed a very small output conductance in saturation with a relatively higher output conductance

(g_o) obtained for samples VMBE-1831, 1832 which may be attributed to the narrower gate recess.

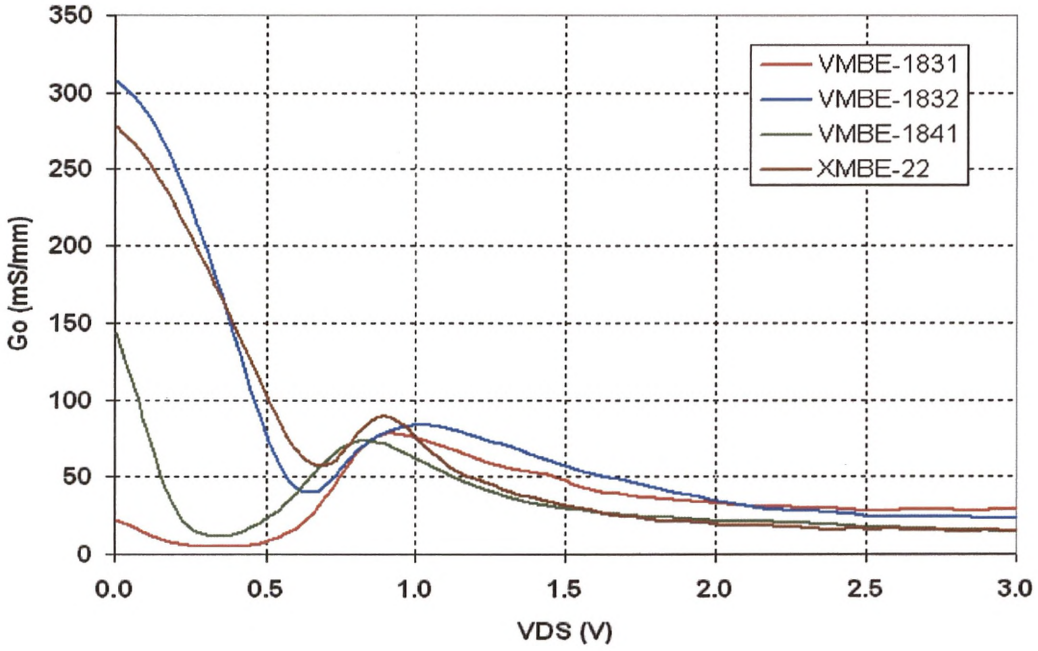


Figure 2.18 Common source output conductance for the old process samples, at gate bias for maximum Gm.

The RF characteristics of the fabricated devices have been measured on-wafer in the frequency range form 45 MHZ to 40 GHz using an HP-8510C VNA along with a Cascade Microtech RF probe station at many different DC bias points and also different modes of operation of the devices for the purpose of device modeling, these issues will be discussed in details in chapter-4.

The unity current gain cut-off frequency, f_T, and the unity power gain maximum frequency of oscillation, f_{max}, have been obtained form the unilateral current gain (H_{21}) and the maximum available gain (MAG). H_{21} and MAG have been calculated from the measured S-parameters using the ADS simulations.

Figure 2.19 shows the high frequency characteristics of a 2x100 μm devices from the four different samples. All devices are biased for peak transconductance at V_{DS}=1.5 V. The cut-off frequencies demonstrated by all devices are higher than 30 GHz, reflecting

the high intrinsic speed of the samples. The highest f_T (38.4 GHz) has been achieved with sample VMBE-1831, representing the excellent values for the gate geometry used.

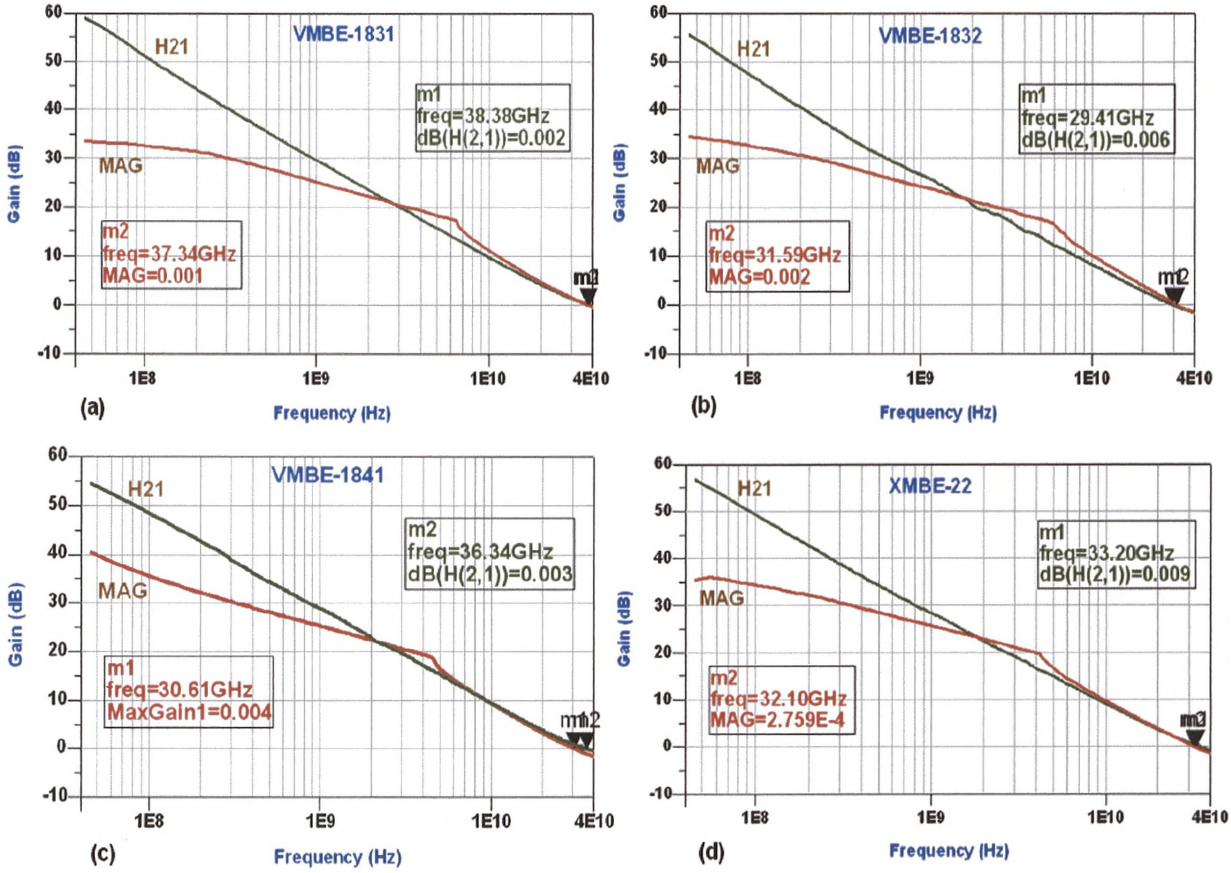


Figure 2.19 RF characteristics of the fabricated samples (device size is 2x100 µm biased for maximum Gm at V_{DS} = 1.5 V).

The relatively low f_{max} obtained for all samples may be attributed to high parasitic effects on the devices' performance. The relation between f_T and f_{max}, given in **[67, 68]** states that:-

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_S + R_g + R_i}{R_{ds}} + 2\pi f_T R_g C_{gd}}} \qquad (2.13)$$

This relationship shows that the parasitic resistances (Rg and Rs) together with the gate-drain capacitance (Cgd) strongly affect the value of f_{max}. This issue will be

addressed in depth during the device modeling and parameters extraction processes introduced in Chapter-4.

2-6-3 Measured DC and RF characteristics of the new process samples

The new process of the thick gate metallization has not been optimized yet and all samples that will be introduced here have been fabricated on the first run of this process. So, any unexpected behaviors for the new devices compared with the old ones, such as shift in the threshold voltage, lower g_m, current, or higher leakage are may be to some extent attributed to processing problems such as using a different photo-resist which may not be suitable for a perfect lift-off for the much thicker metal layers. However, this will not greatly affect our main target of investigating the optimum device structure for the best noise performance in the low SKA frequency band.

Figure 2.20 shows the forward and reverse Schottky diode characteristics for the new process samples. The turn-on voltage of sample VMBE-1841 has not changed (0.25 V) and although it exhibits higher off-state reverse leakage current, it still has very high breakdown voltage.

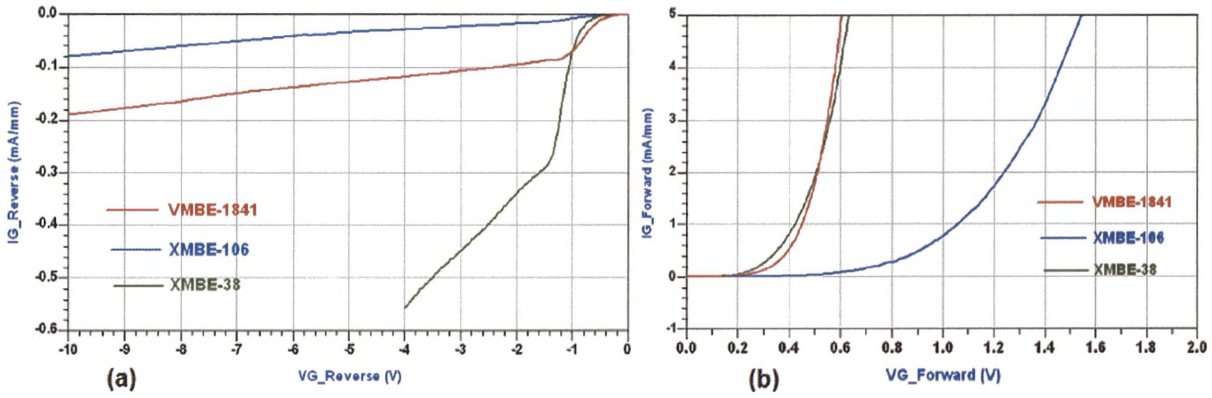


Figure 2.20 Schottky diode characteristics of the new process samples (a) Reverse (b) Forward.

While sample XMBE-106 exhibits the highest turn-on voltage (0.63 V) and the lowest off-state leakage current (90 μA/mm @ V_G=-10 V), sample XMBE-38 in contrast has provided the lowest turn-on voltage (0.24 V) and the highest reverse leakage current (0.55 mA/mm @ V_G = -4V), resulting in a much lower breakdown voltage for this sample compared with all other samples.

Sample XMBE-38 also suffers from a significant increase in the on-state leakage (520 μA/mm at V_{DS} = 1.5 V), that is almost two order of magnitude higher than all other samples, as shown in Figure 2.21. However, all of these observations for this sample were expected because of the high carrier density due to the double-delta doping profile.

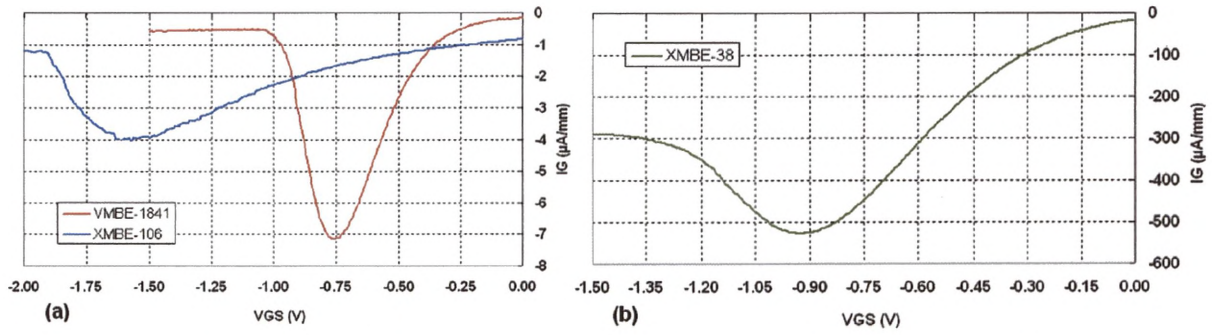


Figure 2.21 On-state leakage current the new process samples at V_{DS} = 1.5 V.

The transconductance characteristics of the new devices are shown in Figure 2.22. Samples XMBE-38, as expected, provides the highest maximum gm (≈ 440 mS/mm @ V_{DS}=1.5 V) and the lowest transconductance has been observed for XMBE-106 (230 mS/mm @ V_{DS}=1.5 V).

It should be noted that sample VMBE-1841 exhibits about 20% reduction in gm compared with the old process and almost the same percentage shift in the threshold voltage (-0.98 V instead of -0.78), Figure 2.23 due to some processing problems as stated before (in particular the existence of a residual thin photoresist layer in the AZ process which would explain the higher threshold voltage and reduced gm).

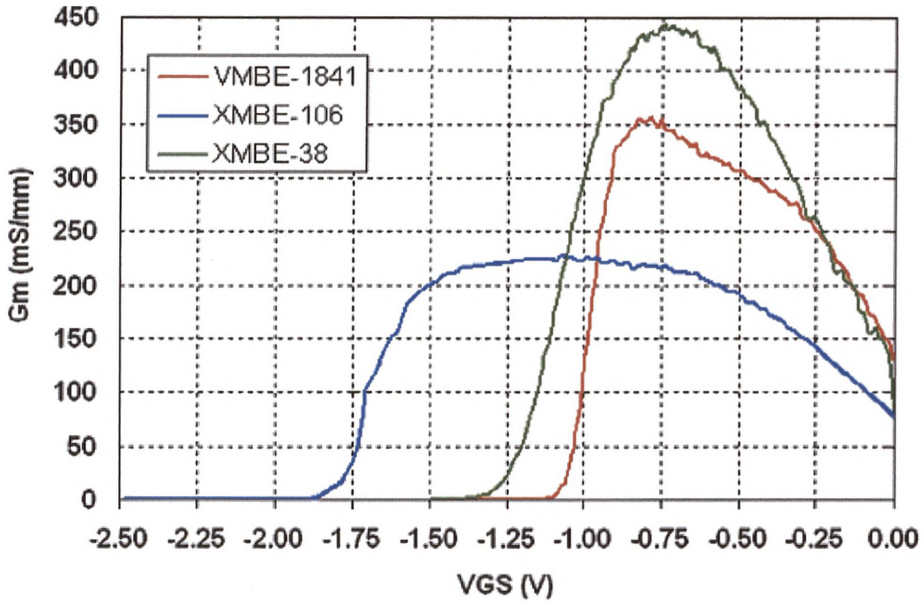


Figure 2.22 Transconductance characteristics of the new process samples at V_{DS} = 1.5 V.

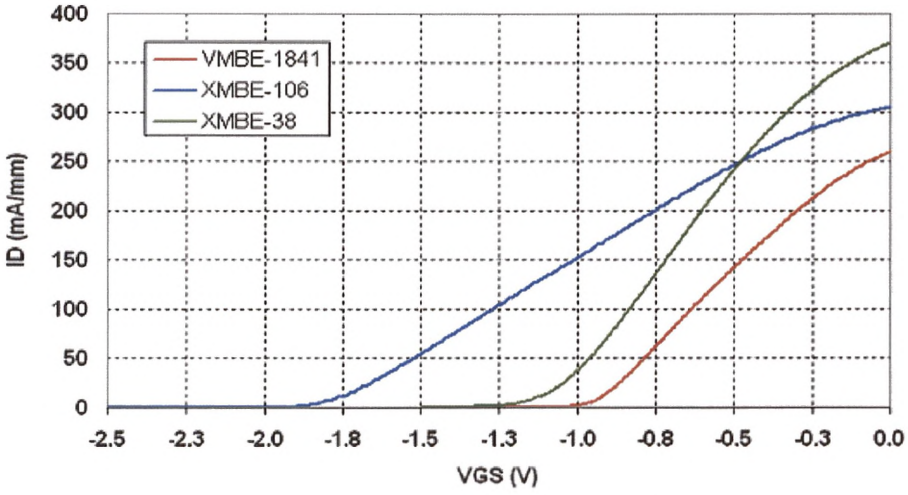


Figure 2.23 I_D-V_{GS} characteristics of the new process samples at V_{DS}= 1.5 V.

The typical common source IV-curves of the new samples are shown in Figure2.24. As expected, the double-delta doped sample (XMBE-38) provides the maximum current density (I_{DSS} = 375 mA/mm @ V_{DS}=1.5 V), while VMBE-1841 exhibits 10% reduction in current compared with the old process (I_{DSS} = 260 mA/mm @ V_{DS}=1.5 V).

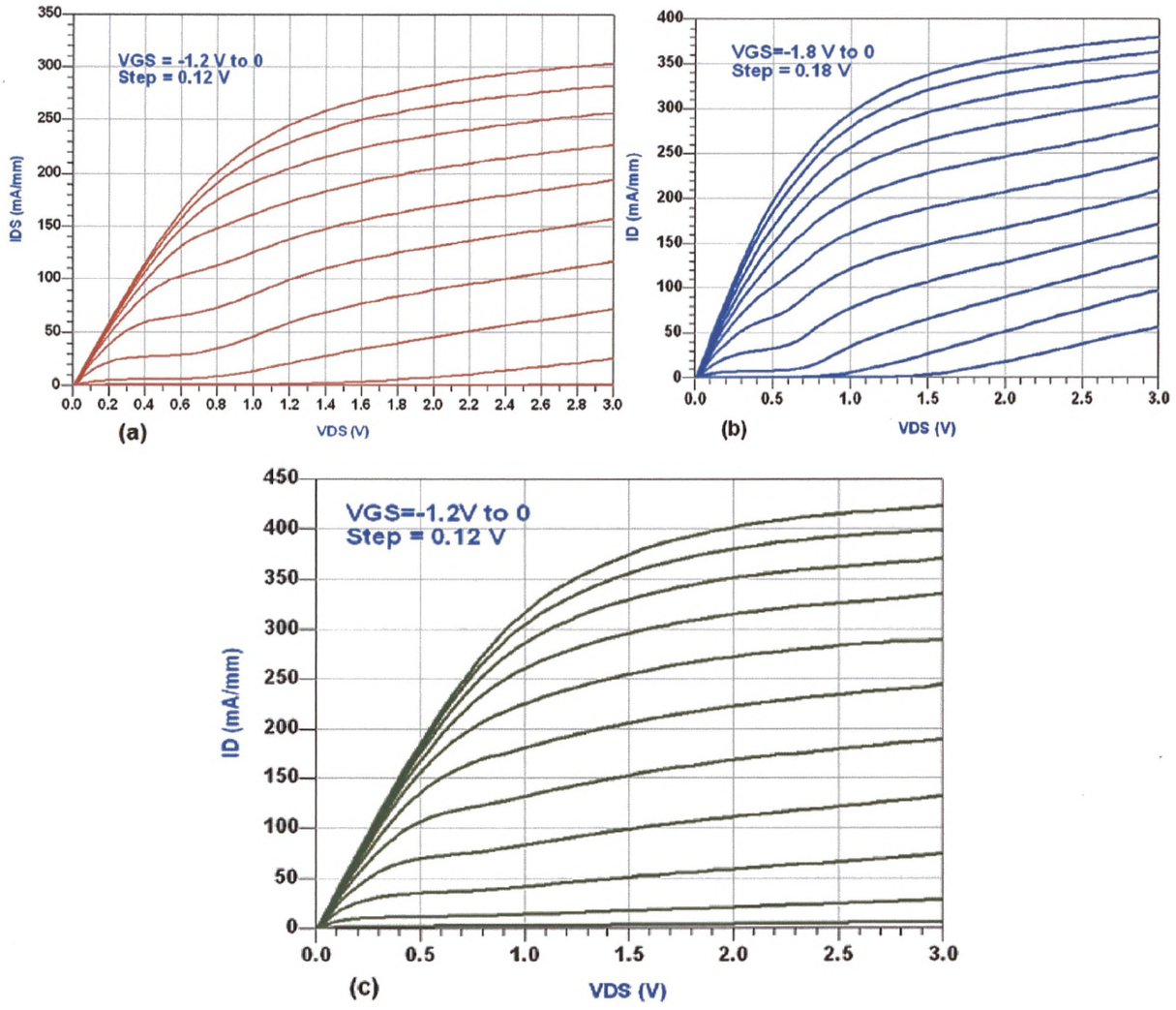


Figure 2.24 Common source IV-curves for the new process samples (normal size 2x200 µm), (a) VMBE-1841 (b) XMBE-106 (c) XMBE-38.

Compared with the old process samples, the new devices exhibit the same high cut-off frequencies but with much higher maximum oscillation frequencies as shown in Figure 2.25. These results mean that the new devices suffer much less parasitic effects than the old process devices as will be proved later in chapter-4.

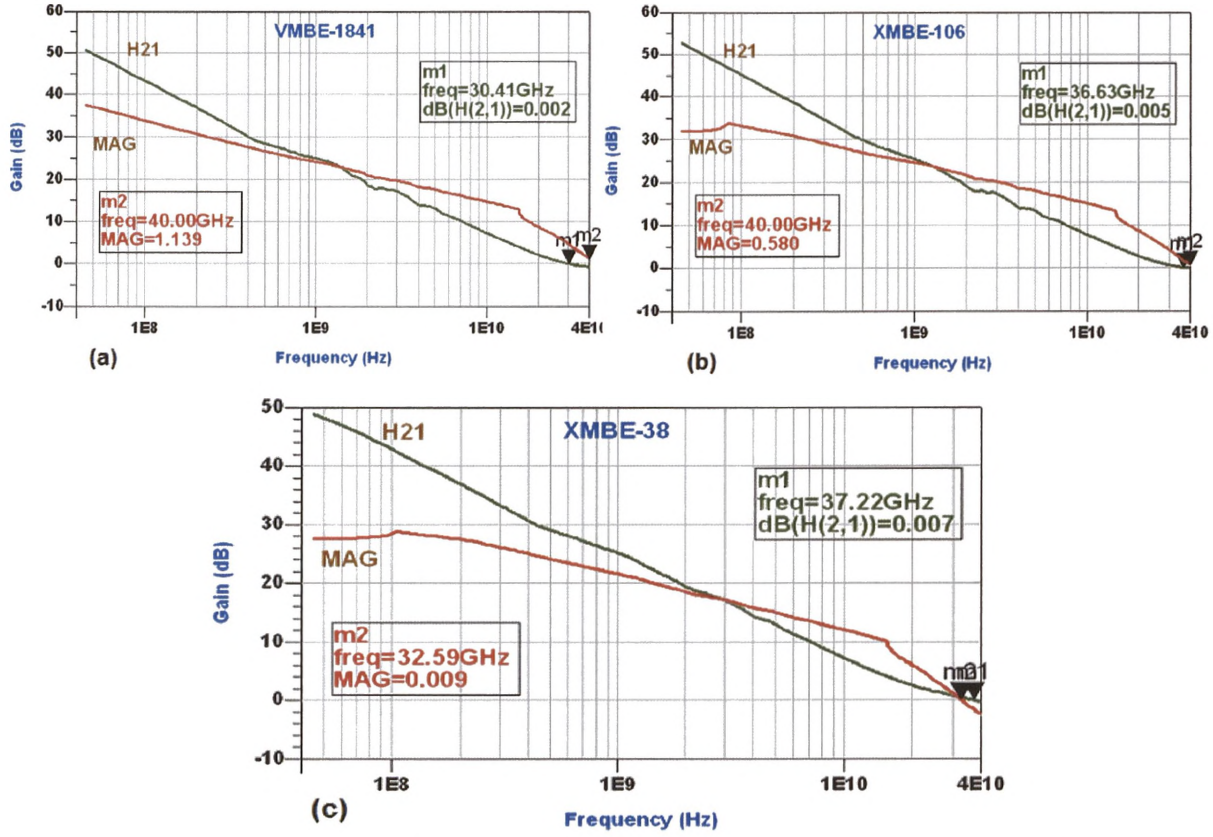


Figure 2.25 RF characteristics of the new process samples (device size is 2x200 μm biased for maximum Gm at V_{DS} = 1.5 V).

2-7 Conclusions

In conclusion, a class of new high breakdown low leakage devices has been developed and characterised for use in the design of low noise amplifiers in the low SKA frequency band.

Two different processes have been applied for our in-house fabricated 1 μm strained gate InGaAs/InAlAs InP-based pHEMTs.

The old process devices of thin gate metallization (150 nm) have been demonstrated to exhibit the highest reported off-state breakdown voltage and the lowest on-state leakage current. A sharply defined pinch-off and very high transconductances with small amount of kink-effect in the common-source IV characteristics have been observed for these devices. Also, a much higher cut-off frequencies were measured for the InP-based devices compared with GaAs-based ones (in Appendix-D) and both exhibited relatively low f_{max} values due the parasitic effects associated with this process.

The InP-based pHEMTs kept their good DC and RF characteristics in the new process of thick gate metallization (450 nm) with higher f_{max} levels suffering much less parasitic effects, compared with the old process samples, making them the best candidates for low noise applications in the low SKA frequency band.

CHAPTER-3

Noise Characterization and Fundamentals of LNAs

3-1 Introduction

Noise is a phenomenon inherent to any electronic system. It is especially of particular concern in communication systems where small signals are received in the midst of noise. Usually, noise power results from random processes such as flow of charges or holes in an electron tube or solid-state device, propagation through the ionosphere or other ionized gas, or most basic of all, the thermal vibrations in any component at a temperature above absolute zero.

Noise can be passed into microwave system from external sources, or generated within the system itself. In either case the noise level of a system sets the lower limit on the strength of a signal that can be detected in the presence of noise. Thus, it is generally desired to minimize the residual noise level of a radar or communications receiver, to achieve the best performance. In some cases, such as radiometers or radio astronomy systems, the desired signal is actually the noise power received by the antenna, and it is necessary to distinguish between the received noise power and the undesired noise generated by the receiver system itself **[69]**. This chapter emphasis the noise characterization in microwave circuits, explaining the basic concept of noise, different

types of noise associated with semiconductor devices, noise parameters, and different techniques used in noise measurements. Also, the fundamentals of low noise amplifiers, their basic parameters, different topologies, and advances have been done up to now in their design will be discussed.

3-2 Noise Definitions

The word **noise** is always referred to any undesired excitation on the system. In other contexts, noise is also used to refer to signals or excitations which exhibit chaotic or random behavior. There are many definitions for electronic noise given in standard scientific literature but they are all based on the same meaning that is the unwanted disturbances or fluctuations, usually irregular, superposed upon the useful signal that tend to obscure its information content and usually produced by other services called interference. The origin of noise can be either internal or external to the system **[70]**.

3-2-1 Intrinsic noise

The internal, also known as intrinsic, noise is the noise generated inside the investigated device or circuit. Intrinsic noise shows up at all frequencies and once it is present in a circuit nothing can be done to filter it out, because its spectrum extends to very high frequencies, usually beyond the frequency of any actual useful signal. The amplitude of the intrinsic noise is usually very small and does not exceed a fraction of mille volt.
According to their physical origin, there are many different types of intrinsic noise like thermal, shot, flicker, diffusion noise and others. One of the most important features of intrinsic noise is its randomness which means that it is difficult to predict the amplitude of a fluctuating voltage or current and hence a statistical description is required to describe it. As for the frequency spectrum, the intrinsic noise may be found in some different forms such as **white** noise with a flat power spectral density. In other words, the signal's power spectral density has a uniform distribution in any band having a given centre frequency and bandwidth. White noise is considered analogous to white light which contains all frequencies.

Pink (1/f) noise is a signal with a frequency spectrum such that the power spectral density is proportional to the reverse of the frequency. The name arises from being intermediate between white noise ($1/f^0$) and **Red** noise ($1/f^2$).

3-2-2 Extrinsic noise

The external, extrinsic, noise is that generated outside the system under investigation. Usually it is the noise picked up from the environment surrounding the circuit which acts only as a receiving antenna and thus this type of noise may be called extraneous or spurious signals. According to its nature the extrinsic noise is classified into two main categories.

- **Environmental perturbations** including sky noise (Sun and Milky Way), atmospheric noise (lightning discharges in thunderstorms), and human-made noise (electric motors, arc welding, power lines, radio and TV broadcast, switches, cellular telephones, household appliances, etc.)
- **Crosstalk noise** which is the noise produced due to the interference (coupling) between different components in the same system. Such coupling can be reduced by modifying the relative position of various components in the circuits, but in some cases it is unavoidable.

Although the amplitudes of the extrinsic noise signals are always relatively high they have a much more restricted spectrum; this enables to avoid their effect either by inserting the appropriate rejection filters or to shift the band of the useful signal outside their spectrum.

3-3 Physical Noise Sources

Intrinsic noise is usually generated by random motion of charge carriers in devices and materials. Such motions can be caused by several mechanisms leading to various types of noise.

3-3-1 Thermal (Johnson) noise

It is the most basic type of noise; it arises from thermal vibrations of conduction electrons and holes due to their finite temperature. Some of the vibrations have spectral

content within the frequency band of interest and contribute noise to the signals. The noise spectrum produced by thermal noise is nearly uniform over RF and microwave frequencies (white). Thermal noise is also known as Nyquist noise and can be modeled by a noisy resistor R_N, connected to the input of the amplifier circuit, and the noise is generated inside this resistor by random fluctuation of charge carriers (electrons) due to thermal agitation **[71]**. The noisy resistor is represented by means of identical noiseless resistor series with lumped external noise voltage source (v_n) or parallel with external noise current source (i_n), where,

$$\overline{v_n^2} = 4kTR\Delta f \quad (3.1)$$

$$\overline{i_n^2} = 4kT\Delta f/R \quad (3.2)$$

$$P_n = kT\Delta f \quad (3.3)$$

In these equations:-

$\overline{v_n^2}$, $\overline{i_n^2}$ ----- Noise voltage and current spectral densities

P_n---------- Available noise power

k---------- Boltzmann's constant equals to 1.38×10^{-23} J/K

T---------- Resistance noise temperature in Kelvin

Δf----------Noise bandwidth in Hertz

It must be noted that the available thermal noise power is independent of the magnitude of the resistor value but, actually, the amount of noise power delivered to a load resistor depends on the degree of matching between source and load resistors. Most dissipative elements in electrical systems are very well characterized as ideal kTB noise power source over the microwave and millimeter-wave frequencies.

3-3-2 Diffusion noise

The physical origin of diffusion noise is the charge carriers' velocity fluctuations (random scattering) caused by collisions during the diffusion process from higher to lower carrier density regions. It is white noise observed in device regions that exhibit non-uniform carrier distribution or non-ohmic characteristics. A typical example of diffusion noise is the channel of the FET/MESFET if the transistor operates in the saturation region, where Ohm's law is no longer valid.

3-3-3 Shot (Schottky) noise

Firstly discovered by Schottky, the shot noise is generated by random fluctuations of charge carriers in the modulating channel due to their discrete nature. So, Shot noise is proportional to the random number of electrons crossing a potential barrier at any instance and is especially associated with current carrying active devices. Shot noise can be represented as:

$$\overline{i_{n,shot}^2} = 2qI_o \Delta f \qquad (3.4)$$

I_o is the DC current through the device. Unlike thermal noise, shot noise doesn't depend on temperature it only depends on the DC current flowing through the device and so it can be easily controlled by modifying the bias current level.

3-3-4 Flicker (1/f) noise

Flicker noise is a type of electronic noise with a 1/f, or pink spectrum. In semiconductors this noise is mostly due to random trapping and de-trapping of charges and associated changes in carrier mobility due to Coulombic scattering. Flicker noise power varies inversely with frequency, and so is often called 1/f noise. Flicker noise is often characterized by the corner (knee) frequency, Fc, the frequency at which 1/f power equals kTΔf. Usually the flicker noise is not important in the design of microwave amplifiers because the knee frequency of transistors is below 100 MHz but it is an important source of phase noise in microwave oscillators **[72]**.

3-3-5 Generation-Recombination (G-R) noise

G-R noise is that type of electronic noise caused statistically by fluctuations in the generation and recombination rates of thermally and optically generated carriers. The continuous trapping and de-trapping of the charge carriers causes a fluctuation in the number of carriers in the conduction and valence bands contributing more G-R factors. Crystal lattice defects, including impurity atoms or molecules contaminating the surface of semiconductor during fabrication, act as carrier traps increasing the generated noise **[73]**. G-R noise is not significant in highly doped semiconductors, since the conductance is mainly determined by carriers released from impurity atoms dominating those that are thermally or optically generated. However, current transport through regions where

carrier concentrations are relatively low (intrinsic and lightly doped semiconductors, and space charge layer of every junction) are adversely affected by G-R noise.

3-3-6 Other types of noise

Actually there are a few other types of intrinsic noise, but they are often insignificant relative to the stated noise sources like Quantum noise which results from the quantized nature of charge carriers and photons, Burst (Popcorn) noise that may be associated with shallow heavily doped emitter junctions of BJTs, and Avalanche noise which is a result of the process of carrier multiplication due to impact ionization in a reverse-biased PN-junctions.

3-4 Noise Representation

The noise generated by an electronic circuit can be represented in many different ways; in this section a discussion of the most commonly used forms for expressing the noise of any noisy system is presented.

3-4-1 Noise parameters

The noise performance of any linear network can be represented in three different but related ways: noise factor (Fn), noise figure (NF) and equivalent noise temperature (Te); these properties are definable as a simple ratio, decibel ratio or temperature, respectively.

3-4-1-1 Noise factor (figure)

When noise and a desired signal are applied to the input of a noiseless network, both noise and signal will be amplified or attenuated by the same factor, so that the signal-to-noise ratio (SNR) will be unchanged. But if the network is noisy, the output noise power will be increased more than the output signal power, so that the output SNR ratio will be reduced [25]. A concept created to characterize this degradation in the output signal-to-noise ratio (the internally generated noise of a system) is known as the noise factor, F_n.

$$F_n = \frac{S_i/N_i}{S_o/N_o} = \frac{N_o}{GkT\Delta F} \tag{3.5}$$

While S_i/N_i and S_o/N_o are the input and output signal-to-noise ratios of the system, N_o is the available noise power at the output and G is the available gain of the network over the bandwidth ΔF. If Na is the noise power added by the system then:

$$F_n = \frac{GkTB + Na}{GkT\Delta F} = 1 + \frac{Na}{GkT\Delta F} \qquad (3.6)$$

The noise figure (NF) is the noise factor represented in decibel notation and it is the commonly used form to express the noise performance of a network.

$$NF = 10\ Log_{10}(F_n) \quad dB \qquad (3.7)$$

A component which contributes no noise to the system has F_n = 1or NF = 0 dB.

3-4-1-2 Noise temperature

The noise added by a system is frequently described by the effective input noise temperature, T_e, which can be defined as the temperature of a fictitious additional source resistance at the system input that produces the same noise power at the system output as does the system to be characterized assuming the system itself is noiseless, Figure 3.1.

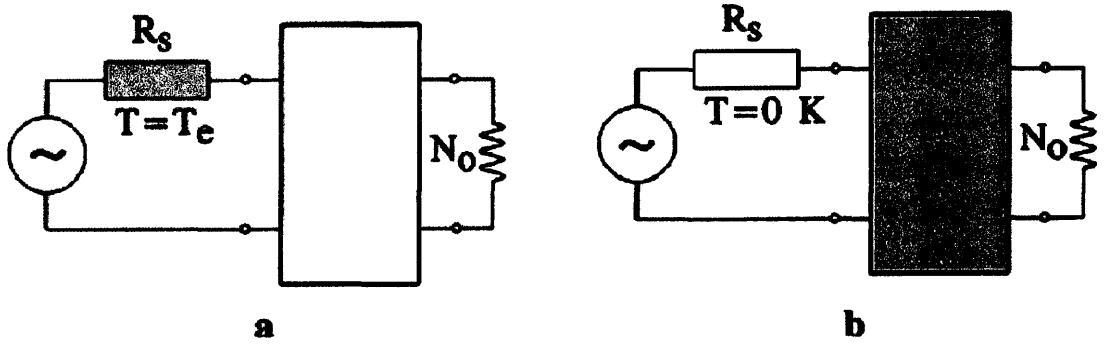


Figure 3.1 Equivalent noise temperature definition.

$$N_o = GkB\ (T_o + T_e) \qquad (3.8)$$

The noise factor (figure) and the noise temperature T_e of the system are related by:

$$F_n = 1 + \frac{T_e}{T_0} \geq 1 \quad \text{OR} \quad NF = 10Log_{10}\left(1 + \frac{T_e}{T_0}\right) \geq 0\ (dB) \qquad (3.9)$$

It must be noted that the equivalent input noise temperature does not depend on the temperature of the source (Ts), but only the source internal impedance (which determines the available gain G).

3-4-2 Noise performance of a cascaded system

Usually in a typical microwave system, the input signal travels through a cascaded network sections, each of them may degrade the signal-to-noise ratio to some degree. If the noise figures (temperatures) of the individual stages are known, then the noise figure (temperature) of the cascade connection can be determined. For N-stages cascaded in series with gain values G_i, noise factors F_i, and noise temperatures T_i, then the total noise factor and temperature of the N-stage system are given by the following expressions:

$$F_{Total}=F_1+\sum_{I-2}^{N}\frac{F_I-1}{G_1G_2.....G_{I-1}} \tag{3.10}$$

$$T_{Total}=T_1+\sum_{I-2}^{N}\frac{T_I}{G_1G_2.....G_{I-1}} \tag{3.11}$$

If the N stages are equal in gain and noise figure, as $n \rightarrow \infty$, the overall noise figure obtained is called the noise measure F_M, given by:

$$F_M = \frac{F-1/G}{1-1/G} \tag{3.12}$$

Usually the noise performance of the first stage is the most critical and so it should be chosen with the lowest possible noise and as much gain as possible (for amplifier applications).

3-4-3 Noise representation of noisy tow-port network

The circuit theory of linear noisy networks shows that any noisy two-port can be modeled by a noise equivalent circuit which consists of the original two-port (assumed to be noiseless) and two additional noise sources **[74, 75]**. There are many equivalent representations for noisy two-ports, but only three of them are required for common applications, those are the impedance, admittance and ABCD-parameters representations, shown in Figures 3.2a,b,c respectively. The effects of the noise sources are represented by the external noise-voltage/current sources V_{Ni} and I_{Ni}, placed in

series/parallel with the input and output terminals, respectively. Those sources must produce the same noise voltage/current at the circuit terminals as the internal noise sources. The representation of the noisy tow-port network requires four complex parameters (Z-, Y-, or ABCD-Matrix) to describe the passive but hypothetical noise-free tow-port, and two real parameters corresponding to the equivalent noise generators. Since these generators are always partially correlated, the correlation coefficient is a complex quantity; hence, the noise of a two-port can be represented by four real parameters.

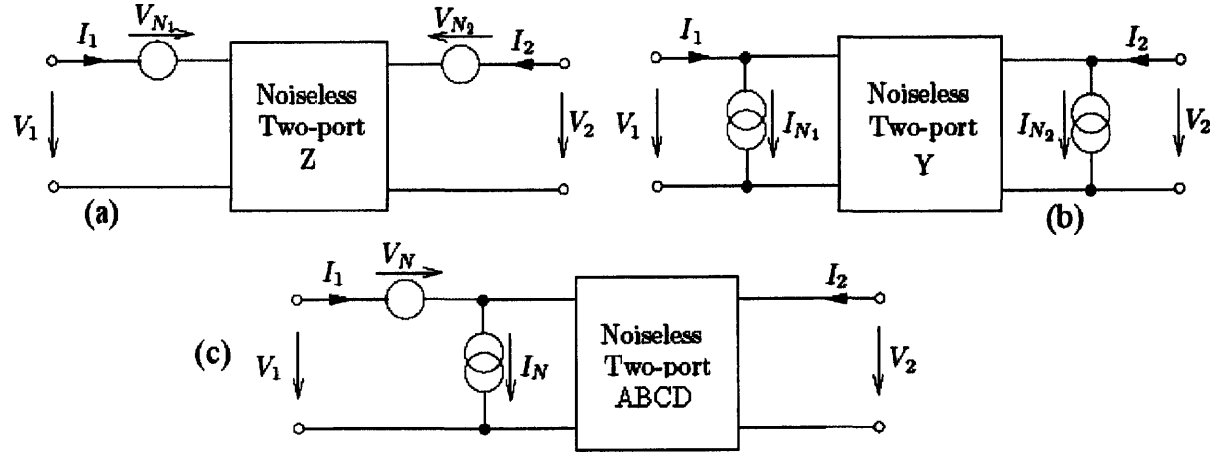


Figure 3.2 Different representations of a noisy two-port (a) Impedance. (b) Admittance. (c) Chain (ABCD).

These representations of the noisy two-port network can be mathematically expressed as:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + \begin{bmatrix} V_{N1} \\ V_{N2} \end{bmatrix} \tag{3.13}$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} I_{N1} \\ I_{N2} \end{bmatrix} \tag{3.14}$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} + \begin{bmatrix} V_N \\ I_N \end{bmatrix} \tag{3.15}$$

Starting with this group of equations, following a complicated mathematical regime, found in **[76, 77]**, one can derive an expression for the noise figure in terms of group of parameters that are commonly used to characterize any noisy device.

$$F=F_{min}+4r_n\frac{\left|\Gamma_S-\Gamma_{opt}\right|^2}{\left|1+\Gamma_{opt}\right|^2\left(1-\left|\Gamma_S\right|^2\right)} \tag{3.16}$$

In this equation, Γ_{opt} is the optimum input (source) reflection coefficient that results in minimum noise figure. F_{min} is the minimum noise figure, obtained when $\Gamma_S = \Gamma_{opt}$ and r_n is equivalent noise resistance normalized to the reference impedance of the system (usually 50 Ω).

Actually the noise resistance, R_n, plays a very important role in the process because it measures the level of noise factor deterioration with increasing mismatch. A small R_n value is always preferred because it indicates a relatively insensitive system in terms of noise level variations, and also measures how close F is to F_{min}.

Generally for good noise performance, it is desired to have low Fmin, small R_n, and close proximity between Γ_S & Γ_{opt} but these can be quite difficult to achieve over large bandwidths.

The quantities F_{min}, r_n, Γ_{opt} are known as the standard noise parameters of the device. They are frequency and bias dependent and always given by the manufacturer data sheets or can be measured and extracted experimentally as is the case in this work.

3-5 Noise Characterization in HEMTs

All semiconductor devices exhibit the basic noise mechanisms discussed before in different ways according to their features and physical properties. III-V compounds generate less thermal noise than Si due their higher electron mobilities. MESFETs exhibit higher noise levels compared with HEMTs due to strong ionized impurity scattering in the doped channel and the consequent degradation of drift mobility. HEMTs offer high electron density together with high electron mobility, making them least susceptible to intrinsic noise. Also, the availability of low resistance ohmic contacts minimizes the thermal noise contribution of parasitic elements. This section focuses on the physical aspects of noise in HEMTs and describes modern noise models developed

to predict noise characteristics and estimate the effect of certain device parameters on the overall system noise.

3-5-1 Noise sources in HEMTs

As in any semiconductor device, there are five dominant noise mechanisms in HEMTs: thermal noise, diffusion noise, shot noise, G–R noise, and flicker noise. These noise sources can be described as following:-

(a) Thermal noise, generated by the parasitic resistances of source, drain, and gate.

(b) Channel noise, which is essentially thermal if the device is operating in the linear mode, or diffusion noise in the saturation mode.

(c) G-R input noise due to carrier tunneling through the Schottky barrier and electron-hole pair generated in the space-charge and intrinsic regions or by impact ionization.

(d) The flicker noise, which shows up primarily at frequencies lower than 1MHz, is often disregarded, since most HEMT devices are dedicated to microwave applications. Nevertheless, there are at least two situations in which 1/f noise still affects microwave circuit operation by means of side-effects like up-conversion occurring in mixers and the phase noise of HEMT oscillators **[78]**.

(e) Shot noise due to the reverse biased gate current **[79]**.

3-5-2 FET/HEMT noise modeling

The noise performance of the FETs has been studied by many researchers in the literature and all try to predict the noise performance of the devices by extracting the four basic noise parameters, discussed before, over a wide frequency range under different bias conditions. The first FET noise model was presented by Van der Ziel in the early 1960s **[80]** for a planar JFET made of p-type material with one-dimensional channel operating in the linear mode. After then, more sophisticated models emerged from the Van der Ziel theory and adapted to MESFETs and HEMTs with the most important model proposed by Pucel and his co-workers in 1972 **[81]**. The Pucel modeling takes into account velocity saturation and how the noise changes with bias based on changes in the small-signal parameters and their noise variables P, R, and C.

3-5-2-1 Fukui's model [82]

Fukui garnered much attention in the late 1970s with the introduction of his empirical noise model. Although it involved empirical parameters, directed mainly for GaAs MESFETs, it was expressed directly in terms of the noise parameters, and made clear how key small-signal parameters contributed to the noise performance. The model is also convenient because the noise at different frequencies and device scaling can be easily determined. Fukui's expressions for the noise parameters are:-

$$NF_{min} = 10Log\left(1 + k_1 \frac{f}{F_T}\sqrt{Gm(Rs + Rg)}\right) \tag{3.17}$$

With

$$F_T = \frac{G_m}{2\pi C_{gs}} \tag{3.18}$$

Then

$$NF_{min} = 10Log\left(1 + k_1 f C_{gs}\sqrt{\frac{Rg + Rs}{Gm}}\right) \tag{3.19}$$

$$R_n = \frac{k_2}{G_m^2} \tag{3.20}$$

$$R_{opt} = k_3\left[\frac{1}{4G_m} + R_g + R_s\right] \quad \text{and} \quad X_{opt} = \frac{k_4}{fC_{gs}} \tag{3.21}$$

In these equations; F_T is the unity current gain cut-off frequency, R_{opt} & X_{opt} are the real and imaginary parts of the optimum source impedance. The variables k1–k4, are fitting parameters that depend on the material system used or the device technology (for GaAs MESFETs $k_1 \approx 2.5$ and $k_2 \approx 0.03$).

Hence all noise parameters can be determined from basic semiconductor characteristics making the model extremely attractive when developing new materials and devices.

3-5-2-2 Pospieszalski's model [83]

In the late 1980's, Pospieszalski introduced a new noise figure model that took a different approach than the previous methods by removing correlation between the noise sources and including only two frequency-independent fitting coefficients. In this model, there are only two (uncorrelated) noise sources for the entire transistor: thermal noise of the intrinsic gate resistance, R_i, defined by an effective noise temperature T_g and the thermal noise of the drain-source resistance, R_{ds}, expressed by a temperature

T_d. T_g is usually (but not always) close to room temperature, while T_d can be several thousand degrees Kelvin. With T_a the ambient temperature, the noise parameters of Pospieszalski's model are given by the following expressions:-

$$F_{min}=1+2\left(\frac{f}{F_T}\right)\frac{R_i T_d}{R_{ds} T_a}+\frac{2f}{F_T T_a}\sqrt{\frac{R_i T_g T_d}{R_{ds}}+\left(\frac{f}{F_T}\right)^2\frac{R_i^2 T_d^2}{R_{ds}^2}} \tag{3.22}$$

$$R_n=\frac{T_g R_i}{T_a}+\frac{T_d}{T_a R_{ds} G_m^2}\left(1+w^2 C_{gs}^2 R_i^2\right) \tag{3.23}$$

$$R_{opt}=\sqrt{\left(\frac{F_T}{f}\right)^2\frac{T_g R_i R_{ds}}{T_d}+R_i^2} \qquad \text{and} \qquad X_{opt}=\frac{1}{wC_{gs}} \tag{3.24}$$

Only the fitting factors T_g and T_d, need to be determined from measurements. If these noise coefficients are known as well as the small-signal model parameters of the transistor, all noise parameters can be easily calculated using the above expressions.

3-5-2-3 Cappy's model [84]

This is a one-dimensional physical model developed by Cappy in the late 1980's. In this model, general method used in noise analysis is presented, including the calculation of the gate and drain noise sources and their correlation coefficient, as well as the calculation of the noise figure and the other noise parameters.

$$F_{min}=1+2\sqrt{P}\frac{f}{F_T}\sqrt{G_m\left(R_S+R_G\right)} \tag{3.25}$$

$$\frac{1}{R_n}=PG_m\left(\frac{f}{F_T}\right)^2 \tag{3.26}$$

$$R_{opt}=\sqrt{\frac{G_m\left(R_S+R_G\right)}{P}}\frac{1}{wC_{gs}} \qquad \text{and} \qquad X_{opt}=-\frac{1}{wC_{gs}} \tag{3.27}$$

$$P=\frac{I_{DS}}{E_C L_g G_m} \tag{3.28}$$

In these expressions; E_C is the critical field of an idealized V-E relationship, L_g is the gate length, and I_{DS} is the drain current.

The main advantages of this model are the easy calculation of all noise parameters and the deep understanding of how the electrical and technological parameters influence the noise performance of any device.

3-6 Noise Measurements

Modern receiving systems must often process very weak signals, but the noise added by the system components tends to obscure those very weak signals. Sensitivity, bit error ratio (BER) and noise figure are system parameters that characterize the ability to process low-level signals. Of these parameters, noise figure is unique in that it is suitable not only for characterizing the entire system but also the system components such as the pre-amplifier, mixer, and IF amplifier that make up the system. By controlling the noise figure and gain of system components, the designer directly controls the noise figure of the overall system. Once the noise figure is known, system sensitivity can be easily estimated from system bandwidth. Noise figure is often the key parameter that differentiates one system from another, one amplifier from another and one transistor from another. Such widespread application of noise figure specifications implies that highly repeatable and accurate measurements between suppliers and their customers are very important. The reason for measuring noise properties of networks is to minimize the problem of noise generated in receiving systems **[85]**. Noise measurements are essential for assuring that the added noise is minimal. Many different techniques used for noise measurements are described here.

3-6-1 Y- Factor method

The Y-Factor method is the basis of most noise figure measurements whether they are manual or automatically performed internally in a noise figure analyzer. Using a noise source, this method allows the determination of the internal noise in the DUT and therefore the noise figure or effective input noise temperature. The used noise source can have two different levels of noise output power N_C, N_H corresponding to two different noise temperatures T_{cold} and T_{Hot}. Gas discharge tubes and avalanche diodes are the most commonly used noise sources. The manufacturers of such sources always specify a term denoted ENR, the excess noise ratio, defined as:-

$$ENR = 10\log\left(\frac{T_{Hot}}{T_{Hot}+T_{Cold}}\right) \quad (3.29)$$

The ratio between the two different output noise powers N_H and N_C, corresponding to switching the noise source ON and OFF, is defined as the Y-factor (Y). The noise factor, F, can be calculated using the following expression:-

$$F = \frac{ENR}{Y-1} \quad (3.30)$$

It should be noted that the above parameters are in linear units. Normally the ENR provided on the noise sources is in dB, so, it should be converted into linear for calculating F.

The power detector used to make this measurement may be a power meter, spectrum analyzer, Figure 3.3, or a special internal power detector in the case of noise figure meters and analyzers. The main advantages of this technique are its simplicity as the equipments required are only noise source and power meter and the noise figure measurements can be done over a wide range of frequency. Finally, the absolute power level accuracy of the measuring device is not important since a ratio is to be measured **[86]**.

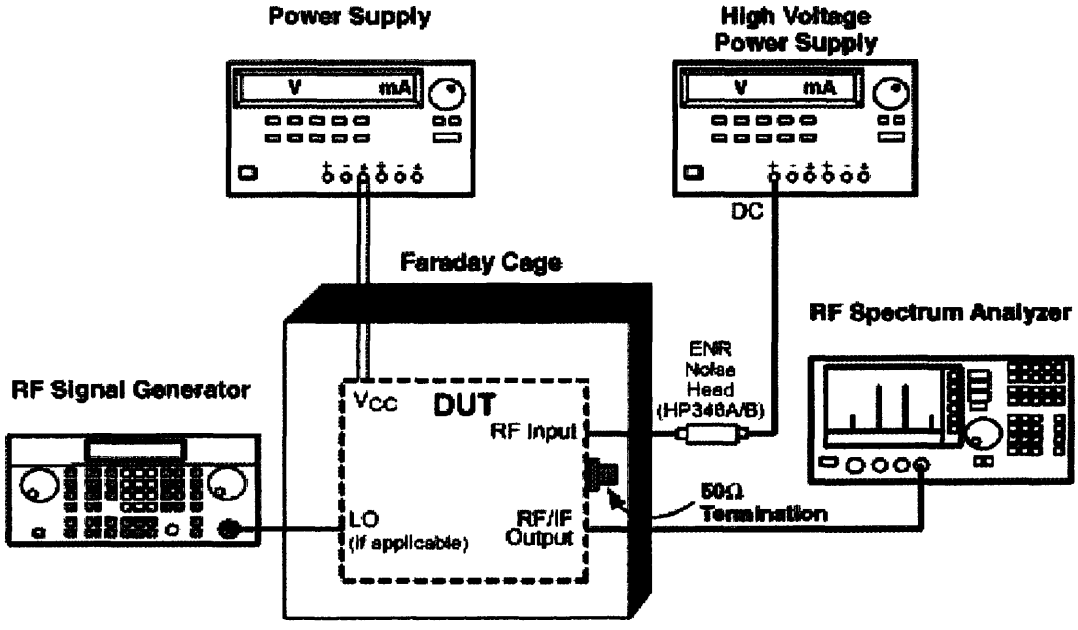


Figure 3.3 Practical setup for noise temperature measurements by Y-Factor method [87].

3-6-2 Gain method

This method involves more measurements as well as calculations, but under certain conditions, it turns out to be more convenient and more accurate. The gain method is based on the noise factor definition given earlier, as the ratio between the total output noise power and the output noise due to input source only.

At room temperature (290 K), the noise power density P_{NAD} = **-174dBm/Hz**. Thus we have the following equation **[87, 88]**:-

$$NF = P_{NOUT} - (-174dBm/Hz + 20 * \log_{10}(BW) + Gain) \quad (3.31)$$

In the equation, P_{NOUT} is the measured total output noise power. To make the formula simpler, the output noise power density (in dBm/Hz) can be directly measured, and the equation becomes:

$$NF = P_{NOUTD} + 174dBm/Hz - Gain \quad (3.32)$$

To use the "Gain Method" to measure the noise figure, the gain of the DUT needs to be pre-determined. Then the input of the DUT is terminated with the characteristic impedance (50 for most RF applications, 75 for video/cable applications). Then the output noise power density is measured with a spectrum analyzer.

3-6-3 Noise-Figure meter method

The noise figure meter generates a 28V DC pulse signal to drive a noise source which generates noise to drive the DUT. The output of the DUT is then measured by the noise figure analyzer. Since the input noise and Signal-to-Noise ratio of the noise source is known to the analyzer, the noise figure of the DUT can be calculated internally and displayed. For certain applications (mixers and receivers), a LO signal might be needed, as shown in Figure 3.4. Also, certain parameters need to be set up in the Noise Figure Meter before the measurement, such as frequency range, application (Amplifier/Mixer), etc. Using a noise figure meter is the most straightforward way to measure noise figure. In most cases it is also the most accurate. The noise figure over a certain frequency range can be measured, and the analyzer can display the system gain together with the noise figure to help the measurement. A noise figure meter also has limitations. The analyzers have certain frequency limits. For example, the Agilent N8973A works from 10MHz to 3GHz. Also, when measuring high noise figures, e.g., noise figure exceeding

10dB, the result can be very inaccurate. Finally, this method requires very expensive equipment.

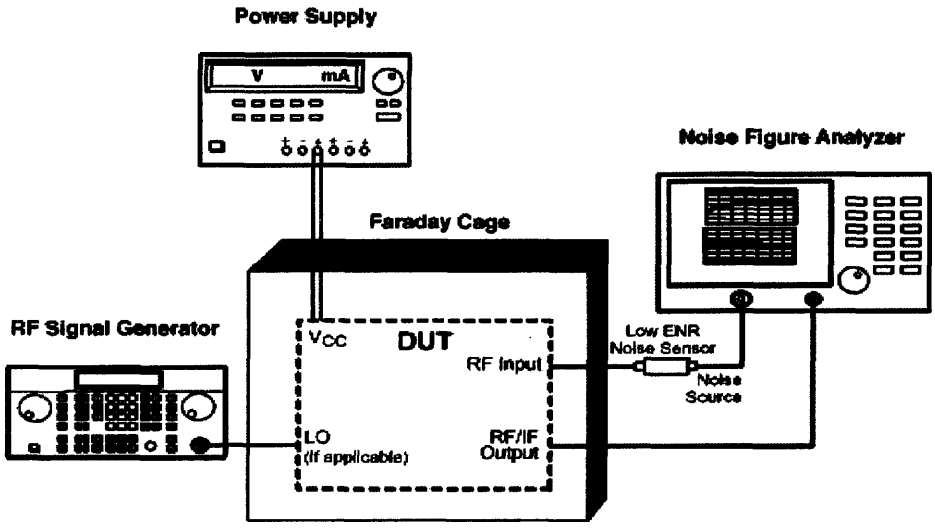


Figure 3.4 Noise measurements by noise figure analyzer [87].

A comparison between all mentioned noise measurement techniques is summarized in table 3.1.

	Applications	Advantages	Disadvantages
Y-Factor Method	Wide range of NF	Can measure wide range of NF at any frequency regardless of gain.	When measuring very high NF, error could be large.
Noise Figure Analyzer	Super low NF	Convenient, very accurate when measuring super low (0-2dB) NF.	Expensive equipment, frequency range limited.
Gain Method	Very high gain or very high NF	Easy setup, very accurate at measuring very high NF, suitable for any frequency range.	Limited by spectrum analyzer noise floor. Can't deal with systems with low gain and low NF.

Table 3.1 Comparison between noise measurement techniques.

3-6-4 practical considerations in noise figure measurements

To achieve accurate and repeatable noise figure measurements, the following precautions must be taken into account during experiments **[89, 90]**:-

- Select the appropriate noise source
- Minimize extraneous signals.
- Minimize mismatch uncertainties.
- Use averaging to minimize display jitter.
- Avoid non-linearities.
- Account for mixer characteristics.
- Use proper measurement correction.
- Choose the optimal measurement bandwidth.
- Account for path losses.
- Account for the temperature of the measurement components.
- For double-side band measurements, choose an IF that provides equal gain for both upper and lower side bands.

3-7 Fundamentals of Low Noise Amplifiers

The interest in microwave techniques for communication systems has grown immensely over recent years, and the performance of microwave active and passive circuits for wireless systems technology has become extremely advanced. One of the most critical active circuits employed in systems applications is the microwave low noise amplifier (LNA).

Low noise microwave amplifiers, employing solid-state (semiconductor) devices, are extensively used in communication systems, radio telescopes, satellite earth stations, and radar systems. Since the LNA is the first circuit block in a receiver chain, its noise performance dominates the system's sensitivity. It determines the noise figure and input voltage standing wave ratio (VSWR) of the overall system as it is the first block that a signal fed from an antenna meets. In this section, a discussion of the fundamentals of low noise amplifiers, their basic parameters, different topologies, and advances have been done up to date in their design are presented.

3-7-1 Low noise amplifiers basic parameters

Like all microwave amplifiers, there are many parameters that should be taken into consideration when designing a LNA. The most important of these, are the power gain, stability, noise, linearity, and dynamic range.

3-7-1-1 Power Gain

A single-stage microwave transistor amplifier can be represented by the circuit shown in Figure 3.5, where a matching network is used on both sides of the active device. The input matching circuit transforms the input impedance to the source impedance Z_S (or to Z_{opt} in case of LNA) while the output matching circuit transforms the output impedance to the load impedance Z_L.

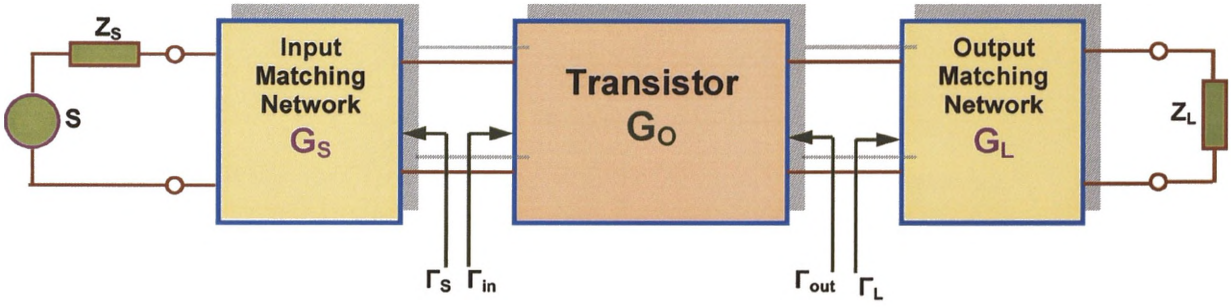


Figure 3.5 Linear active transistor amplifier.

The most useful gain definition for amplifier design is the transducer power gain, G_T, which is the ratio of the power delivered to the load to the power available from the source i.e.

$$G_T = \frac{P_L}{P_{AVS}} = \frac{|S_{21}|^2\left(1-|\Gamma_S|^2\right)\left(1-|\Gamma_L|^2\right)}{\left|(1-\Gamma_S S_{11})(1-\Gamma_L S_{22})-\Gamma_S\Gamma_L S_{12}S_{21}\right|^2} \qquad (3.33)$$

It should be noted that this gain definition accounts for the source and load mismatch, i. e. if the amplifier network is perfectly matched at the input and output ports ($\Gamma_L = \Gamma_S = 0$), then

$$G_T = |S_{21}|^2$$

Also, in this situation, a differentiation must be made between unilateral and bilateral amplifier networks, in the first one (the most common case), the reverse transmission

coefficient is insignificant (S_{12}= 0), i.e. it is assumed to have virtually no feedback, and in this case $\Gamma_{in}=S_{11}$, $\Gamma_{out}=S_{22}$, then the unilateral transducer power gain, defined as G_{TU}, can be written as:-

$$G_{TU} = \frac{1-|\Gamma_S|^2}{|1-\Gamma_S S_{11}|^2} |S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-\Gamma_L S_{22}|^2} = G_S G_0 G_L \qquad (3.34)$$

$G_0 = |S_{21}|^2$ is a parameter of transistors usually given in the manufacture's data sheets, and is fixed once the bias conditions of the transistor are chosen and remains invariant throughout the design. G_S, G_L are two quantities that represent the gain/loss produced by the matching/mismatching of the input and output networks respectively.

When the reverse transmission parameter, S_{12}, of the transistor is not significantly small, then a non-unilateral amplifier is produced. The non- unilateral transducer power gain is generally given by equation (3-34), but the maximum gain is achieved when the amplifier network is conjugately matched at both input and output ports, i.e. $\Gamma_S = \Gamma_{in}^*$, $\Gamma_L = \Gamma_{out}^*$.

3-7-1-2 Stability

The stability of an amplifier is its resistance to oscillate at any frequency under the DC bias conditions of interest. So care must be taken, in the design and fabrication of microwave amplifiers, because unavoidable parasitics in such high frequencies are often sufficient to start oscillations.

An active device (two-port network) is said to be unconditionally stable at a given frequency if both of its input and output impedances have a positive real part for any passive load and source terminations. In S-parameter terminology the device must satisfy all of the following conditions:-

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1$$

$$|S_{11}| < 1 \text{ and } |S_{22}| < 1$$

Where K is known as the Rollett's stability factor and Δ is the determinate of the S-Matrix. When one of the above statements is not satisfied, then the transistor is said to be potentially unstable (conditionally stable). In this case the transistor can still be used to perform as an amplifier provided the regions of source and load terminations that cause instability are avoided and those regions can be determined from the source and load stability circles' plots on Smith Chart.

3-7-1-3 Noise Figure

This is the most important parameter of concern during the design of a LNA. The noise figure expression given before in equation (3-16) defines a family of circles called constant noise figure circles. Each, when plotted on the Smith chart, represents the locus of source impedances (reflection coefficients) that give the same noise figures. The constant noise figure circles centers (C_F) and radii (R_F) are given by **[91]** :

$$C_F = \frac{\Gamma_{opt}}{1+N_i} \quad , \quad R_F = \frac{1}{1+N_i}\sqrt{N_i^2+N_i\left(1-\left(\Gamma_{opt}\right)^2\right)} \tag{3.35}$$

Where;

$$N_i = \frac{\left|\Gamma_S-\Gamma_{opt}\right|^2}{1-\left|\Gamma_S\right|^2} = \frac{F-F_{min}}{4r_n}\left|1+\Gamma_{opt}\right|^2 \tag{3.36}$$

It must be noted that for maximum power gain amplifier design Γ_S must be matched to Γ_{in}, while for minimum noise figure designs it should be matched to Γ_{opt}, and because Γ_{in} and Γ_{opt} are always different, it is not possible to obtain both minimum noise figure and maximum gain for the same amplifier circuit, so some sort of compromise must be made. This can be made by using constant gain circles and circles of constant noise figure to select a useable trade-off between noise figure and gain.

3-7-1-4 Linearity

The transfer characteristic of the amplifier is still linear up to a certain level of the input power. As the input power increases above this level, the transfer function becomes nonlinear i.e. the output power is lower than predicted by small-signal gain, in this case, the output signals of the amplifier suffer from harmonic distortion **[92]**.

(1) One dB compression point

The output power at which the gain has dropped by 1 dB below the linear gain is called 1-dB compression point P_{1dB}. Typically, the gain will drop rapidly for power above P_{1dB}, reaching a maximum or fully saturated output power within 3 to 4 dB above P_{1dB} as shown in Figure 3.6. Knowing the 1-dB compression point is a good measure to the nonlinearity behavior of the amplifier.

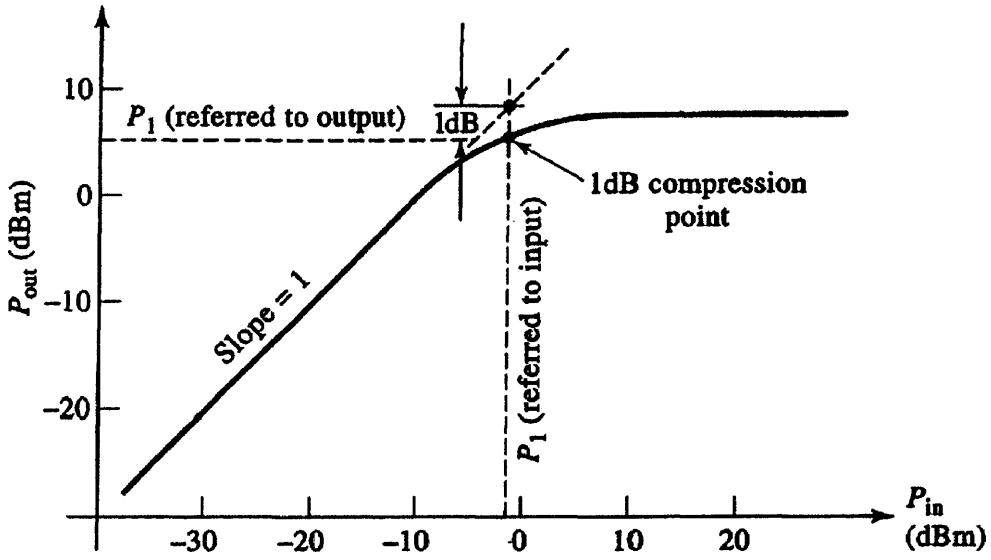


Figure 3.6 Illustrating the gain compression of a realistic amplifier.

(2) Third order intercepts

For every 1 dB increase in the input power, the first-order (linear) output power increases by 1 dB, while the third-order (cubic) output power increases by 3 dB. Plotting the line describing the third-order products (with slope 3) together with the linear first-order product line (with slope 1), both of them exhibit compression at high input power levels, but the extension of their idealized responses will intersect, typically at a point above the onset of compression, as shown in Figure3.7. This hypothetical intersection point, where the first-order and third-order output powers are equal, is called the third-order intercept point, denoted IP3 or TOI. Usually IP3 is referenced at the output of the amplifier and occurs at levels approximately 12-15 dB higher than the 1-dB compression point.

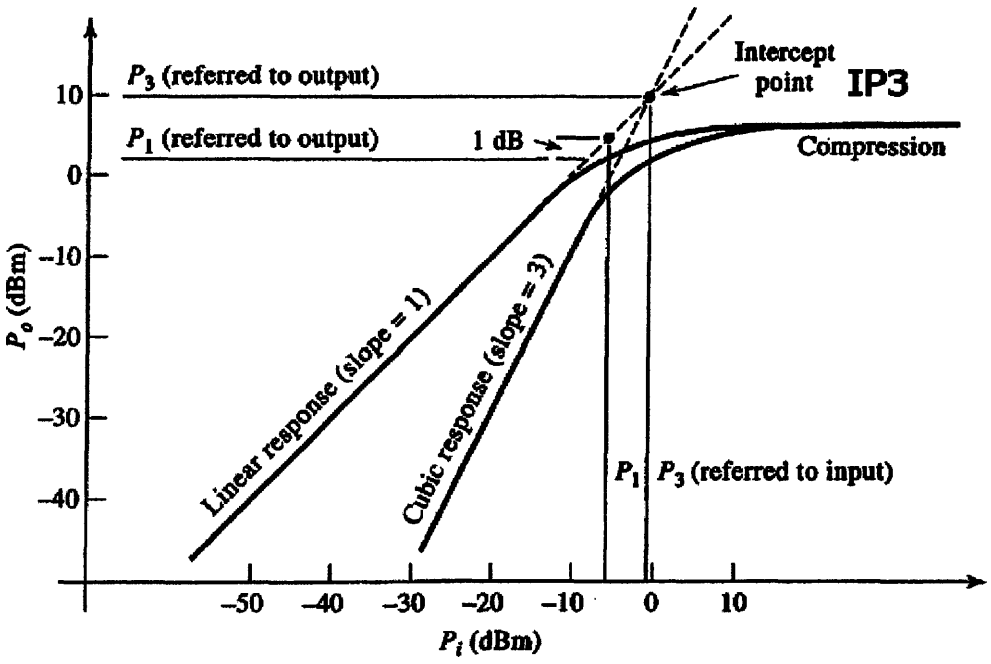


Figure 3.7 Definition of the third-order intercept point.

(3) Dynamic range

The range of an input signal that can be detected by a receiver without much distortion is called the dynamic range. The dynamic range (DR) of an amplifier is defined as the ratio of the 1-dB compressed output power to the minimum amplified detectable signal and this can be expressed mathematically as:

$$DR = P_{1dB} - P_{RFmin} \text{ (dB)} \tag{3.37}$$

3-7-1-5 Amplifier efficiency

In microwave engineering, the amplifier efficiency is defined by three different measures briefly will be discussed here.

(1) Drain efficiency

Drain efficiency gets its name from FET devices, as the primary terminal where DC power is input is the drain. Drain efficiency is the ratio of output RF power to input DC power:

$$\delta_{Drain} = \frac{P_{RFout}}{P_{DC}} = \frac{P_{RFout}}{V_{DC} x I_{DC}} \tag{3.38}$$

Drain efficiency is a measure of how much DC power is converted to RF power. The problem with this unit of measure is that it doesn't take into account the incident RF power that goes into a device. In the case of a single-stage RF amplifier, the RF input power can be substantial, because low gain levels.

(2) Power added efficiency (PAE)

Power added efficiency is similar to drain efficiency, but it takes into account the RF power that is added to the device at its input.

$$PAE = \frac{P_{RFout} - P_{RFin}}{V_{DC} x I_{DC}} \tag{3.39}$$

In a theoretical sense, an amplifier with infinite gain will have power added efficiency equal to drain efficiency. For a real amplifier, PAE will always be less than drain efficiency, but once you get to 30 dB of gain or so, the two quantities become very close in value because input power will be less than 1% of output power.

(3) Total efficiency

Total efficiency, sometimes called overall efficiency, gives a complete picture of the ratio of output power to both types of input power (DC and RF):

$$\delta_{Total} = \frac{P_{RFout}}{V_{DC} x I_{DC} + P_{RFin}} \tag{3.40}$$

Total efficiency is the measure that makes the most sense from a thermodynamic point of view, but PAE is still the most popular measure in the microwave community.

3-7-2 LNA design considerations

In designing a LNA, it is always required to obtain low noise, high gain, and low In/Out VSWR performances with adequate circuit stability, all over the frequency band of interest. Because of all these aspects, the design of the LNA is quite challenging. A successful LNA design may be achieved by certain technique consisting of a number of steps, briefly discussed here.

3-7-2-1 Choice of the circuit topology

The first step in designing the LNA is to decide which profile provides the best combination of features and performance.

For LNAs with common-source (CS) single gate (SG) FET, it is well known that the noise matching for achieving the NF_{min} results in high input VSWR, and vice versa **[93]**. This is because the optimum noise match source reflection coefficient, Γ_{opt}, is usually very different from the maximum available power gain match source reflection coefficient, G_{max}. So, some tradeoffs between the noise figure, the gain, and the input VSWR are needed. If, however, Γ_{opt} and G_{max} are coincident, NF_{min}, maximum power gain and low VSWR can be achieved simultaneously, but this is always very difficult.

Although negative feedback techniques for designing wide-band LNAs can be used to flatten the gain response, improve the input and output match/SWR, and improve the device's stability, this is always at the expense of gain level and noise performance **[92, 94]**.

One of the most efficient alternatives to the CS configuration is the cascode feedback configuration. In this technique, noise and the gain, and input/output matching can be simultaneously achieved with good stability and wide bandwidth by combining the inherent advantages of the cascode and resistive-shunt feedback. This technique is more suitable for monolithic form than for hybrid because the device impedance level can be chosen at will by changing the gate size, thus the high-quality feedback resistance is easily available **[93, 95, 96]**.

3-7-2-2 Choice of device size

The choice of device size is a critical step in designing a MMIC LNA. Device size will affect the LNA's bandwidth, DC power consumption, noise figure, and nonlinear performance.

While the effect of the gate length on the noise performance (NFmin) is great at high frequencies, it becomes much less pronounced at low frequencies (see Figure 3.8) **[97]** and so the 1μm devices still can be used at lower frequencies instead of the sub-micron devices that require the high cost of E-beam technology. Also, sub-micron devices always exhibit a high amount of instability at low frequency bands **[98]** and so they are more suitable for high frequency applications.

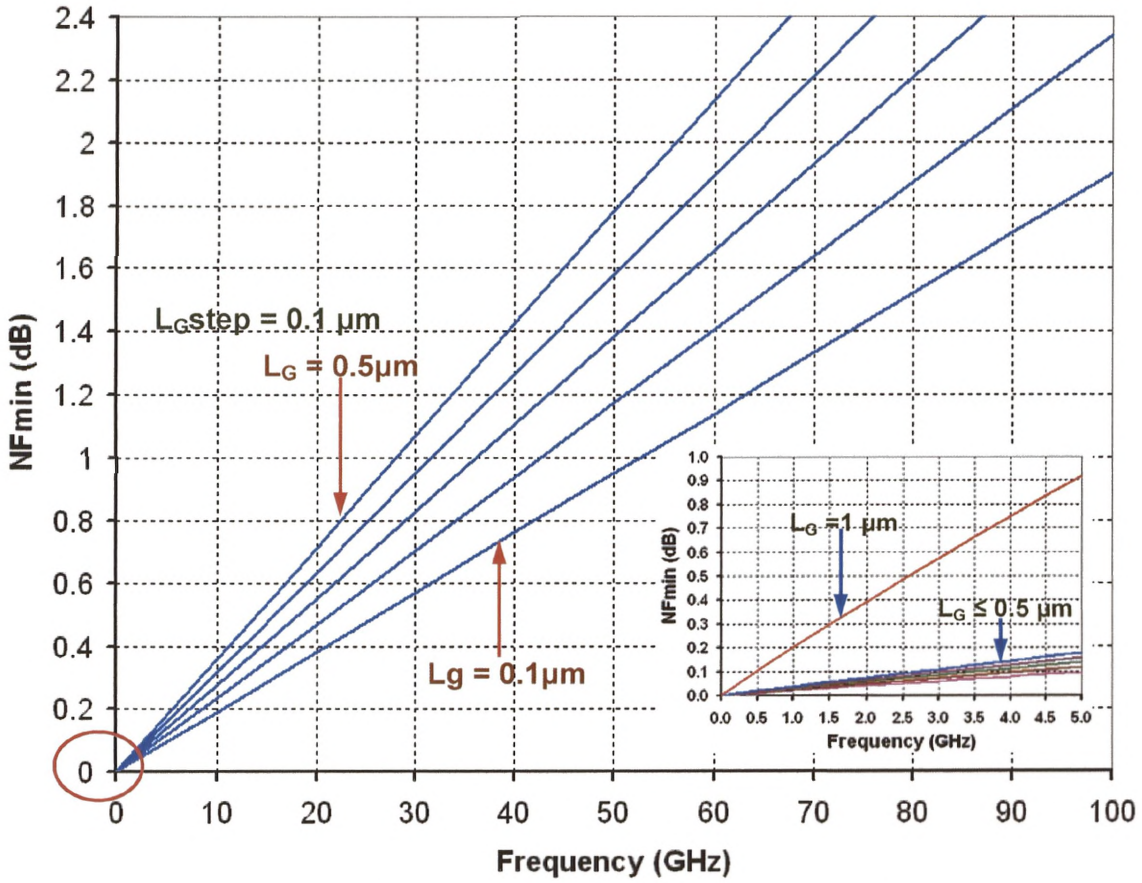


Figure 3.8 Modeled NFmin of InGaAs/InAlAs HEMT versus gate length [97].

On the other side, small gate widths are always preferred for reduced power consumption and higher amplifier efficiency. However, as the gate width gets smaller, resistive losses for matching circuits and interconnections will increase relative to the device impedance, effectively increasing the noise figure.

Also, it is well known that when a transistor has broad noise circles, tuning of the generator reflection coefficient to Γ_{opt} will be easier achieving noise figure close to NF_{min} and the design of the LNA will be much easier. Hughes, **[99]**, has derived an expression for the optimum gate width for a broad noise circles as a function of frequency showing that the optimum gate width is inversely proportional to frequency as illustrated in Figure 3.9.

The opposite trend in the evolution of NFmin and NF with the gate width is due to the change in the noise resistance of the devices. This parameter shows that at low

frequency (below 2GHz) the noise performance of the transistor is dictated by its noise resistance Rn rather by NFmin only. On the other hand, the gate metallization resistance, Rg, increases with increasing gate width and so does NFmin. Therefore, in order to reach ultra low noise at low frequencies, increasing the gate width together with keeping Rg low is a key requirement that can be achieved by employing multi gate-finger devices.

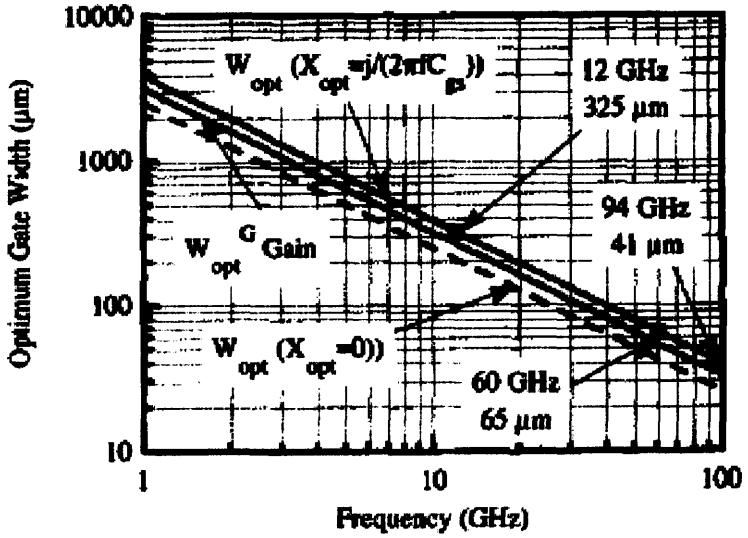


Figure 3.9 Plots of optimum gate widths for broadest noise circles (W_{opt}) and broadest gain circles (W_{opt}^{G}) versus frequency for a FET with Cgs of 1 pF/mm [99].

In addition to an increased noise figure and reduced gain as a device shrinks, there are other drawbacks in using too-small a device. These include nonlinear effects and susceptibility to interfering signals within the operating bandwidth due to poor IP3 performance. There is also a range of device sizes that is best suited for matching to 50-ohm systems. Devices smaller or larger than this optimal range will tend to reduce bandwidth, perhaps not a concern in narrowband applications but certainly important in more wide-band systems. Thus, the intuitive tendency to make the device as small as possible for reduced power consumption is tempered by other performance issues.

3-7-2-3 Choice of the DC bias point

The drain bias current affects the noise figure more than the drain voltage. Additionally, drain bias affects amplifier gain as the low current results in low gain. As a compromise

between gain and noise, LNAs are typically biased at 15 to 20 percent of the drain saturation current (IDSS). This trade off between gain and noise is less severe in HJ-FETs due to their broader range of bias for NF_{min} compared with the traditional MESFETs **[100]**. However, the designer must be very careful during the choice of the DC bias point and should not take the above rule as an axiom. The bias point should be investigated by plotting the I_{DS}-(NF_{min} &Gain) curves of the used device and then one can choose the optimum bias point suitable for the desired performance.

3-7-2-4 Design of In/Out matching networks

Once device size, bias current, and bias voltage have been chosen, the next step is to design the LNA's matching circuits. Nonlinear and linear device models or S-parameters are generally available for a typical device, but these are optimized for a specific device size, such as 300 μm. Errors increase as the device is scaled upward or downward, although it is often unclear how much the error increases due to this model scaling. Matching circuits are designed using a simulator and the appropriate device model. An iterative design flow is used to develop the LNA design along with the circuit layout, and various checks are performed along the way. Finally, layout design-rule checks (DRCs) are performed before sending the design out for fabrication.

3-8 Advances in LNAs Design

Because of their highly versatile circuit function, microwave LNAs have always been the first to benefit from developments in the device and semiconductor technologies. Over the last few decades, the technological revolution achieved in this expanding field not only resulted in improved devices, subsystems, and systems, but also enabled new markets to be developed such as the cellular market, Direct TV, satellite communications, Internet communications, etc.

Throughout this period, the low-noise concepts and techniques have been dramatically changed even in terms of the vocabulary used to express the LNAs. The most commonly used LNAs during the 1970s and 1980s were the parametric amplifiers (paramps), cryogenically cooled amplifiers, microwave amplification by stimulated emission of radiation (MASERS), thermoelectrically cooled (TE) amplifiers, field-effect

transistors (FETs), and bipolar junction transistors (BJTs). Okwit gives a very interesting historical review of these LNAs in **[101]**, and their state-of-the-art noise performance is shown in Figure 3.9.

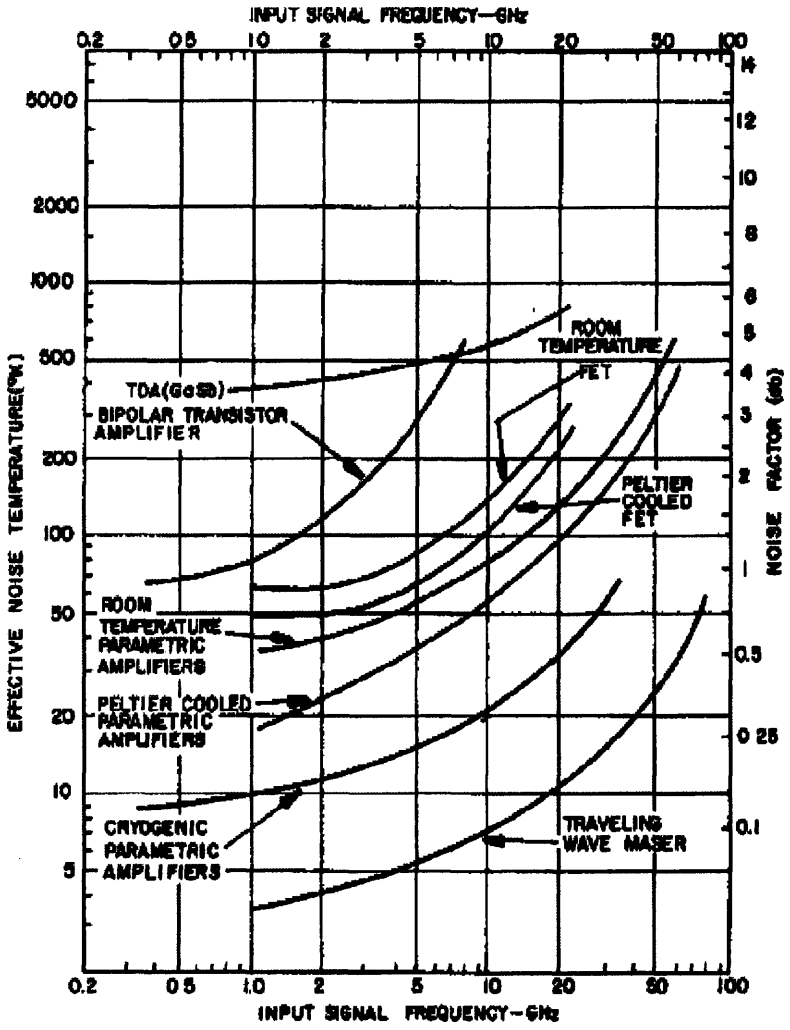


Figure 3.10 State-of-the-art noise performances of the 1980s LNAs [101].

While the performances of the LNAs were extremely good then, and convenient for the low-noise applications during that time, most of LNA circuits were large, heavy, expensive, and consumed a lot of power. Satellite ground terminals were one application where low-noise performance, light weight, low power, and high reliability were simultaneously required, but not always achieved until the development of three-

terminal devices that has continually lowered the noise threshold coupled with a significant reduction in size, weight, and power **[102]**.

The three-terminal revolution started a long time ago and has acquired an astonishing progress rate leading the world today to entirely new generations of low-noise concepts such as HEMTs, pHEMTs, InP-pHEMTs, HBTs, high-temperature superconductivity (HTSC), and expanding.

The most rapid advances in LNAs based on FETs and HJ-FETs, the main concern of this study, seem to have occurred between 1980 and 1995. Three different generations of low noise HJ-FETs have been introduced during that period; the first generation used AlGaAs/GaAs HEMTs, the second used InGaAs/AlGaAs pHEMTs, and the third generation the InP-based InGaAs/InAlAs pHEMTs. The continuous improvement in these technologies has led to better performance in noise temperature, gain, bandwidth, power dissipation, size, and reliability. Also, advances in optical lithography techniques have allowed an extensive use of these devices in the MMIC LNAs in the millimeter and sub-millimeter wave frequencies **[103]**, employing transistors with very short gate lengths down to 70 nm and ultra-high cut-off frequencies up to 600 GHz. As the devices improved, the achievable noise figures in the microwave and millimeter wave regions are continuously lowered due to the increase in transconductance (> 1000 mS/mm) and the reduction in parasitics. In addition, the devices can be cryogenically cooled and, therefore, extremely low-noise temperatures can be achieved **[104]**.

However, it is almost impossible to discuss all the advances that have been made in this field over the last three decades. For this reason, highlights of some of the most important achievements in the MMIC HJ-FETs LNAs that have been reported in the last 15 years are reported here. Table 3-2 shows these LNA circuits arranged according to their frequency bands of operation. It is not a complete list, but it gives an idea about the great progress that has been done in a relatively short time.

Frequency Band	Active Device	NF (dB)	Gain (dB)	Croy.	Year	Ref.
0.5-20 GHz L-S-C-X-Ku	2x4 Matrix (0.25x200 AlGaAs/InGaAs pHEMT)	3.5 ±1	19 ±1	No	2004	[105]
5-6.4 GHz C-Band	Two-stage (0.25x400 µm AlGaAs/InGaAs pHEMT)	0.76	16	No	2000	[98]
4-12 GHz C-X-Band	Three-stage (0.2x200 µm InGaAs/InAlAs/InP pHEMT	1.25	28	No	2004	[60]
		0.45	27	Yes		
8-18 GHz X-K_u-Band	Single-stage (0.2x200 µm AlGaAs/InGaAs pHEMT)	2.2	10	No	1993	[106]
26-32 GHz Ka-Band	Two-stage (0.15x120 µm AlGaAs/InGaAs pHEMT	1	18	No	1997	[107]
23-49 GHz Q-Band	Two-stage (0.2x100 µm InGaAs/InAlAs/InP pHEMT)	2.6	11	No	2004	[108]
60-80 GHz	Four-stage (0.1x75µm	2.3	25	No	2001	[109]
73-77 GHz	InGaAs/InAlAs/InP pHEMT)	0.4	25	Yes		
82-106 GHz W-Band	Six-stage (0.1x50 µm InGaAs/InAlAs/InP HJ-FET)	1.8	35	Yes	2000	[110]
91 GHz (W-Band)	Two-stage (0.15x60 µm AlGaAs/InGaAs pHEMT)	5.6	8.7	No	1994	[111]
155 GHz D-Band	Three-stage (0.1x30 µm InGaAs/InAlAs/InP pHEMT)	5.1	10	No	1998	[112]
183 GHz G-Band	Seven-stage (0.08x30 µm InGaAs/InAlAs/InP pHEMT)	5.5	24	No	2001	[113]

Table 3.2 Most important achievements in the MMIC HJ-FET LNAs.

3-9 Conclusions

In this chapter, a description of noise characterization of two port networks has been given with detailed expressions of the most important models (Fukui and Pospieszalski). A review of the state of the art MMIC is reported and a clear distinction has been made between the majority of work reported in the literature at > 2 GHz and the required performance for the low frequency SKA band which dictates very low Rn and low NFmin. These in turn imply large device widths at the frequencies of interest (0.3 to 2GHz). Such large devices invariable demand low leakage current devices which are the subject of studies of this work. These now set up the scene for the design of LNA for the low frequency band SKA as described in the following chapters.

CHAPTER-4

Linear and Nonlinear FET/HEMT Transistor Modeling

4-1 Introduction

Accurate small and large-signal models of Metal-Semiconductor Field Effect Transistors (MESFETs) and High Electron Mobility Transistors (HEMTs) devices are essential in all modern microwave and millimeter wave applications. Those models are used for robust designs and fabrication development. The sophistication of modern communication and radio astronomy systems dictates the need for monolithic microwave integrated circuits (MMICs), which consist of many transistors on the same chip. As the chip density increases, it is extremely important to complete MMIC device modeling and simulation prior to fabrication because the technology and design iterations are expensive and the technology often does not allow post fabrication tuning. Therefore, model accuracy is an essential part of first-pass design success. Device modeling is useful not only in the design, but also in production control and yield analysis **[38]**.

In this chapter, a simple approach for extracting a 15-element linear small signal model for HEMT devices is used. This technique implies the use of two sets of S-parameter measurements at two different bias conditions. It consists of two main steps; in the first step, the eight, bias-independent, extrinsic model parameters are extracted in preparation for the second step. In the second step, the seven, bias-dependent, intrinsic

model parameters are extracted at the bias point of interest. This model parameters extraction technique is achieved using a commercial microwave CAD software package from Agilent technologies, ADS, giving reliable results, and showing insensitivity to the unavoidable measurement errors over wide frequency range.

Also, the EE-HEMT nonlinear large signal models for the same devices are extracted by the aid the device modeling and measurement automation software package, IC-CAP, then the extracted models are exported to the ADS where some optimization algorithms are applied until the modeled DC and RF characteristics of the devices accurately fit the measured data.

Finally, based on Fukui's noise analysis **[114]** using the linear small signal model parameters extracted through the stated procedure, and also referring to the noise performance of the extracted nonlinear large-signal models of the devices, a noise characterization has been achieved and the noise behavior of the devices could be accurately estimated.

This technique has been applied to our (in-house) fabricated 1μm stained-gate InP-based InGaAs/InAlAs pHEMT devices, both for the old process and the new process samples and excellent agreements between the modeled and measured characteristics have been obtained.

4-2 Types of Transistor Models

Modeling is an investigative technique that uses a mathematical or physical representation of a system (in general, complex), process, or device in order to make a manageable description or analogy for all or some of its properties. Modeling can be divided into two main categories based on the way the device is to be represented: analytical modeling and equivalent circuit modeling. The analytical model of the device is formed by mathematical equations that represent or describe electron/hole transport in the device. This model is solved either numerically or analytically. However, in practise, this model is solved numerically in most cases because of the complexity and nonlinearity of the equations. Typically, many approximations are required to obtain a useful analytical model **[115]**. This is not the scope of this work; and hence, details of this modeling approach will not be dealt with further here. The work at hand is mainly

concerned with the second type of modelling: equivalent circuit models. In this modeling scheme, a circuit is proposed based on the expected physical behaviour of the device. This circuit consists of lumped elements: (e.g. resistances, capacitors, inductors) and sources. The basic task is to extract (calculate) those elements (parameters) depending on the DC or/and RF measurements of the device. In a device-model categorization, more than one model may be used to represent the same device depending on either the type of application or the level of the excitation of signal. Typically, three models are used for the device characterization:

(i) Linear small-signal model,

(ii) Noise model,

(iii) and nonlinear large signal model.

The **linear small-signal** model represents the behaviour of the device under low level of input excitation (i.e. when the signal voltages are small compared with the static operating point). Small-signal models are useful for small-signal amplifier designs **[116-123]**.

Noise model whose parameters are bias and temperature dependent but not frequency and power dependent, represents the noise behaviour of the device. Noise models are very useful for low noise amplifier and oscillator applications **[83, 84, 104, 124-132]**.

The **large-signal model** represents the behaviour of the device under large level of input excitation. This model is usually used in the design of circuits having large voltages propagating through them such as: power amplifiers and oscillators. The large-signal model is vital for calculations of nonlinear information: harmonic content, inter-modulation distortion, saturation...etc. The large-signal model also has to take into account the breakdown effects that occur at high voltage levels and generally they are applicable for both linear and nonlinear applications **[133-139]**.

Usually, the small-signal model is the corner stone for both noise and large-signal models. If an accurate large-signal or noise model is required, an accurate small-signal model should be devised first. In order to extract a large-signal model, small-signal model parameters should be extracted at different bias points through out the region of interest. Those parameters should fit bias dependent equations to represent the dependence of the device on the bias point **[140]**.

4-3 Device Modeling Software Tools

The general idea of the device modeling process is depicted in Figure 4.1. For a given device, an adequate model is selected according to the desired application. Next, the model equations are solved for the model parameters extraction process which gives a clear indication about the measurement setups and stimulus sweeps required for characterization.

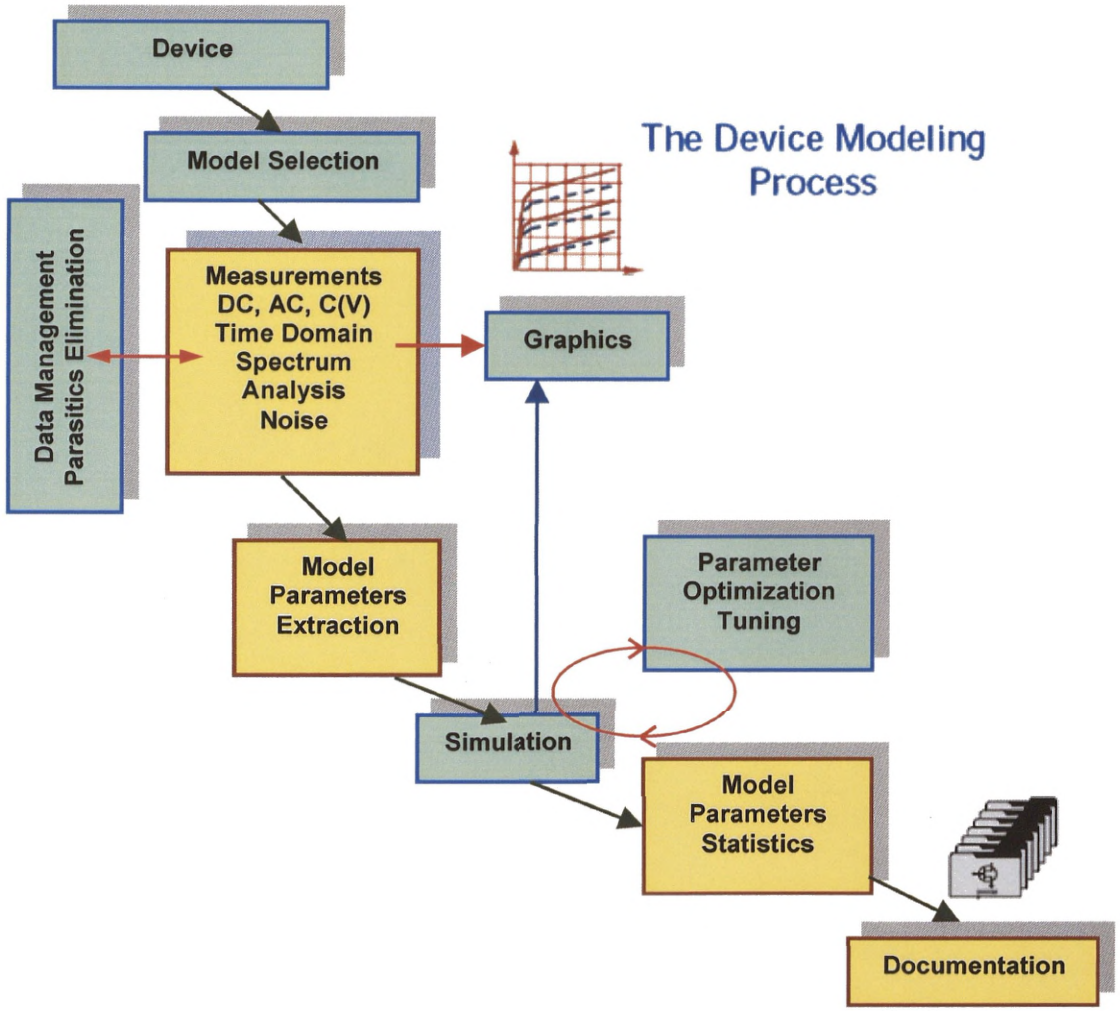


Figure 4.1 Device modeling process flow.

After all these measurements have been performed, the parameters extraction process, of the selected model, starts and it is usually a combination of direct parameter determination out of the measured data, followed by parameter fine-tuning with an optimizer or interactively by the modeling engineer. Once the parameter set has been

obtained, its validity has to be checked and documented. Finally, the design kit is developed, allowing the design engineers to simply insert this modeled component into their designs **[141]**.

For all of these tasks to be achieved, it is very helpful to use a dedicated control software. It serves to control the measurements, to extract the model parameters, to check the obtained results, to interact with a simulator and, finally, to compare and optimize the simulated data versus the measured ones.

Many device-modeling software packages are now commercially available and widely used for the purposes discussed above, and good examples of these are the Optimization Systems Associates' (**OSA™**), Compact Scout™, the Optotek's Small and Large Signal Analysis (SALSA™), and the software package used during this study, IC-CAP.

The HP/EEsof's Integrated Circuit Characterization and Analysis Programs (**IC-CAP™**) modeling suite is PC- and workstation-based, and is a robust, and effective device-modeling toolset that provides powerful characterization and analysis capabilities for today's semiconductor devices. The software allows users to develop their own model equation and extraction techniques, and also provides turn-key modules for a wide range of popular device models, including MESFET, HEMT, and HBT Empirical Device Models (EDMs), as well as Physical Based Models (PBMs) and HP Root data-based models **[142]**.

The software modules include measurement set-up, mathematical transforms, automation macros, and optimization routines to facilitate modeling. The model parameters are extracted by applying mathematical transforms to measured data. A Parameter Extraction Language (PEL) is built-in to facilitate creation of the transforms. The results of simulation based on the extracted model parameters can be plotted together with the measured data. IC-CAP contains three SPICE simulators and provides direct links to external simulators. The software has several optimization algorithms and user-controlled optimization settings. The sensitivity analysis mode provides information on important parameters for a particular optimization. The distinct feature of this software is the combined capabilities of instrument control, data acquisition, graphic analysis and optimization for device modeling. The software is compatible with the

Advanced Design System, ADS™, and many other CAD and simulation tools providing the power to build model libraries for them **[143]**.

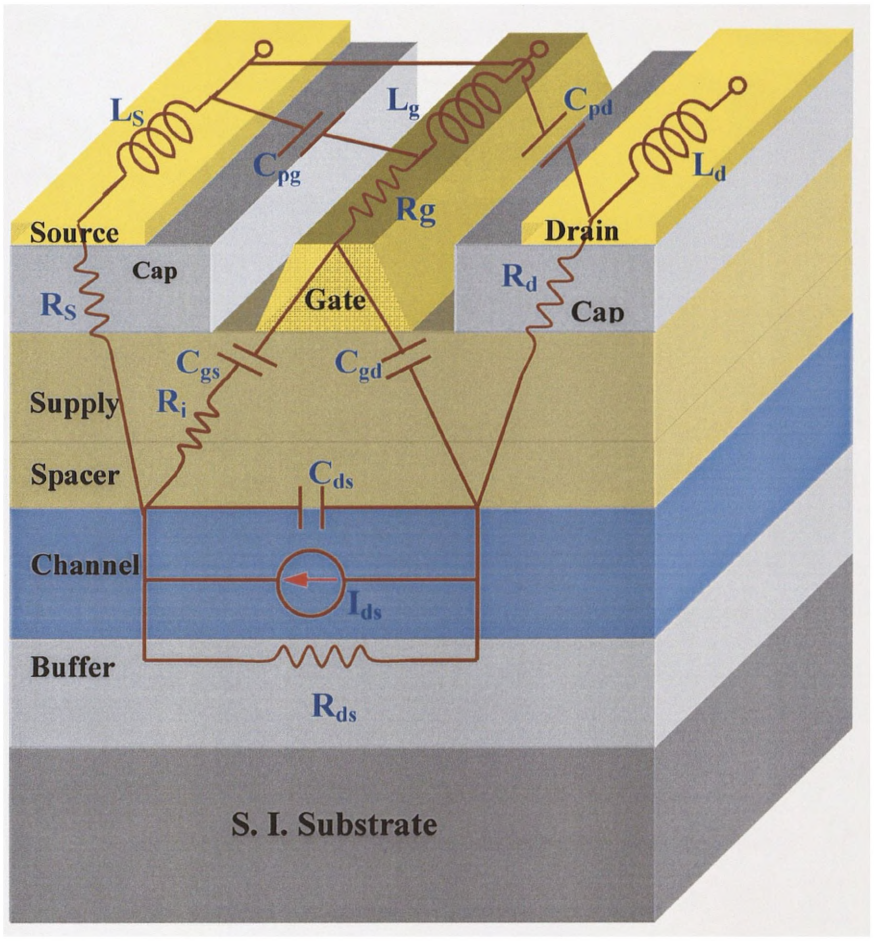
4-4 Linear Small-Signal Device Modeling

Determination of the small-signal equivalent circuit of a field effect transistor is very useful for the device performance analysis (gain, noise, etc.) in designing of microwave circuits and characterizing the device technological process. Usually, the small-signal equivalent circuit is obtained by optimizing the component values to closely fit the small-signal microwave scattering parameters measured on the device at certain DC bias point.

4-4-1 Physical origin of the HEMT small-signal model

Figure 4.2 shows a schematic cross-section diagram of a HEMT device with the small-signal model elements associated with its physical structure. In this Structure, the model elements can be defined as following:-

- R_g and L_g are the gate metallization resistance and Inductance (of the gate Schottky contact). R_g is directly proportional to the gate size and inversely proportional to the gate metallization thickness and it is one of the basic parameters that determine the noise performance of the device. L_g is usually large for short gate lengths although it is a function of the particular layout used.
- R_S and R_d are the source and drain parasitic resistances that account for the contact resistance of the ohmic contacts between the metal electrodes and the doped cap layer in addition to the bulk resistance of the semiconductor regions between the gate and both of the source and drain.
- L_S and L_d are the source and drain metallization inductances.
- C_{pg} and C_{pd} are the gate and drain bond pad capacitances.
- R_i is the resistance of the semiconductor region under the gate, between the source and the channel (usually known as channel resistance).
- C_{ds} represents the drain-source capacitance and arises from capacitive coupling between the doped regions of the drain and sources, separated by the depletion region, and always considered constant (bias independent)



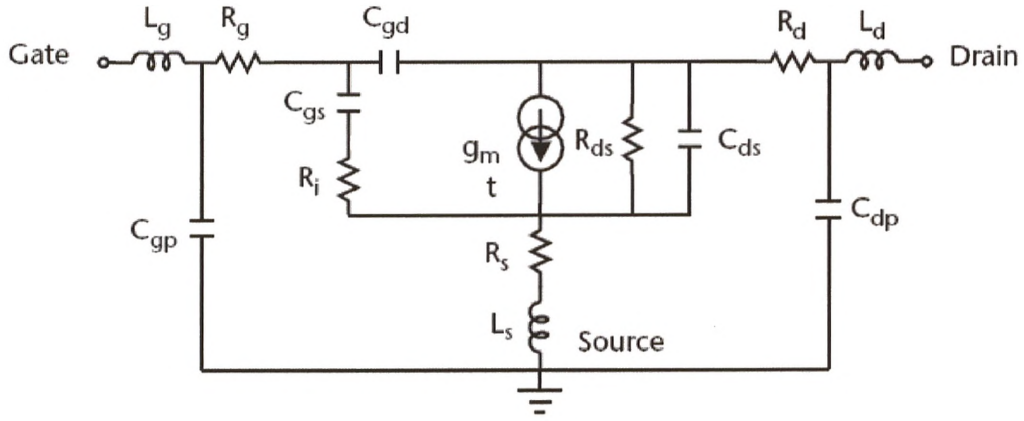


Figure 4.2 FET/HEMT linear small-signal equivalent circuit model with physical origin of the model elements.

•C_{gs} and C_{gd} are the gate-source and gate-drain (channel) capacitances representing the change in depletion charge with respect to V_{GS} and V_{GD} and they are always considered nonlinear.

•I_{ds} is a voltage controlled current source representing the drain-source current with transconductance G_m, time delay τ, and output resistance R_{ds}.

Some of these elements are nonlinearly dependent on the internal voltages V_{gs} and V_{ds}. Others are linear, or can be approximated as linear elements. I_{ds}, C_{gs}, and C_{gd} are usually nonlinear elements for their strong dependence on V_{gs} and V_{ds}.

4-4-2 Small-signal modeling theory

The circuit model shown in Figure 4.2 is the most commonly-used linear small-signal equivalent circuit FET/HEMT model. Even though there are other circuit topologies with additional elements in the literature the equivalent circuit topology shown has demonstrated excellent agreement with measured data and while there are numerous small-signal equivalent circuit topologies for microwave FET's models, the main difference among them lies in the parasitic elements location, which depends on the transistor geometry and the transistor embedding medium.

Independently of topology, the small-signal model circuit is normally divided into two sections:-

(a) The bias-dependent intrinsic section which includes the seven intrinsic elements: G_m, R_i, τ, R_{ds}, C_{ds}, C_{gs}, and C_{gd}.

(b) The bias-independent extrinsic section which includes the eight extrinsic (Parasitic) elements: R_S, R_d, R_g, L_S, L_d, L_g, C_{pd}, and C_{pg}.

The main concept of the extraction process, which is employed by many researchers, is to remove the extrinsic element section from the measurements to end up with Y-parameters of the intrinsic section. The Y-parameters are the most convenient parameters since the intrinsic section exhibits PI topology. The simple analytical expressions of the Y-parameters can be used to calculate the intrinsic elements, after de-embedding the measured S-parameters of the active device with the extrinsic elements values, as discussed in the following subsections.

4-4-3 Extrinsic model parameters extraction

The extrinsic component values of the small-signal model can be analytically obtained from the measured cold-device S-parameters. As a matter of fact, at zero drain bias and for a gate voltage lower than the pinch-off voltage, the intrinsic gate capacitance (i.e., under the gate) cancels, as does the channel conductance. Under these biasing conditions, the analytical equivalent circuit of the cold device is represented by Figure 4.3 **[129]**.

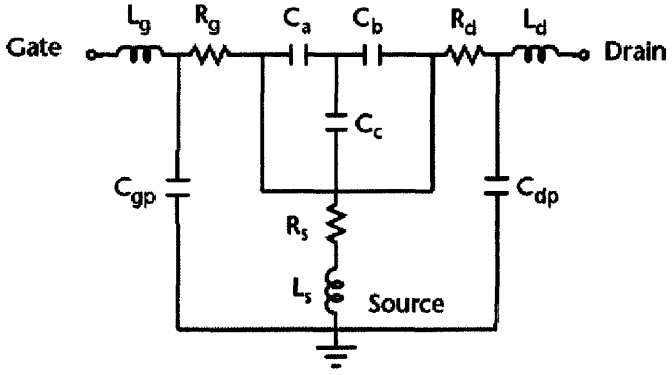


Figure 4.3 Cold-device equivalent circuit model [23].

The capacitors C_a, C_b, and C_c represent the fringing capacitance due to depletion layer extension at each side of the gate. This circuit preserves the symmetry of the device when viewed from the gate and drain sides of the device. In this circuit, the influence of the C_{pd} and C_{pg} pad parasitic capacitances is negligible and consequently the extrinsic Z parameters, **Zcij**, corresponding to the device's cold S-parameters are simply given by:-

$$Z_{C11}=R_g+R_s+j\left[w\left(L_g+L_s\right)+\frac{1}{wC_{ab}}\right] \tag{4.1}$$

$$Z_{C12}=Z_{C21}=R_s+j\left[wL_s+\frac{1}{wC_b}\right] \tag{4.2}$$

$$Z_{C22}=R_d+R_s+j\left[w\left(L_d+L_s\right)-\frac{1}{wC_{bc}}\right] \tag{4.3}$$

Where $$C_{ab}^{-1}=C_a^{-1}+C_b^{-1},\ C_{bc}^{-1}=C_b^{-1}+C_c^{-1} \tag{4.4}$$

From the real parts of equations (4.1)-(4.3), the extrinsic (parasitic) resistances can be extracted as follows:-

$$R_s = Re(Z_{C12}) \quad (4.5)$$

$$R_d = Re(Z_{C22}) - Re(Z_{C12}) \quad (4.6)$$

$$R_g = Re(Z_{C11}) - Re(Z_{C12}) \quad (4.7)$$

While the imaginary parts of equations (3.1)-(3.3) show that:-

$$wImag(Z_{C11}) = w^2(L_g + L_s) - \frac{1}{C_{ab}} \quad (4.8)$$

$$wImag(Z_{C12}) = w^2 L_s - \frac{1}{C_b} \quad (4.9)$$

$$wImag(Z_{C22}) = w^2(L_d + L_s) - \frac{1}{C_{bc}} \quad (4.10)$$

Equations (4.8)–(4.10) enable the inductances corresponding to L_g, L_d, and L_s to be obtained from the gradients of $wImag(Z_{C11})$, $wImag(Z_{C12})$, and $wImag(Z_{C22})$ against w^2 plots.

Under pinch-off biasing conditions and for frequencies up to a few gigahertz, the resistances and inductances have no influence on the imaginary part of the Y-parameters, of the circuit model, that can be written as:-

$$Imag(Y_{11}) = jw\,(C_{pg} + 2C_c) \quad (4.11)$$

$$Imag(Y_{12}) = Imag(Y_{21}) = -jwC_c \quad (4.12)$$

$$Imag(Y_{22}) = jw\,(C_{pd} + C_c) \quad (4.13)$$

Parasitic (extrinsic) capacitances, C_{pg} and C_{pd}, can be directly extracted from equations (4.11)–(4.13).

4-4-4 Intrinsic model parameters extraction

After extracting the eight-extrinsic (parasitic) elements from the cold (pinched) device measurement, they can be used for de-embedding the measured hot (active) device S-parameters to calculate the intrinsic device admittance matrix (Yint), through a series of matrix manipulations. The procedure of determining Yint from the measured hot S-matrix is shown in Figure 4.4.

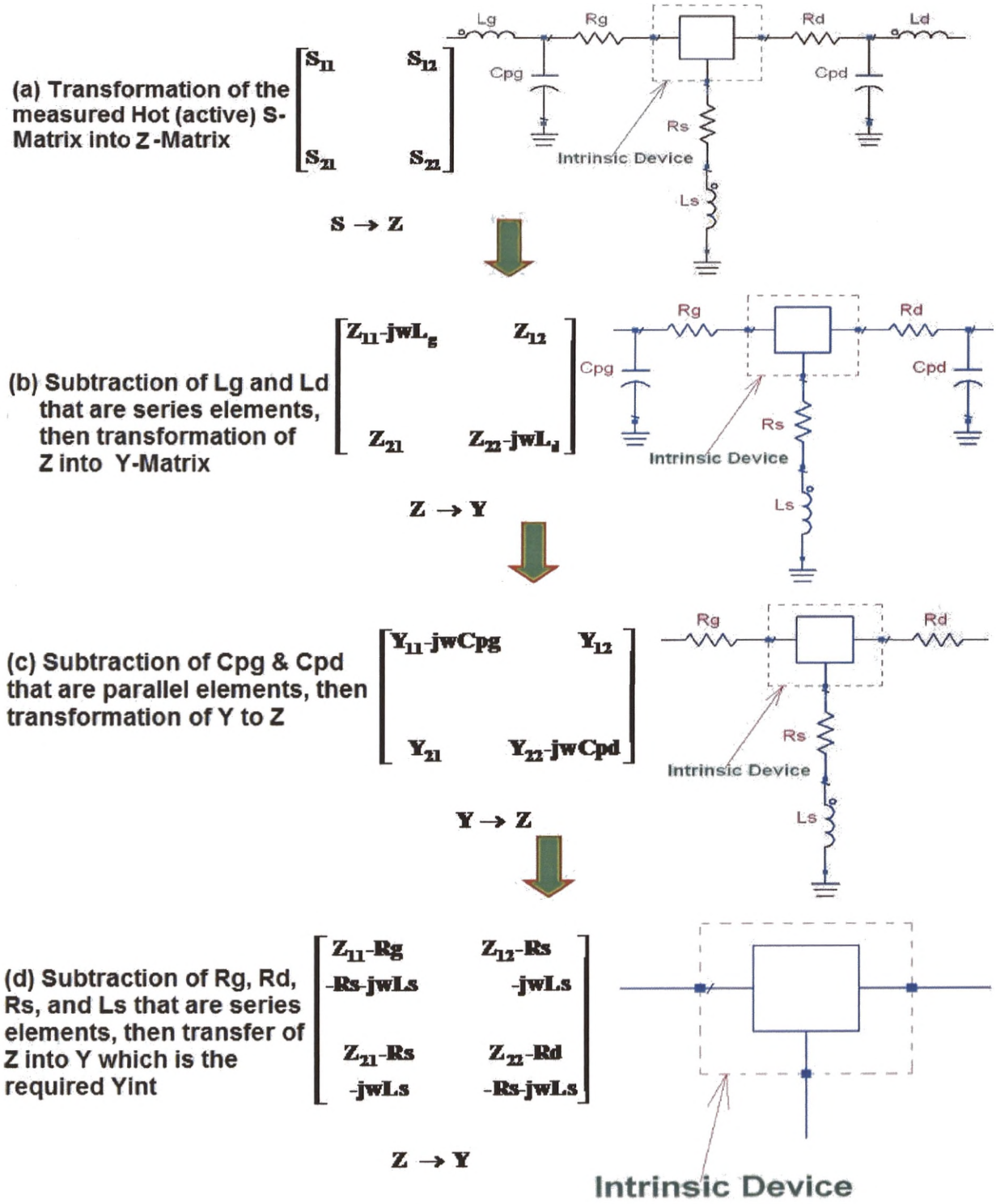


Figure 4.4 Extraction procedure of the device intrinsic Y-matrix.

The intrinsic Y-Matrix of the device under active bias conditions, determined by the previous procedure can be expressed as [117] :-

$$Yint = \begin{bmatrix} \frac{R_i C_{gs}^2 w^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) & -jwC_{gd} \\ \frac{g_m e^{-jwT}}{1+jwR_i C_{gs}} - jwC_{gd} & g_{ds} + jw\left(C_{ds} + C_{gd}\right) \end{bmatrix} \quad (4.14)$$

Where, $$D = 1 + w^2 C_{gs}^2 R_i^2 \quad (4.15)$$

The seven intrinsic model parameters of the device, given by the following expressions, can be extracted directly from equations (4.14) and (4.15).

$$C_{gd} = \frac{Imag(Y_{21})}{w} \quad (4.16)$$

$$C_{gs} = \frac{Imag(Y_{11}) - wC_{gd}}{w}\left(1 + \frac{(Re(Y_{11}))^2}{(Imag(Y_{11}) - wC_{gd})^2}\right) \quad (4.17)$$

$$R_i = \frac{Re(Y_{11})}{(Imag(Y_{11}) - wC_{gd})^2 + (Re(Y_{11}))^2} \quad (4.18)$$

$$g_m = \sqrt{\left((Re(Y_{21}))^2 + (Imag(Y_{21}) + wC_{gd})^2\right)\left(1 + w^2 C_{gs}^2 R_i^2\right)} \quad (4.19)$$

$$\tau = \frac{1}{w} Sin^{-1}\left(\frac{-wC_{gd} - Imag(Y_{21}) - wC_{gs}R_i Re(Y_{21})}{g_m}\right) \quad (4.20)$$

$$C_{ds} = \frac{Imag(Y_{22}) - wC_{gd}}{w} \quad (4.21)$$

$$R_{ds} = \frac{1}{Re(Y_{22})} \quad (4.22)$$

Equations (4-15)-(4-21) are valid for all frequencies lower than the cut-off frequency (f_T), all drain voltages greater than zero, and all gate voltages above pinch-off.

The above extraction procedure is programmed on the ADS for an automatic parameters extraction process which can save a lot of time and effort. All details about the programming on the ADS and the resulted small-signal parameters as a function of frequency are given in Appendix-B

4-4-5 Small-signal models extraction for the (in-house) fabricated devices

The linear small-signal model parameters extraction procedure stated here was applied for our (in-house) fabricated 1 μm InP-based InGaAs-InAlAs pHEMT samples, introduced before in chapter-2, and also for the GaAs/AlGaAs samples introduced in Appendix-D.

On-wafer measurements for the linear modeling process have been carried out using an HP-8510C VNA and Cascade Microtech RF probe station automated by the Agilent's IC-CAP software. S-Parameters have been measured form 45 MHz up to 40 GHz at two different modes of operation for each device under test;

- Cold (passive) measurements of the device in pinch-off mode ($V_{DS} = 0$, $V_{GS} < V_{TH}$) for the extrinsic model parameters extraction.
- Hot (active) measurements of the device in normal mode of operation ($V_{DS} > 0$, $V_{GS} > V_{TH}$) for the intrinsic model parameters extraction. S-Parameters have been measured at many different active bias points for linear model extraction at all of them to check the device behavior at many different conditions (low and high current, voltage, and transconductance).

After performing all of the above measurements for many different devices on the same sample, the measured data were exported form IC-CAP to the ADS where the model parameters extraction technique discussed here is applied according to the procedures shown in Appendix-B.

The extracted linear models could be checked if they accurately fit the measured data or not and if not, the model parameters are fine tuned further. Almost all of the small-signal models extracted using this technique accurately fitted the measured data without doing any optimization or tuning as shown in Figure 4.5 for a 2x100 μm device from sample VMBE-1841 (old process) and Figure 4.6 for a 4x75 μm device from sample XMBE-106 (new process).

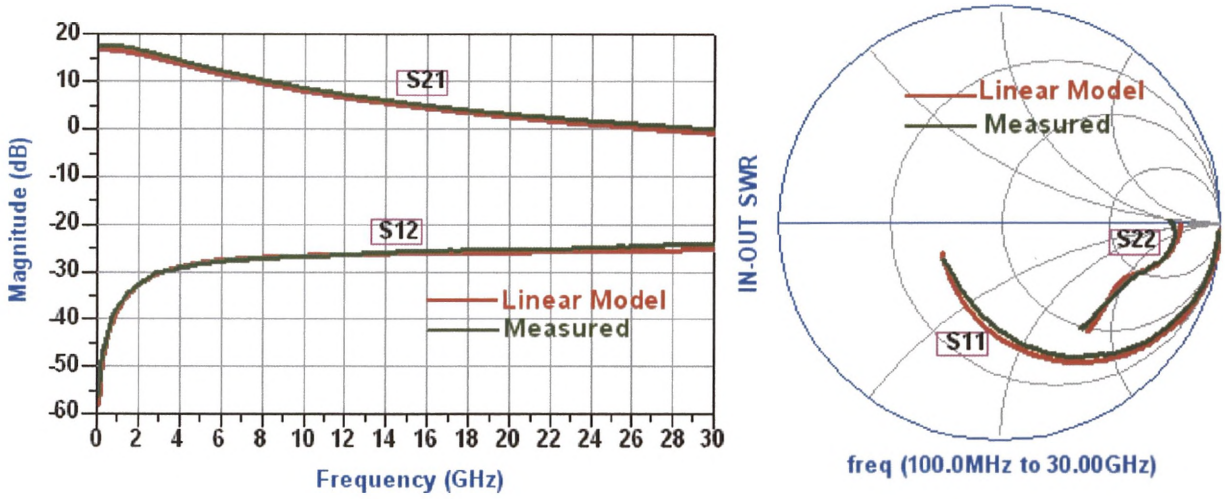


Figure 4.5 Comparison between the modeled and measured S-Parameters of a 2x100 device, sample VMBE-1841 (old process) biased at 1.5 V, 19.6 mA.

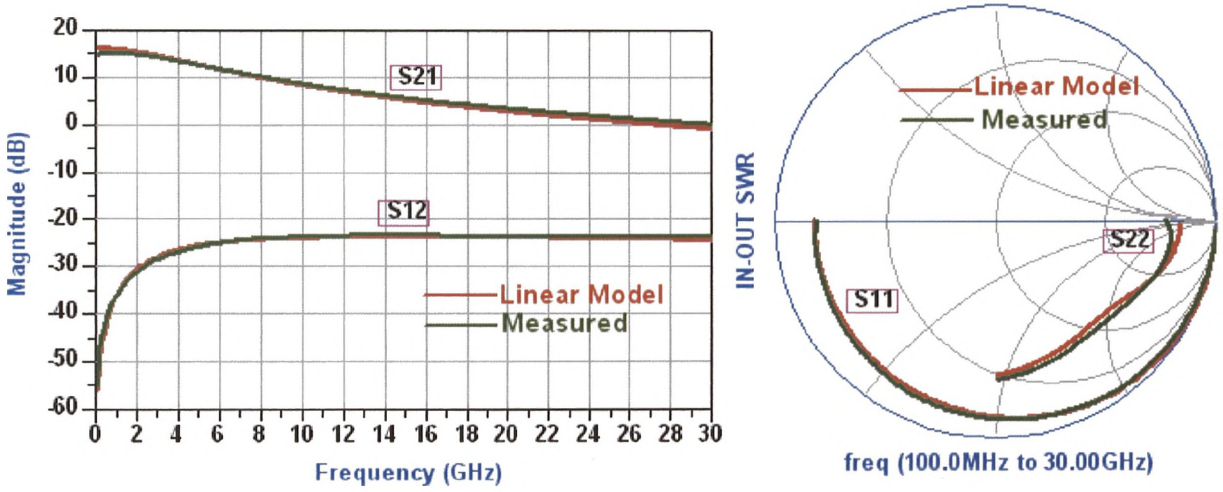


Figure 4.6 Comparison between the modeled and measured S-Parameters of a 4x75 device, sample XMBE-106 (new process) biased at 1.5 V, 23 mA.

The linear small-signal modeling technique introduced here has been applied to all of the fabricated and measured devices; the old process samples of thin gate metallization, VMBE-1831, 1832, 1841 and XMBE-22 and the new process samples of thick gate metallization, VMBE-1841, XMBE-106, and XMBE-22. The extracted model parameters were compared in three different ways;

•Devices with the same size from different samples, under the same DC biasing conditions, were compared together to study the small-signal behavior of the devices of each sample and to check the agreement of the extracted model parameters with the previously measured data.

•Different device sizes for a particular sample, also under the same biasing conditions, were compared together to check the scaling of the extracted parameters with the device size.

•The behaviors of a particular device under different bias conditions were compared to check the variation of the model parameters with bias.

4-4-5-1 Small-signal models of the old process samples

Table 4.1 shows the extracted model parameters of 2x100 μm devices from the old samples, all biased for maximum transconductance at 1.5 V drain voltage. From these data the following observations can be made:

•The highest transconductance was provided by VMBE-1841 (460 mS/mm) and the lowest gm was obtained for sample VMBE-1832 (270 mS/mm). These values have a good match with the g_m values extracted previously form the DC-measurements (Chapter-2); they may be slightly higher but that may be attributed to deep level traps and surface states **[144]**, or the carrier generation/recombination in a dynamic process**[145]**.

•R_{ds} is the inverse of the output conductance, g_{ds}, which measures the flatness of the IV-curves in saturation. From the obtained data it can be observed that the lowest output conductance, g_{ds}, (highest R_{ds}) is provided by VMBE-1841 and the opposite for VMBE-1832 exactly the same results obtained before from the DC measurements, but with relatively different values. However, special care must be taken when comparing the DC and RF calculations of g_{ds} as it is subject to a number of influences that must be carefully separated. DC-g_{ds} values obtained from the output characteristics can sometimes appear to be negative. A first effect to be separated is the effect of self-heating and the temperature dependence of the parasitic resistances, especially the gate resistance R_g. Self-heating leads to a rise of R_g and thus to a reduction of the internally applied V_{GS} bias, so self-heating causes an internal bias shift **[146]**. A second

effect is the influence of carrier generation/recombination. As reported especially for GaN HEMTs **[147]**, but also for pseudomorphic HEMTs **[145]**, the occurrence of traps leads to hysteresis in the DC-output characteristics, an effect, which is not seen in RF-parameters. The RF-value of g_{ds} extracted of measured data is therefore always positive and may be different from those obtained from DC characteristics.

Sample →		VMBE-1831	VMBE-1832	VMBE-1841	XMBE-22
Intrinsic Model Parameters	g_m (ms)	72	54	95	77
	T (psec)	1.63	1.9	1.87	1.48
	R_i (Ω)	7.8	4.6	6.2	7
	R_{ds} (Ω)	350	335	500	440
	C_{gs} (pF)	0.36	0.4	0.48	0.418
	C_{ds} (pF)	0.043	0.041	0.022	0.019
	C_{gd} (pF)	0.034	0.037	0.021	0.025
Extrinsic Model Parameters	R_s (Ω)	1.8	2.25	2.3	2.4
	R_g (Ω)	12.8	17.2	20.7	22
	R_d (Ω)	2.2	3.2	3.25	2.5
	L_s (pH)	4.3	5.5	4	4.7
	L_g (pH)	22.7	14.35	12	13
	L_d (pH)	24.5	15.3	25.4	22.5
	C_{pg} (fF)	2.8	2.5	1.5	1.2
	C_{pd} (fF)	33.5	28	34	35

Table 4.1 Linear small-signal model parameters for 2x100 µm devices of the old process samples biased for maximum transconductance at 1.5 V drain voltage.

•The general trend of the channel resistance, R_i, is to decrease with increasing the drain current. Looking at R_i values obtained here, the lowest value obtained is for VMBE-1832 because this is the only sample for which the peak g_m (DC bias point applied) is obtained very far from the pinch-off (i.e. at high current value) while for all other samples

the peak transconductance has been obtained at low current values (i.e. very close to the pinch-off).

•Low intrinsic capacitances, C_{ds} and C_{gd}, are obtained with relatively high gate-source capacitance, C_{gs}, but that may be attributed to the fringe capacitances added due to coupling between the semiconductor caps, the ohmic metal, and the gate metal **[148]**.

•Relatively high parasitic resistances R_s and R_g are obtained for all samples but with very low parasitic inductances and pad capacitances.

Usually the parasitic inductances have a direct effect on the noise performance of the devices especially L_s and L_g that are responsible for the variation of the noise resistance, R_n, with frequency **[149]**.

•The gate resistance, R_g, which is the main parameter of interest during this study, consistently lies between 12.8 Ω and 22 Ω. These values are almost an order of magnitude higher than commonly reported values for a 1 μm technology **[114]**. The high values of R_g are certainly attributed to the thin metallization scheme (150 nm) used in the old process as the gate metallization resistance, R_g, is inversely proportional to the metal thickness **[150]**. Williams **[68]** suggests a metallization thickness of 300 nm at least for the lowest R_g contribution.

From all of these observations it can be concluded that the old process devices suffer relatively high parasitic effects, especially the parasitic resistances and source-gate capacitance, describing the previously obtained low f_{max} values. Also, relatively poor noise characteristics are expected for these devices as will be seen later in this chapter. The least sample subjected to these effects is VMBE-1831 and that is why it recorded the highest f_T (38.4 GHz), and f_{max} (37.3 GHz).

To check the effect of the device size on the small-signal model parameters, the small-signal modeling technique discussed was applied for many different device sizes (2x20 μm - 2x100μm) from sample VMBE-1832, all biased at V_{ds} = 1.5 V and V_{gs}= -0.6 V. More tabulated data given in Appendix-B shows the extracted parameters of these models. The obtained results showed a good agreement with the classic scaling rules **[151-153]** for all parameters either the group that are fully scaled with W_g like g_m, R_{ds},

C_{gs}, and C_{gd} or the parameters that have a moderate dependence on W_g such as C_{ds}, R_i, and the parasitic resistances and also the parameters that are completely independent of the device size and their values have to be individually extracted for a particular device size. A clear example of the last group is the parasitic inductances that are mainly dependent on the number of gate fingers and gate-to-gate pitch.

Now to check the effect of DC bias on the small-signal model, the model parameters of a 2x100 µm device of sample VMBE-1841 have been extracted under different bias conditions. The drain bias voltages are 1V and 1.5V and the gate voltages are -0.2V, -0.4V, -0.5V, and -0.6V, while the nominal pinch-off voltage of this sample is -0.78V. Figure 4.8 depicts the behaviour of the model parameters as a function of the drain and gate bias voltages from which the following observations can be made:-

•The transconductance behaviour, shown in Figure 4.8(a), perfectly supports the theoretical expectations. Since all values of V_{ds} are in the saturation region, the dependence of g_m on V_{ds} is very slight in this region. On the other hand, the parasitic effect is the main cause of gm reduction at a high V_{gs} **[154]**. According to Lee et al's calculations **[155]**, channel electron carrier density increases linearly with V_{gs} at a low V_{gs} but saturates at certain V_{gs} value resulting in the transconductance compression shown.
•Figure 4.8(b) shows the normal and expected dependence of R_{ds} on V_{gs} and V_{ds}. R_{ds} is highly dependent on V_{gs} and weakly dependent on V_{ds} in the saturation region.

•The value of C_{gs}, Figure 4-8(c), decreases as V_{gs} increases towards pinch-off as the depletion region width of the gate-source junction widens, and hence the depletion capacitance decreases with the higher reverse bias voltage. Also, the value of C_{gs} slowly increases with higher drain voltage since V_{ds} does not directly affect the depletion width of the gate source junction.

•Similar conclusions can be drawn from the C_{gd} plot in Figure 4.8(d). The behaviour is almost the opposite to that of C_{gs} because increasing the depletion region width towards one side diminishes the depletion region width on the other side.

•As stated before, the general trend of the channel resistance, R_i, is to decrease with higher drain current values (higher V_{ds} or lower V_{gs}), as depicted in Figure 4.8(e).

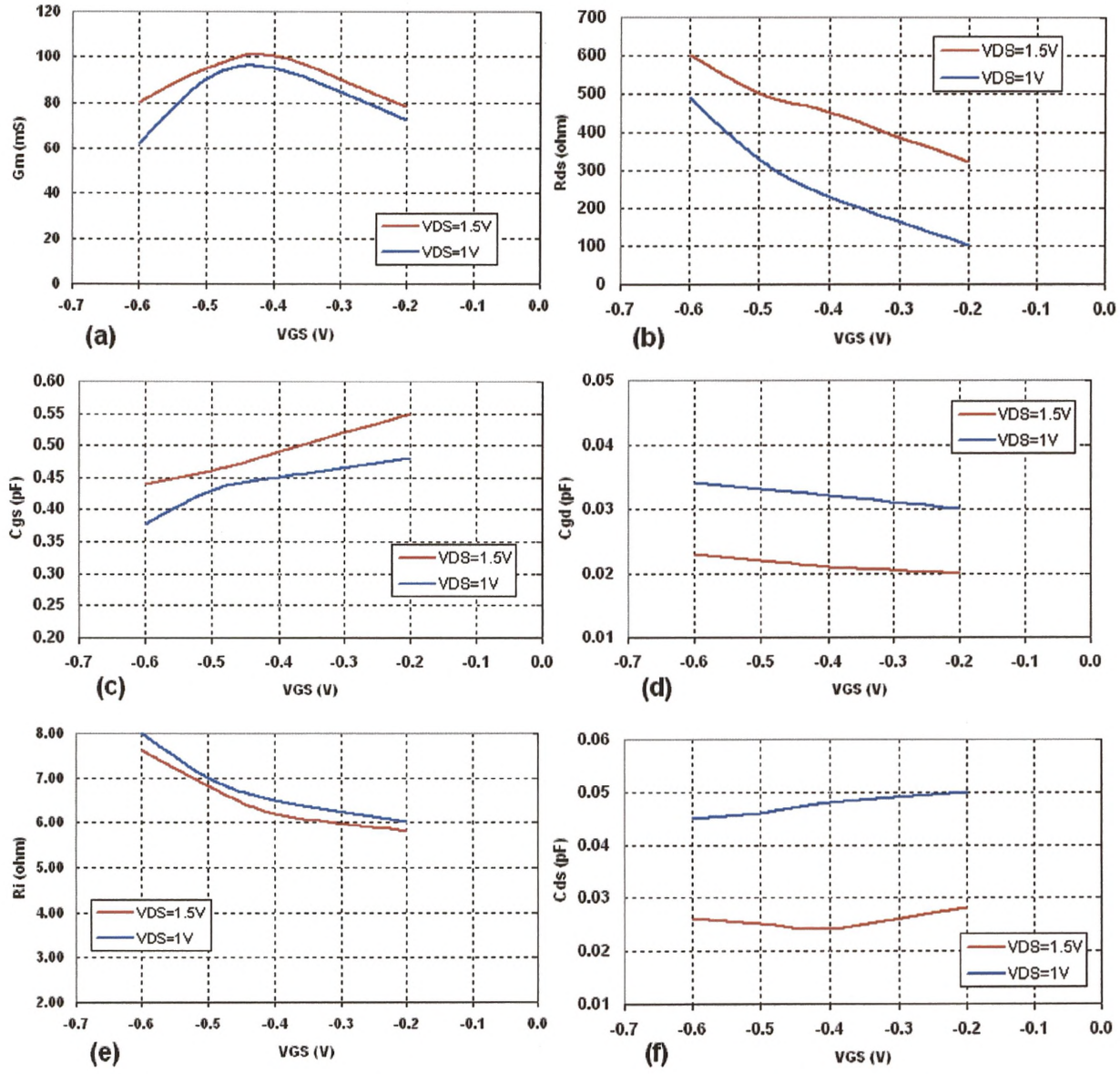


Figure 4.7 Small-signal model parameters variation with DC-bias (device 2x100 µm sample VMBE-1841).

•Finally, the characteristics of C_{ds} is shown in Figure 4.8(f) which provides good evidence that C_{ds} is less affected by the bias voltages especially for larger values of V_{gs}. This behaviour is expected because C_{ds} basically originates from the capacitive coupling

of the source and drain and many researchers assume that C_{ds} is constant. However, bias dependent contributions to C_{ds} arise from buffer and channel layers depending on the channel carrier distribution **[156]**.

4-4-5-2 Small-signal models of the new process samples

The linear small-signal models parameters for 2x200 μm devices of the new process samples are shown in Table 4.2. All devices are biased for maximum g_m at drain voltage of 1.5 V. Looking at these results, the followings can be seen:-

•The new process devices exhibit relatively lower transconductances compared to the old process but with better output conductances, the issue that is consistent with the DC calculations of g_m and g_o.

•Almost the same range of the intrinsic capacitances (C_{gs}, C_{ds}, and C_{gd}) values has been obtained for the new devices except of sample XMBE-38 which exhibits much higher capacitances especially C_{ds} and C_{gd} and this is may be the main reason behind the lower f_{max} obtained for this sample compared with the other new process samples.

•The parasitic resistances R_s and R_d have been greatly enhanced in the new process promising for a better noise performance for the new devices. However, the greatest improvement done within the new process is the tremendous reduction in the gate resistance values (~ 3 Ω for 400 μm) compared with the very high values obtained before in the old process. This is certainly because of the much thicker gate metallization used and so, much better noise characteristics will be expected for the new devices as we will seen later in this chapter.

In fact, a further improvement in the gate resistance, R_g, and the noise resistance, R_n, was the major driving force behind the latest generation of the 1 μm InP pHEMTs with the multi-gate fingers and very large gate periphery.

Sample →		VMBE-1841	XMBE-106	XMBE-38
Intrinsic Model Parameters	g_m (ms)	142	110	165
	T (psec)	1.9	1.8	2.6
	R_i (Ω)	0.5	2	0.5
	R_{ds} (Ω)	920	350	540
	C_{gs} (pF)	0.82	0.7	0.88
	C_{ds} (pF)	0.065	0.049	0.12
	C_{gd} (pF)	0.058	0.047	0.143
Extrinsic Model Parameters	R_s (Ω)	0.8	1.1	0.72
	R_g (Ω)	3	3.2	2.8
	R_d (Ω)	1.7	2	2.1
	L_s (pH)	6.8	7	6.1
	L_g (pH)	45.4	52.7	60
	L_d (pH)	35.4	51	73
	C_{pg} (fF)	13.7	11.8	6.45
	C_{pd} (fF)	61	65.5	67.3

Table 4.2 Linear small-signal model parameters for 2x200 µm devices of the new process samples biased for maximum transconductance at 1.5 V drain voltage.

Table 4.3 shows the small-signal linear models extracted for these devices from sample XMBE-106, all biased for the maximum g_m at V_{ds} = 1.5 V. Also, for a fair and clear comparison between these devices the air-bridges that connect the gate fingers together are chosen for all of them to be over the drain side. Looking at these devices the following properties can be noticed:-

•The same relatively low transconductance (like the two gate finger devices of the same process) but with higher output conductance and both of them almost scale with gate size regardless of the number of fingers.

•The lowest intrinsic gate-source capacitance, C_{gs}, has been obtained for these devices compared with all other two gate finger devices (~ 1.4 pF/mm instead of 2 pF/mm) and also independent on the number of fingers (four or six).

Size (μm) →		4x50	4x75	4x100	4x200	6x50	6x100	6x200
Intrinsic Model Parameters	g_m (ms)	50	73	102	195	81	135	280
	T (psec)	1.85	1.84	1.82	1.94	2.1	1.92	2.2
	R_i (Ω)	4.3	3.7	2	1	3.4	1.6	1
	R_{ds} (Ω)	900	550	450	100	555	280	70
	C_{gs} (pF)	0.312	0.432	0.582	1.12	0.45	0.74	1.6
	C_{ds} (pF)	0.019	0.032	0.046	0.163	0.038	0.057	0.2
	C_{gd} (pF)	0.021	0.032	0.048	0.155	0.043	0.07	0.2
Extrinsic Model Parameters	R_s (Ω)	0.9	1	1	1	0.9	0.8	0.6
	R_g (Ω)	1.7	1.8	1.7	1.8	1.7	1.72	2.1
	R_d (Ω)	0.85	0.95	0.8	0.75	0.85	0.72	0.58
	L_s (pH)	5.6	3.9	5.6	6.2	5.7	3	2.5
	L_g (pH)	31.4	34.4	63.2	85.6	44.25	82	120
	L_d (pH)	37.7	36.5	46.6	52	44.5	51	61.5
	C_{pg} (fF)	20.4	23.4	26.7	23	48.6	25.7	3.6
	C_{pd} (fF)	56.3	68.4	81.6	131.3	66.2	112.6	172

Table 4.3 Linear small-signal model parameters for devices with different gate structure from sample XMBE-106, all biased at V_{ds} = 1.5 V and V_{gs} = -1.5 V.

•A further enhancement has been achieved with the parasitic resistances especially R_d which exhibit much lower values than the two finger devices. It should also be noted that the six finger devices exhibit slightly lower parasitic resistances than the four fingers.

•R_g has been further improved till reaching a minimum value of approximately 1.7 Ω for all multi gate finger devices regardless of the device size achieving one of the main objectives of this process.

•While the parasitic inductances still keep their low values, the pad capacitances started to increase with multi gate finger devices. In fact, this issue depends on the position of the air-bridges if they are passing over the drain or the gate side. For the first case, which is the case shown in the table, C_{pd} exhibits much higher values compared with the two finger devices and vise versa for C_{pg} in the second case.
The impact of all of these issues on the noise performance of the devices will be examined in the last section of this chapter.

4-5 Nonlinear Large-Signal Device Modeling

Many different nonlinear large-signal transistor models can be used to represent the device's DC and RF characteristics and a good model should guarantee all of the following **[157]**:-

•Should form a compromise between many typical devices, many bias points, and many signal levels.

•Must accurately predict power performance and linearity and may include power load pull data for power designs.

•Since the passive parasitic elements are based on physical properties of the structure the model can be extrapolated in frequency and scaled within its model limitations.

•Must take into account the breakdown effects that occur at high voltage levels or by forward biasing the gate-source Schottky diode. In particular, the gate-drain avalanche breakdown current occurs at a high value of V_{gd} and the forward gate-source breakdown current occurs when a positive voltage is applied to the device's gate **[23]**.

In the last three decades a lot of effort has been done in the field of nonlinear large-signal modeling of field effect transistors. Table 4.4 shows the most basic FET/HEMT models with the major contribution given by each.

Time	Model Name	Author	Major Contribution
1980	Curtice Model [134, 135]	Curtice	First Empirical model
1987	Staz Model [137]	Staz	2D Capacitance model
1990	TOM Model [158]	McCamant	Negative DC Conductance
1991	Root Model [159]	Root	First Table-based model
1992	Chalmers Model [139]	Angelov	Continuity to High Orders
1993	EE-FET/EE-HEMT [160]	EE-SOF	RF Current added
1997	Parker Model [161]	Parker	Continuity to High Orders
1997	Enhanced TOM Model [162]	Wei	Dispersion Handled better
1997	Black-Box Modeling [138]	Schreurs	Time-Domain

Table 4.4 Main advances in the large-signal nonlinear models.

4-5-1 Basic large-signal modeling theory

In the previous section, the small-signal model was demonstrated as being an equivalent circuit model with elements that are bias dependent, but not frequency or power dependent. For the large-signal model, prediction should extend to gain compression, harmonic distortion, and power load circles. The large-signal simulation relies on the use of a harmonic balance simulator, whereby the linear circuit is simulated in the frequency domain; the nonlinear circuit is simulated in the time domain **[134]**. The time domain analysis comes from voltage controlled current sources placed into the small signal equivalent circuit model in the form of equations defining I_{ds}, I_{dg}, and I_{gs} as seen in Figure 4.8 for the EE-HEMT nonlinear model as an example.

In all large-signal FET models, a main requirement is to have an equation that predicts I_{ds}. This current equation can be modeled by measuring I_{ds} at several values of V_{gs} while sweeping V_{ds} and fitting an appropriate equation to the data. Two other important parameters to characterize are the charge capacitance models. These allow for the change in C_{gs} and C_{gd} at different bias conditions.

With the introduction of newer devices that include InP HEMTs or InGaAs pHEMTs with sub-micron gate lengths, updated models have been proposed to account for the accurate prediction of not only the current and voltage characteristics but the derivatives as well. Angelov et al. **[139]** has proposed a simple method that includes the hyperbolic

tangent gate voltage function in the drain current equation to the voltage dependent capacitance.

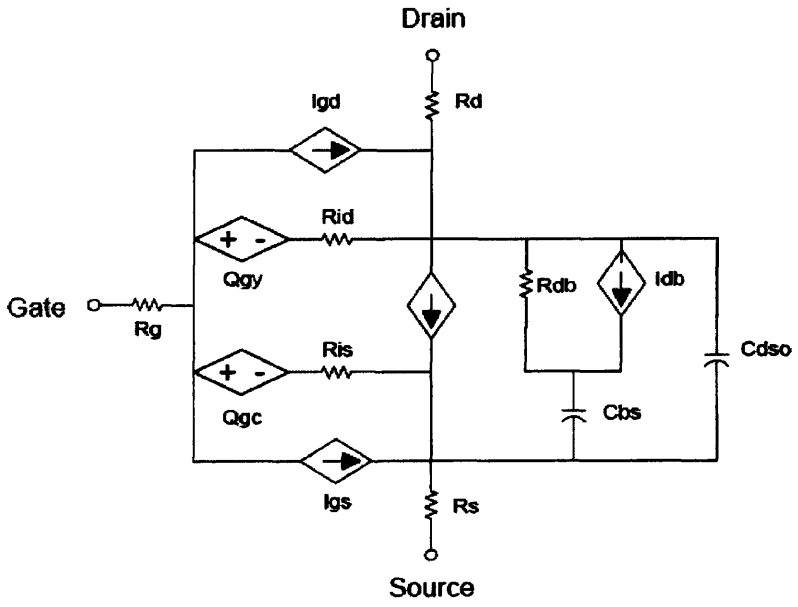


Figure 4.8 EE-HEMT nonlinear large-signal equivalent circuit model.

The theory is that the capacitance changes more before the knee voltage than after, similar to the characteristic of the drain current. If the derivatives of the drain current equation are not accurate, harmonic predictions such as intermodulation distortion could be invalid. Another aspect considered is the transconductance peak versus gate voltage that is particularly important for HEMTs.

4-5-2 EE-HEMT nonlinear large-signal model

The nonlinear model chosen for this work is Agilent's EE-HEMT large-signal model, Figure 4.8, an empirical analytic model developed for the purpose of fitting measured electrical behavior of GaAs FETs and HEMTs. The large-signal modeling process was carried out using Agilent Technologies' modeling and measurement automation software package, IC-CAP; however, any other equivalent modeling software may be used. The fundamental FET's large-signal nonlinear models used by IC-CAP are the Curtice Quadratic model, Curtice-Ettenberg (Cubic) model, and the EE-HEMT model. The first two models are more suitable for GaAs-MESFETs devices, while the EE-HEMT model

can be useful for HJ-FETs (HEMT and pHEMT) device modeling because of its versatile nature that gives it all of the following features **[160]**:-

- An accurate isothermal drain-source current model that fits virtually all processes.
- Self-heating correction for the drain-source current.
- A charge model that accurately tracks measured capacitance values.
- A dispersion model that permits simultaneous fitting of high-frequency conductances and DC characteristics.
- A breakdown model that describes gate-drain current as a function of both V_{gs} and V_{ds}.
- The capability to extrapolate outside the measurement range used to extract the model.
- The model can be automated with extraction macros or the parameters can be extracted individually from measured data.

During the EE-HEMT large-signal model extraction, a series of different IC-CAP setups are used to measure current, voltage, and S-parameters under different bias and frequency conditions. The model parameters are then extracted from the various sets of measured data.

The extraction procedure is divided into measurement setups. Each measurement setup defines a set of measures that allow for the determination of data useful for the next setups and specific model parameters extraction. Successive setups depend on previous setups; therefore the order in which the setups are performed must be respected. The extraction procedure begins with the identification of the parasitic elements; since the successive setups depend on the parasitics previously extracted the parasitic identification is a key point for model extraction. Each setup has a set of dedicated functions (namely "transforms" in the IC-CAP environment) that allow for the extraction of each parameter used to describe elements of the equivalent circuit model. The setups also offer the possibility to optimize the extracted parameters; so it is possible to tune a specific equivalent circuit component without affecting the rest of the model and, therefore, the model must be re-extracted completely if it does not fit the desired measured characteristics.

The theory behind the EE-HEMT large-signal nonlinear model together with explanation for all measurement setups required, and the model parameters extraction techniques

are discussed in details in **[140, 160]** while definitions for all model parameters are given in Appendix-B.

4-5-3 EE-HEMT large-signal models extraction for our fabricated devices

The Agilent's EE-HEMT nonlinear large-signal model extraction technique discussed was applied for all fabricated samples, both of the old and new processes. The measurement setup used for the modeling purpose is shown in Figure 4.9, utilizing a Cascade Microtech probe station for room-temperature on-wafer measurements.

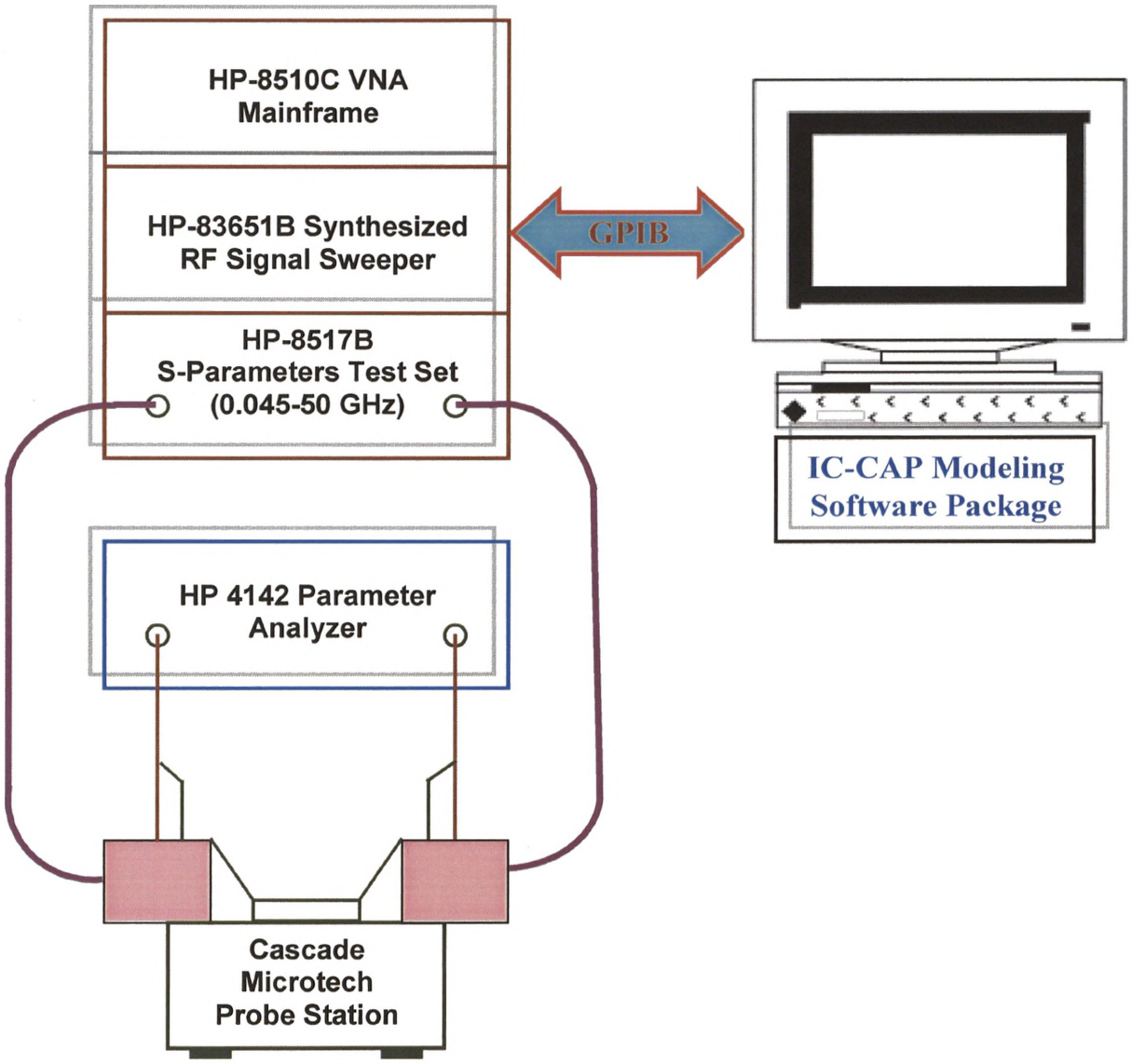


Figure 4.9 Measurement setup used for EE-HEMT large-signal model extraction.

An HP-8510C VNA for S-Parameters measurements (45 MHz-40 GHz) in conjunction with an HP-4142 parameter analyzer for DC measurements and all are automated by the Agilent's IC-CAP modeling software which is designed to meet all the nonlinear modeling requirements.

The large-signal modeling process has been carried out according to the following procedure:-

(a) Performing a set of device preview measurements and setting measurement variable values based on the results.

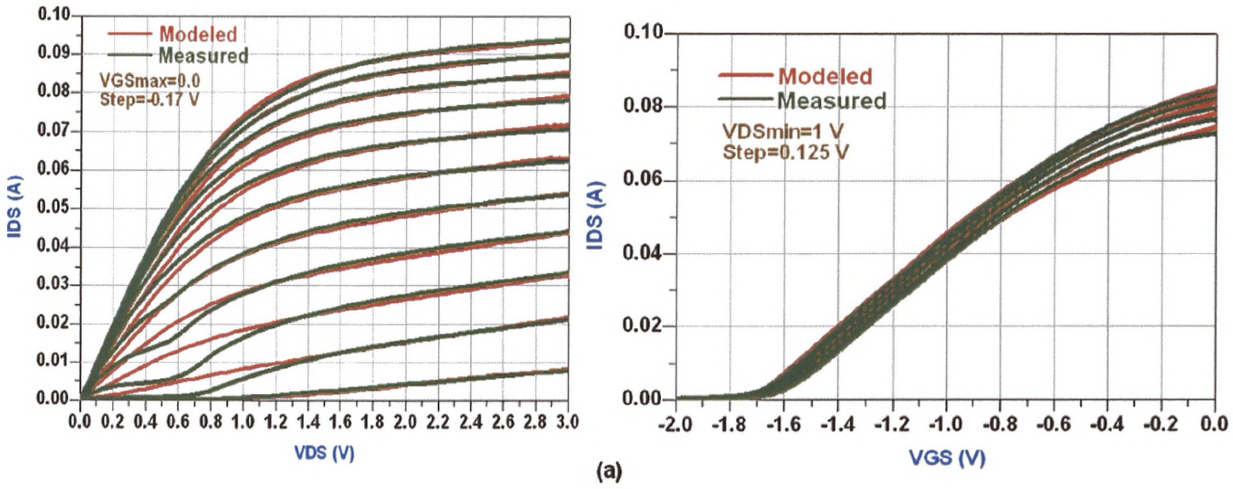
(b) Setting the hardware instrument states and input variables for each measurement.

(c) Making the parasitic, DC, and S-parameter measurements: qualifying the results.

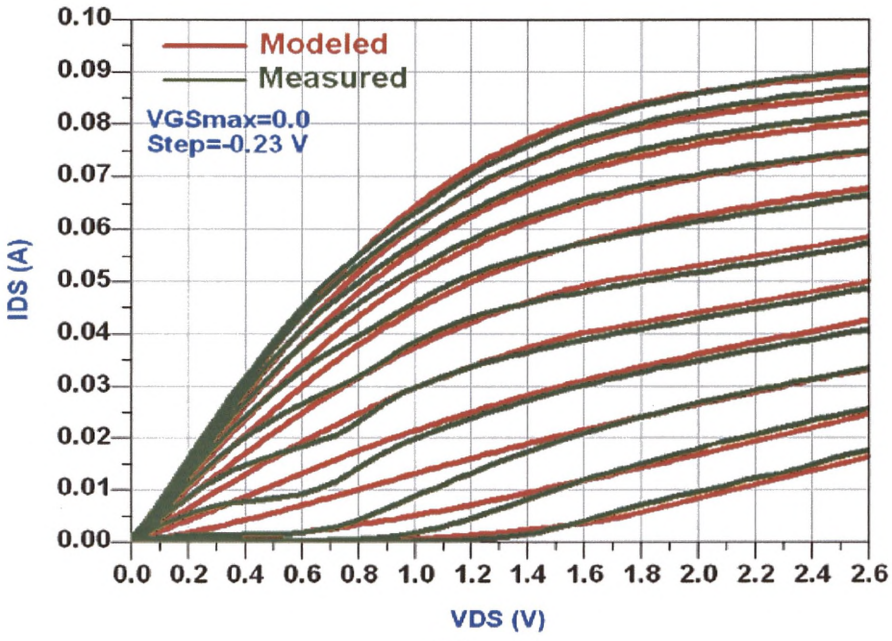
(d) Extracting the individual model parameters and then exporting them from IC-CAP to the ADS where optimization algorithms are applied until the modeled DC and RF characteristics of the devices accurately fit the measured data.

4-5-4 EE-HEMT large-signal model verification

The DC modeling section of the EE-HEMT model has provided a very good fit for the measured DC characteristics except of the knees area at higher V_{GS} values that suffer from Kinks. The Kink effect is the phenomenon which is more pronounced in the InAlAs/InGaAs pHEMTs **[163, 164]** and may be attributed to hot electron injection and trapping in the donor or buffer layers **[165]**, rather than impact ionization at certain V_{DS} values **[166]**, the issues that are not taken into account in the EE-HEMT model. Figure 4.10 gives an evidence of this , illustrating a comparison between the measured and modeled common-source IV characteristics of a 2x100 μm device from sample VMBE-1831 (old process), Figure 4.10(a) and a 4x75 μm device of sample XMBE-106 (new process), Figure 4.10(b).



(a)



(b)

Figure 4.10 Comparison between measured and modeled DC characteristics of the fabricated devices (a) Sample VMBE-1831 (2x100 µm). (b) Sample XMBE-106 (4x75 µm).

Figure 4.11 shows the RF characteristics of the extracted EE-HEMT models compared with those measured for the same devices whose DC data are shown above. A good match has been obtained between the modeled and measured data except for the discrepancy with S_{22} at low frequencies and S_{11} above 20 GHz. This could be because the extraction of the model over bias may not fully reflect the proper output conductance

due to limitations in the DC model. In fact, this problem is much less pronounced in the small-signal models extracted before and more accurate fit could be obtained, this issue is not surprising because the small-signal models are always extracted and may be optimized for a single bias point unlike the large-signal models which should fit the measured data over a wide range of DC bias.

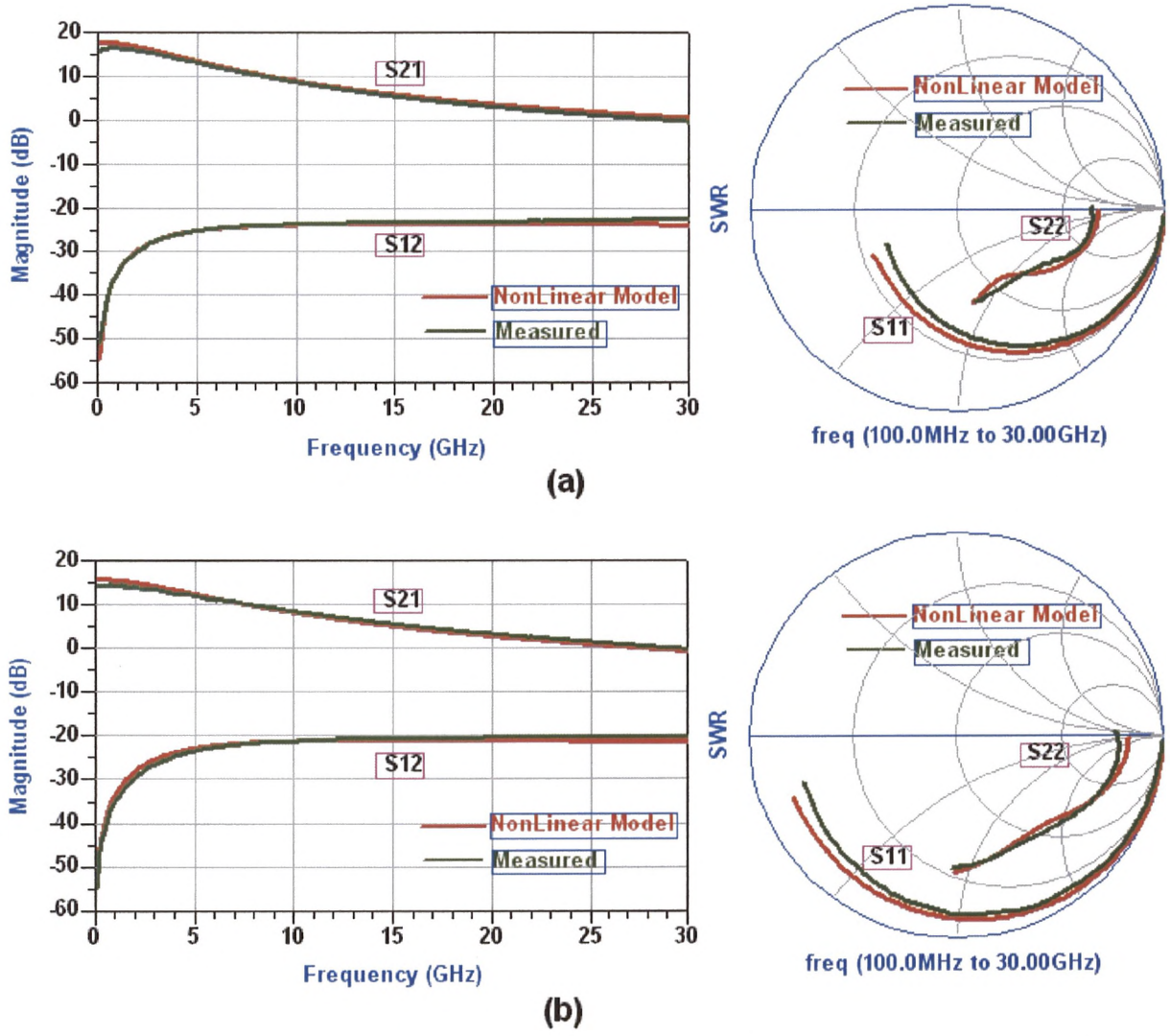


Figure 4.11 Comparison between measured and modeled RF characteristics of the fabricated devices (a) Sample VMBE-1831 (2x100 µm). (b) Sample XMBE-106 (4x75 µm).

Although there are many issues that could be discussed within the nonlinear large-signal modeling process ,we will only emphasis one of the major advantages of the EE-HEMT models which is their ability to predict (simulate) the noise behaviour of the devices over a wide range of frequencies and DC bias, *without any fitting parameters needed.* This issue will be discussed in details in the next section.

4-6 Noise Characterization for the Fabricated Devices

As was mentioned before, the main target of this study is the design and realization of a broadband MMIC LNA in the SKA frequency band based on the in-house fabricated 1 μm InGaAs/InAlAs/InP pHEMTs. Before starting the design process an investigation of the optimum device features for the best noise performance in such low frequency band was undertaken. For this purpose, the noise parameters of the fabricated and modeled devices have been calculated based on the small-signal and large-signal models obtained. The noise characterization of the devices has been achieved by two different techniques, briefly discussed here.

4-6-1 Noise parameters extraction technique

The first method used for noise parameters calculation is mainly based on Fukui's noise analysis (discussed in Chapter-2) and the small-signal model parameters extracted here. Since the noise figure of a FET is affected by both bias point and generator impedance, ***NFmin*** extracted here is an absolute minimum noise figure obtained by adjusting both bias and generator impedance. Recalling Fukui's expression for NFmin (equation 3.17), $NF_{min} = 10Log\left(1 + k_1 \frac{f}{f_T}\sqrt{G_m(R_s + R_g)}\right)$, the only unknown in this equation is the fitting parameter, k_1, and the only way to obtain its value is to compare this calculation with experimentally measured noise data.

Applying this technique for the fabricated samples and comparing the above expression with experimentally measured NFmin for a few devices over all samples, the best extracted values for the fitting factor, k_1, is 3.5-3.6 for all InP-based devices and 2.6-2.7 for the GaAs-based ones. However, this technique has not been applied for the noise resistance, R_n, calculations ($R_n = \frac{k_2}{G_m^2}$) because of two reasons; firstly the lack of

measured data and secondly the value of R_n fitting factor, k_2, itself is usually very small (0.08-0.1) which may lead to great uncertainties in the calculations obtained.
The second technique used for noise parameters calculations is to use the nonlinear large-signal models extracted on the IC-CAP and exported to the ADS as an efficient tool for simulating the noise performance of the devices depending on the fact that the ADS software package can be used to calculate the noise parameters from the large-signal transistor models already defined in its library if they accurately fit the RF characteristics of the devices under test **[167]**. As the EE-HEMT model is one of the default large-signal models on the ADS libraries, it will be used for this purpose based on the numerical analysis given in **[168]**.

4-6-2 Noise parameters calculation for the fabricated devices

The noise parameters calculation technique discussed has been applied for all of the fabricated samples in a wide range of frequency and DC-bias.
Table 4.6 shows NFmin, from the small-signal models, and R_n, from the large-signal models, for the old process samples (the same 200 μm devices whose linear models parameters given in table 4.1). From these results:-

- The lowest NFmin has been obtained for VMBE-1831, the sample with the lowest parasitic resistances and highest f_T.

- Despite its highest g_m and very high f_T, sample VMBE-1841 exhibits the highest NFmin because of its worst parasitic resistances.

- High noise resistances have been obtained for all samples (23-29 Ω) reflecting the difficulty of using these devices for LNA circuit design, the issue was discussed before in Chapter-3.

Sample →	VMBE-1831	VMBE-1832	VMBE-1841	XMBE-22
Bias Point	1.5, -1.5, 18.9mA	1.5, -0.6, 35.4mA	1.5, -0.5, 19.6mA	1.5, -1.2, 12mA
F_T (GHz)	38.4	29.4	36.34	33.2
NFmin@2GHz	0.824	0.937	1.126	1.1
R_n (Ω)	23.3	28.7	24.2	25.4

Table 4.5 Predicted room temperature noise parameters of the old process samples (device size 2x100 µm).

Figure 4.12 shows the room temperature NFmin simulations of the large-signal models illustrating the linear dependence of NFmin on frequency **[169]**, and the good match with linear model calculations.

Generally an equivalent noise temperature of 62 K - 87 K at 2 GHz was obtained for the old process devices, putting them very far from the SKA requirements for the individual devices (~ 35 K at 2GHz).

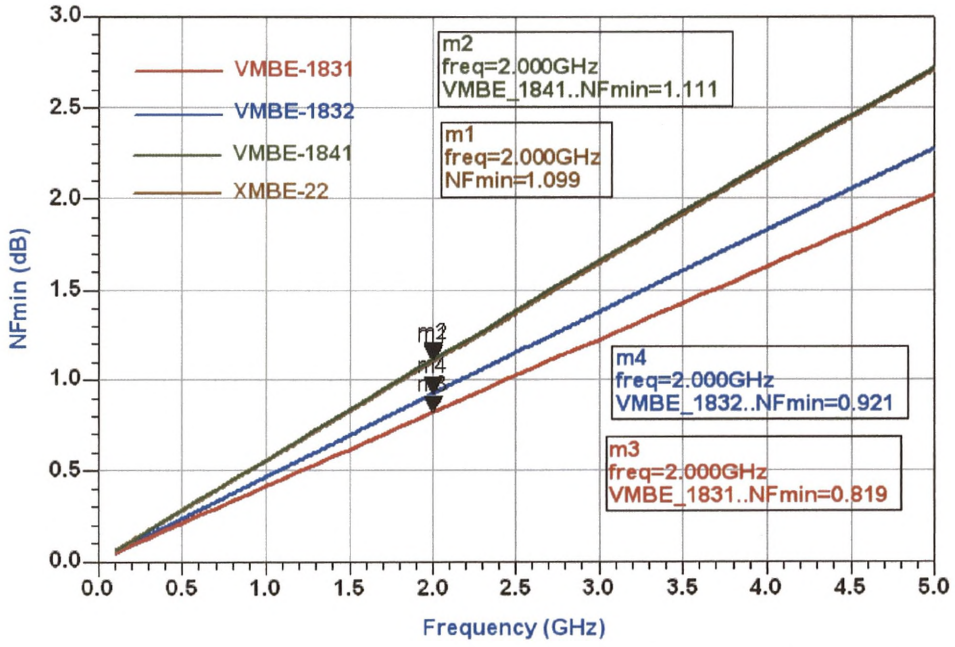


Figure 4.12 Room temperature minimum noise figures of the old process samples.

The predicted room temperature noise parameters of the new process samples are shown in Table 4.6. All devices are 2x200 μm with their small-signal models parameters given before in Table 4.2. From these results, one can easily recognize the great enhancement in the noise behavior of the new devices. An equivalent noise temperature of 41 K - 47 K is obtained at 2 GHz with noise resistances from 9.7 Ω to 12.6 Ω reflecting their much better parasitic resistances compared with the old devices even with lower transconductances or cut-off frequencies. However, a better noise performance may be obtained at different bias points rather than the maximum transconductance used here, especially for lower current values, a state that could be easily verified by extracting the noise parameters over a wide range of DC bias.

Sample →	VMBE-1841	XMBE-106	XMBE-38
Bias Point	1.5, -0.77, 20 mA	1.5, -1.4, 33mA	1.5, -1.4, 54 mA
F_T (GHz)	30.4	36.7	37
NFmin@2GHz	0.644	0.567	0.564
R_n (Ω)	9.7	12.6	-

Table 4.6 Predicted room temperature noise parameters of the new process samples (device size 2x200 μm).

The predicted room temperature noise parameters of the multi gate finger devices of sample XMBE-106 are shown in Table 4.7. The best noise performance among all of the fabricated devices has been predicted for these devices.

Size →	4x50	4x75	4x100	4x200	6x50	6x100	6x200
Bias Point	1.5 18 mA	1.5 23 mA	1.5 34 mA	1.5 60 mA	1.5 31 mA	1.5 37 mA	1.5 >100 mA
F_T (GHz)	27.3	28.8	34	38	33.4	32	36.4
NFmin@2GHz	0.408	0.448	0.483	0.554	0.426	0.517	0.67
R_n (Ω)	13.4	10.8	8.45	-	10.4	7.63	-

Table 4.7 Predicted room temperature noise parameters of multi gate finger devices sample XMBE-106.

Further improvement in the equivalent noise temperatures has been achieved, recording values from 29 K to 49 K for device sizes from 0.2 to 1.2 mm.

Finally, a further enhancement has been achieved in the noise resistance with the multi gate finger devices, having the lowest Rn between all device structures and achieving the second main goal of these devices.

4-7 Conclusions

In this chapter, an extensive experimental microwave characterization and device modeling, together with numerical simulations using suitable linear and non-linear transistor models has been carried out for our in-house fabricated 1 μm strained gate high breakdown InGaAs-InAlAs InP-based pHEMTs. Complete agreements with experimental data were found on different transistor processes. DC, RF, and noise behaviors of the new devices were successfully modeled.

- The old process samples, with thin gate metallization, have been realized to suffer a high amount of parasitics providing devices with relatively poor noise performance. Room temperature minimum noise figures of 0.825 -1.125 dB at 2 GHz with equivalent noise resistances of 23-29 Ω have been obtained for the 2x100 μm devices of this process. For these reasons, a lot of difficulties will be expected when using those devices for realization of LNA in the low SKA frequency band.
- The GaAs/AlGaAs devices, given in Appendix-D, have been shown to suffer the same amount of parasitics as the InP-based devices but with much worse noise performances due to their very low cut-off frequencies.
- The new process devices, with thick gate metallization, exhibit much less parasitic effects compared with the old process ones. Room temperature NFmin between 0.56 dB and 0.64 dB at 2 GHz together with equivalent noise resistance of 9.7-12.6 Ω has been predict for the 2x200 μm devices of the new process samples.
- Further improvement in the gate and noise resistances has been achieved with the multi-gate fingers utilizing the air-bridges technique making them best candidates for implementation in the low SKA frequency band.

CHAPTER-5

MMICs Design and Technology

5-1 Introduction

The monolithic microwave integrated circuits (MMICs) are analog integrated circuits that incorporate various active and passive components on the same semiconductor chip covering the microwave frequency range (300 MHz to 300 GHz). Such chips perform individually the microwave functions as amplification, mixing, switching, phase shifting, filtering, etc., or combine two or more of these functions (multi-function chips) **[170]**. The additional term 'monolithic' is necessary to distinguish them from the established microwave integrated circuits (MICs). Monolithic means an approach wherein all active and passive circuit elements or components and interconnections are formed into the bulk, or onto the surface, of a semi-insulating substrate by some deposition scheme such as epitaxy, ion implantation, sputtering, evaporation, diffusion, or a combination of these processes and others, while the conventional hybrid MICs consist of discrete active devices and passive components integrated together onto common substrate using solder paste or conductive epoxy **[67]**. MMICs were born in the early 1960s out of design research for military and aerospace applications. Their small size, lower power consumption, high reliability and optimum performance made them very attractive for cutting-edge applications. Over the next several years, MMICs remained confined to aerospace and military applications, and only recently, have they begun to penetrate the commercial high-frequency wireless

markets. The demand for high-performance/low-power consumption devices for cell-phones, wireless-Local Area Networks (LAN), Local Multipoint Distribution Systems (LMDS) and the emerging wireless-Wide Area Networks (WAN) has brought MMICs into the commercial market spotlight.

MMICs pose a different set of design challenges than those of traditional analog/digital circuits. At frequencies ranging from 2 to 40 GHz and beyond, physical parasitic effects play a prominent role. This, coupled with other important factors such as the equally important roles of active and passive components, component proximity and inter-connects, high circuit analysis complexity and process variations, presents a tremendous challenge to those seeking top design performance in the microwave frequencies and this means that MMICs have a special range of applications and that MMIC design is very different to conventional VLSI design, in which CAD offers a high degree of layout automation **[38]**.

5-2 Brief History of MMICs

The concept of MMIC is not new; its origin dates back to 1964, when the first MMIC design introduced, based on Si technology, as a transmit– receive module for an aircraft phased-array antenna. The results were disappointing because of the inability of Si to maintain a high resistive state through the high temperature diffusion processes and thus very lossy substrates resulted, which were unacceptable for microwave circuitry **[171]**.

The technology was revived again in 1968 when Mehal and Wacker used a semi-insulating GaAs as the base material, Schottky barrier diodes, and Gunn devices to fabricate a 94-GHz receiver front end **[172]**. However, it was not until Pengelly applied this approach based on GaAs MESFET as the key active element that the present intense activity began. It was the rapid development of GaAs material technology, namely Epitaxy & Ion-implantation and the fast evolution of the GaAs FETs based on metal Schottky gates that brought the MMIC technology revival and gave it its great progress.

In 1975, Ray Pengelly and James Turner introduced the world's first transistor- based MMIC **[173]**. It was a single-stage GaAs-FET amplifier providing 5 dB of gain at X-band using 1 micron optically-written gates. They used computer optimization to design their

lumped element matching structures, with integrated loop inductors and inter-digital capacitors, but no DC blocking on the input/output. Backside processing had not yet been worked out, so the FET's source was grounded externally. Few years later, the first power MMIC amplifiers were introduced. They were two-stage X-band push-pull power amplifier, reported by Texas Instruments in 1979 **[174]**, and a one-stage X-band single-ended power amplifier, reported by Raytheon later in the same year **[175]**. Those amplifiers combined GaAs MESFETs for active elements and transmission lines and MIM capacitors for low-parasitic passive elements on the same semi-insulating substrate. Then, Joshi et al **[176]** presented results of the first FET oscillator MMIC, operating in Ku-band.

After these early GaAs-MMIC successes, the fundamental superiority of GaAs for MMICs have led to an explosion of that technology in the past ten years and IEEE has established a symposium dedicated to GaAs IC developments, 1979. Thousands of papers have been published since then, many resulting from advances in the device technologies which have yielded higher frequencies and better performance. Some of these papers attracted world-wide interests and their contributions became real milestones in the history of MMIC development. Further details about most of these papers are reported in **[67]**.

Strictly speaking, the extensive use of GaAs in the development of MMICs was attributed to many reasons;

- GaAs has higher electron saturation velocity as well as higher low field mobility than Si. This higher electron mobility is the fundamental property that enables higher frequencies of operation and faster switching speeds.

- GaAs can be readily made with high resistivity making it a suitable substrate for microwave low loss passive elements.

- The high-resistivity semi-insulating property of GaAs cross-talk between different devices integrated together.

5-3 Advantages and Disadvantages of MMICs

MMICs have been widely used for many different applications, since the technology meets the front end receiver requirements such as compact area and high reliability. Moreover, to obtain wide frequency band characteristics with high reproducibility and performance uniformity, MMIC technology must be the best candidate **[177]**. Generally, when compared to the other microwave technologies, the MMIC technology offers all the following advantages:

(1) Small size and light weight, making them suitable for many applications that require compact designs like space-born applications, smart cards, and radio transceivers for modern communication systems and mobile phones.

(2) Low cost for medium to large scale of volume production.

(3) Enhanced reproducibility from uniform processing and integration of all parts of the circuit.

(4) Enhanced reliability from integration and process-control improvements.

(5) Enhanced broadband performance due to the elimination of wire bonding and the embedding of active components within a printed circuit that highly reduces many of the undesired parasitics.

(6) Design performance realized without several iterations—the result of processing and material repeatability, and computer-aided design enhancement.

All of the above advantages contribute to the successful achievements of the primary MMIC technology goal of producing advanced microwave and millimeter wave circuits affordable for wide usage in many different systems.

On the negative side, the following drawbacks or disadvantages are pointed out for the MMIC technology;

(1) The post-processing tuning is always very difficult, almost impossible, therefore the design of the MMIC must be based on very accurate physical and electrical models for

both active and passive elements, including dispersion effects due to fabrication process tolerances.

(2) Because of the small chip area, the MMIC process usually offers a limited choice of components and suppression of undesired RF coupling (crosstalk) between different elements is not possible most of the time.

(3) Difficulty of integrating high power sources limits the power handling capabilities of the MMIC chips.

(4) It is always very expensive to start-up the MMIC fabrication process for mass production. Further, the complexity of MMIC fabrication process leads to extremely long iteration times.

A comparison between the MMIC technology and the conventional hybrid MIC technology is shown in table 5.1.

	MMICs	Hybrid MICs
Cost	Cheap in large quantities	Cheaper for simple circuits; automatic assembly is possible
Reproducibility	Very good reproducibility	Poor reproducibility due to device placement and pond-wires
Size and Weight	Small and light	Not very large anyway
Reliability	Reliable	Suffer reliability because all components must be fixed by soldering
Bandwidth	Less parasitics –more band-width and higher frequencies	The best transistors are always available for LNAs and HPAs
Space	Space is at a premium; the circuit must be as small as possible	Substrate is cheap, which allows microstrip to be used abundantly.
Components varieties	Very limited choice of components	A wide selection of devices and components is available
Processing cycle	Long turn around time (3 months)	Can be very fast (1week), making redesigns easy
Technology	Very expensive to start up	Very little capital equipment is required

Table 5.1 Advantages and disadvantages of MMICs compared with hybrid MICs [67].

5-4 MMICs Applications

MMIC technology was born out of the need for high-performing wireless designs for military and aerospace applications. The technology is suitable for transponders which needs small size, light weight, and high reliability. Recently, many satellite communication systems with higher capacity have been proposed for new generation communication services in K- to Ka-band. In such systems, MMICs are expected to be the key components of highly complex TX and RX modules in active phased array antenna (APAAs). HJ-FET devices for MMICs are very promising to improve efficiency of the high power amplifiers (HPA) and noise figure of low noise amplifier (LNA) **[1]**. Consideration is given to performance enhancement in future communications satellites with MMIC technology insertion, application of Ka-band MMIC technology for an Orbiter/ACTS communications experiment, a space-based millimeter wave debris tracking radar, low-noise high-yield octave-band feedback amplifiers to 20 GHz, quasi-optical HJ-FET VCOs, and a high-dynamic-range mixer using novel balun structure. MMIC technology will have a dramatic impact upon future radar, electronic warfare, and communication systems which utilize phased arrays , a case in point being the SKA. Systems in both the commercial and defense industries which require large quantities of densely packed circuitry will become the prime benefactors of MMIC technology. However, receivers and transmitters for communication systems, phased-array antennas, sensors and radars that operate at high frequencies are just few examples of systems that use MMICs. Table 5-2 summaries the main MMICs' applications in civil, military and space fields **[67, 178-184]**.

Civil Applications	Military Applications	Space Applications
•Direct broadcast satellite (DBS) down-converters. •Smart cards, cellular telephone transmitters and mobile phones. •Wireless LANs. •Global positioning system (GPS). •Personal communication networks (PCNs). •High speed internet access. •Fiber-optic systems. •Medical applications.	•Radar systems •Electronic warfare •Smart weapons •Air-defense systems (ground stations +guided missiles •Remote sensing •Decoys	•Satellite communications •Navigation systems •Radio astronomy applications •Wide-band radiometers •On-board air-craft equipments

Table 5.2 Main Applications of MMICs.

5-5 Coplanar Waveguide MMICs

As a result of the efforts spent in reducing chip sizes and increasing operating frequency of MMIC chips into the millimeter-wave band, there has been widespread development of circuits employing **CoP**lanar **W**aveguide (CPW), slotline, and coplanar strips. The major attraction of these uni-planar techniques is that the expensive backside processing and the difficult via etching in the microstrip case are no longer needed. This is attributed to the structure of the CPW transmission line, Figure 5.1, which consists of a signal conductor placed between two ground planes, all placed on top metal layer of the substrate, and since the dominant mode of the CPW is the quasi-TEM there is no low frequency cut-off **[185, 186]**.

In fact, the use of the CPW structure in the MMICs has all the following advantages over the traditional microstrip lines **[187, 188]**:

•Both signal and ground conductors are placed on the same side of the wafer. Therefore, three additional time-consuming processing steps can be avoided: wafer thinning, via holes etching and backside metallization. This reduces cost and enhances process yield.

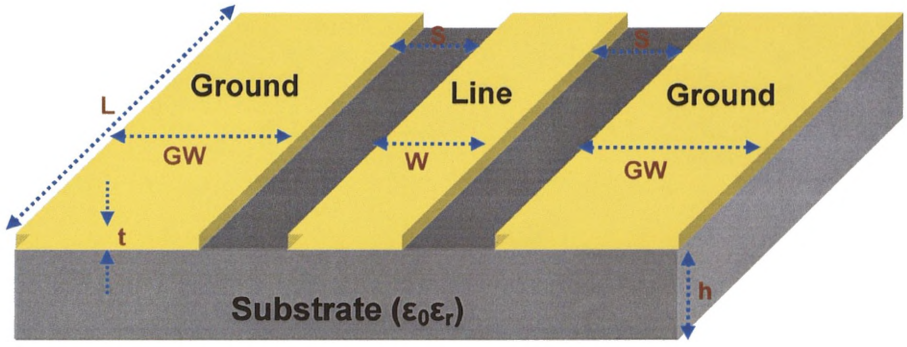


Figure 5.1 CPW Transmission line structure.

•The ground plane is accessible at the front side of the wafer, allowing easy parallel implementation of passive and active elements. For FETs, this is especially advantageous at very high frequencies, where a higher gain can be obtained due to the absence of a via-hole inductance at the source. In addition, with the absence of the back-side ground plane, lumped elements exhibit less parasitic capacitance.

•A given characteristic impedance can be realized with almost any track width and gap combination, which can help reducing the circuit size by 30%.

•Coplanar lines can have a low dispersion: a variation of the effective dielectric constant as low as 2% has been reported for frequencies up to 60 GHz. This feature is important for broadband applications.

•Due to the smaller difference in even- and odd-mode velocity in coupled coplanar lines, a coupled line directional coupler realized in a coplanar technology leads to a better directivity and performance over a broader frequency range than a microstrip version.

•The presence of the ground plane results in a reduced coupling between adjacent lines which enables a further miniaturization of MMIC circuits and then a higher packing density is possible **[189]**.

•The coplanar MMIC is compatible with alternative packaging methods such as flip-chips **[190, 191]**.

•A well-established on-wafer measurement technique based on coplanar probe tips is commercially available, facilitating easy and accurate measurements.

On the minus side, the CPW design usually results in slightly higher losses, especially for lower frequencies, and lower power handling capabilities. In fact, the main problem associated with the CPW lines is that the mode of propagation can easily degenerate from quasi-TEM into a balanced coupled-slotline mode. This happens very often at discontinuities, but can be avoided by incorporating grounding straps between the ground planes, using either air-bridges or underpasses **[192]**.

Although there are many encouraging activities and promising results in CPW design, this technique has not yet achieved the expected breakthrough. The main reason for that is the lack of a complete, accurate CAD oriented software packages containing full libraries of CPW elements. At present there are four possible techniques for the design of the CPW circuits briefly will be discussed here.

(1) Measurement based Modeling, in which a great number of test structures have to be realized and measured. The measured data are then used for the modeling of these structures. This technique has the advantage of great accuracy, but this accuracy is limited to certain dimensions and substrate parameters and the results are only valid for the measured frequency range. The realization and measurements of the test structures take too long time and relatively high cost.

(2) Full-wave EM-field analysis, which is an alternative solver that overcomes the problem of the cost and limitation of validity range. But, the use of such tools is very complicated and simulation time is too long. Good examples of these are the 3-D Ansoft's HFSS™ that computes 3-D fields and currents associated with 3-D structures and the Agilent's Momentum simulator for ADS which computes 3-D fields but only allow 2-D conductors and currents on planar layers, that is why such type of simulators called 2.5D planar simulator).

(3) Analytical approximation, which is another method often used for simulating CPW structures employing some numerical techniques like the finite-difference time-domain (FDTD) or the integral equations technique. However, there is only a few numbers of such approximations available for CPW structures and they are not sufficient for complete and complex MMIC design.

(4) CAD software packages that enable the designer of CPW circuits to simulate and optimize the circuit parameters in relatively short time. There is no limit due to structure dimensions and results are usually accurate for a wide range of frequencies. Unfortunately, there are very few CAD packages that contain full libraries for CPW components and so they are very expensive. The IMST's COPLAN for ADS™ library is the most prominent example of these.

5-6 Passive Components for MMICs

It is the extensive use of passive components that makes MMIC design so different to conventional integrated circuit design and layout. Besides being critical for circuit performance and reliability, passive elements also determine the circuit's bandwidth, center frequency, and other important electrical characteristics. Besides connecting the various active elements together, passive components are used for impedance matching, DC biasing, phase shifting, filtering, and many other functions in the MMICs. Besides the basic lumped elements inductors, capacitors, and resistors, passives also include a wide range of distributed transmission line components such as bends, Tee-, cross-junctions, as well as standard building blocks like transformers, couplers and power splitters/combiners.

Due to the fact that lumped elements are not purely inductive, resistive, or capacitive, but have aspects (parasitics) of all three, there are relatively few design equations in the descriptions of the passive components and hence they are very process-dependant. For a particular MMIC fabrication process the manufacturer's design manual is the essential authority on the exact design rules for component layout as well as the appropriate design curves and equations. Nevertheless, in many cases the design manual is little more than a reference guide to the process data, and accurate physical models based on practical measurements of the fabricated components are still needed to avoid significant errors in circuit design.

A brief description of the basic passive elements for MMICs, spiral inductors, MIM capacitors, and thin film resistors, will be introduced here. Their design, modeling, in-house fabrication and measurements will be discussed in details.

5-6-1 Spiral inductors

Inductors are usually used as circuit components, matching networks, DC biasing chocks playing a significant role in the realizations of compact size MMICs. In the low-microwave-frequency, monolithic approach, low loss inductors are essential for developing compact, low cost low noise amplifiers and high power-added-efficiency amplifiers. In MMICs, inductors may be realized in many different forms such as straight narrow tracks (ribbon inductors), single-loop inductors, or multi-turn spiral inductors.

Ribbon inductors, also known as distributed inductors, are realized by a section of high impedance transmission line. These inductors are limited to inductance values below 1 to 2 nH because of the high losses associated with the long lengths of high-impedance transmission line, while the line length itself is limited by the chip size and line width is determined by the fabrication limits. Ribbon inductors are relatively 'pure' inductors with very low parasitics and hence they are often used in distributed amplifiers where very large bandwidths are required.

Single-loop inductors were used extensively in the pioneering days of MMIC technology. This is probably because the processing, at the beginning, didn't offer air-bridges for spiral inductors. In recent years, loop inductors have been used very little because of their inefficient use of chip area. A number of papers give useful design equations for loop inductors.

Spiral inductors are typically comprised of a transmission line in a spiral shape and can be realized in many different shapes such as rectangular, circular, hexagonal and octagonal but, for this study, our interest will be mainly in the rectangular spiral inductors that are the most commonly used in modern MMICs.

5-6-1-1 Spiral inductors description

A typical spiral inductor is shown in Figure 5.2. The total inductance is a result of the self-inductance of the high-impedance transmission line and the mutual inductance created by the electromagnetic coupling between the closely spaced lines.

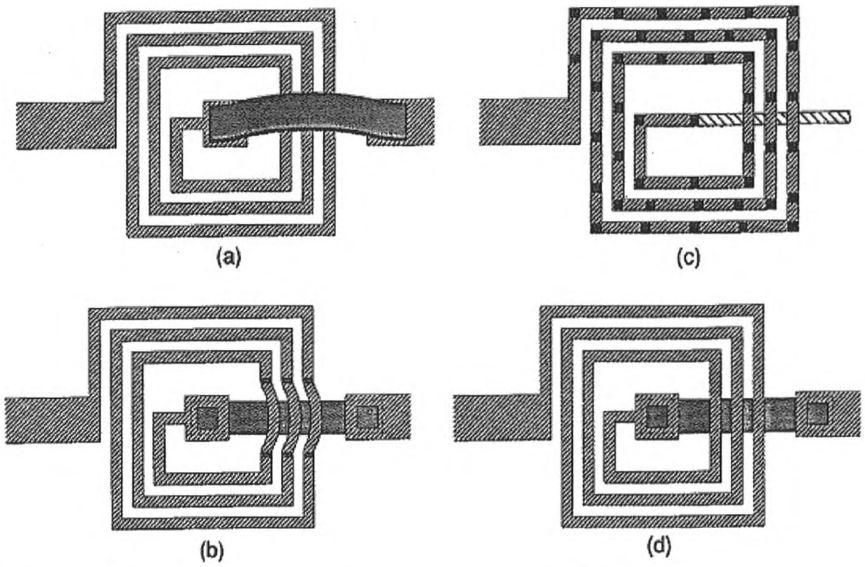


Figure 5.2 Spiral Inductor (a) Single air-bridge (b) Air-bridges over an underpass (c) Formed entirely of air-bridges; (d) Using two metal levels for an underpass [67]

The requirement to connect the center tap of the spiral inductor back to the outside circuit is one of the most famous processing difficulties of spiral inductors. Practically, there are two different forms for this fundamental connection either by using crossover air-bridges or dielectric spaced underpasses. Air-bridges may take three different forms, as shown in Figure 5.1a,b,c, but they always add more complexities to the processing cycle and sometimes their use is limited by the fabrication technology or reliability issues.

The alternative to using air-bridges is to employ a two-level metal process with a spacer dielectric. Polyimide is often preferred for its low ε_r and because thick films can be deposited very quickly. In this type of inductors, Figure 5.1d, the spiral turns are normally on the top metal layer above the dielectric so that the coupling to the substrate is minimized hence parasitic capacitance is reduced and so that the turns can be plated up for less resistance. The underpass is necessarily of a much thinner metal, and may thus be made quite wide to maintain a usable current carrying capability and to minimize the series resistance. The connection between the upper metal and the underpass is made through a via in the dielectric. These vias should not be confused with the through-substrate vias used for grounding requirements. This is the preferred process technique used for our in-house fabrication of spiral inductors reported in here.

5-6-1-2 Spiral inductors design

During the design of spiral inductor, three parameters are usually employed as figure-of-merits, namely, inductance (L), quality-factor (Q), and the self-resonant frequency (SRF). Spirals are usually designed for a certain desired inductance with the highest possible quality factor and the operating frequency which must be far enough from the SRF. Thus, these parameters should be accurately calculated because they determine the performance of the inductors.

(1) Inductance (L)

Many classical formulas are given for the calculation of the inductance of the spiral inductor depending on its physical dimensions such as track width (W), separation (S), number of turns (N), outer diameter (D), and the total length of the spiral line (L_{tot}) **[193, 194]**. During this work, the formula provided by **[195]** is used.

Also the inductance value can be extracted from the measured S-parameters of the two-port inductor after transferring them into Y-parameters **[196]**.

$$L = \frac{\mathrm{Imag}\left(\frac{1}{Y_{21}}\right)}{2\pi f} \qquad (5.1)$$

In practice it was found that whatever expression was used for calculating L, they all give very close values at lower frequencies that are very far from the first SRF, and of interest to the work presented here.

(2) Q-Factor

There are several definitions for inductor's Q-factor, but the most fundamental definition is the one proportional to the ratio of energy stored to the energy lost in the internal series resistance, R_S, per cycle in the inductor. Q-factor can be mathematically expressed as:

$$Q = \frac{wL}{R_S} \tag{5.2}$$

The Q-factor estimated by the above expression is not very accurate because it does not include the effect of all parasitics, so it is better to use the measured two-port parameters for more accurate calculations. Q-factor is defined as the ratio of the imaginary part to the real part of the input impedance (Z_{in}) at port-1 when port-2 is unloaded **[197]**.

$$Q = \frac{\text{Imag}(Z_{11})}{\text{Real}(Z_{11})} = \frac{\text{Imag}(1/Y_{11})}{\text{Real}(1/Y_{11})} = -\frac{\text{Imag}(Y_{11})}{\text{Real}(Y_{11})} \tag{5.3}$$

(3) Self-Resonance Frequency

At a certain frequency, resonance will occur due to the parasitic effects of the substrate and the distribution characteristic of metal tracks. When self-resonance happens, the inductive reactance and parasitic capacitive reactance become equal. After the SRF point, the inductor has a negative reactance value, thus behaves as a capacitor. Usually, the inductors are required to operate at frequencies far from their SRF. At resonance, the imaginary part of the input impedance is equal to zero, so the SRF can be determined graphically as the point where S_{11} trace crosses the horizontal axis on the Z-Smith Chart **[198]**.

5-6-1-3 Spiral inductors modeling

Although the spiral inductor is easy to fabricate, it is one of the most difficult devices to theoretically model because of the coupling between adjacent lines. Therefore, experimental characterization is usually required.

(a) Physical modeling

Generally, the basic equivalent circuit model of the spiral inductor, Figure 5.3, consists of a primary inductance (L_s) along with its associated series resistance (R_s), inter-turn and cross-over feedback capacitance (C_p) and some capacitance to ground stands for the

capacitive coupling between the spiral and the lossy substrate (C_{in} & C_{be}). It is more common, however, for the equivalent circuit data to be found for a number of different inductor geometries, and to use empirical curve-fitting expressions for the values of the equivalent circuit elements. However, expressions for calculating the lumped elements values of the equivalent circuit model shown below as a function of the spiral inductor's geometrical dimensions are given by **[199]**.

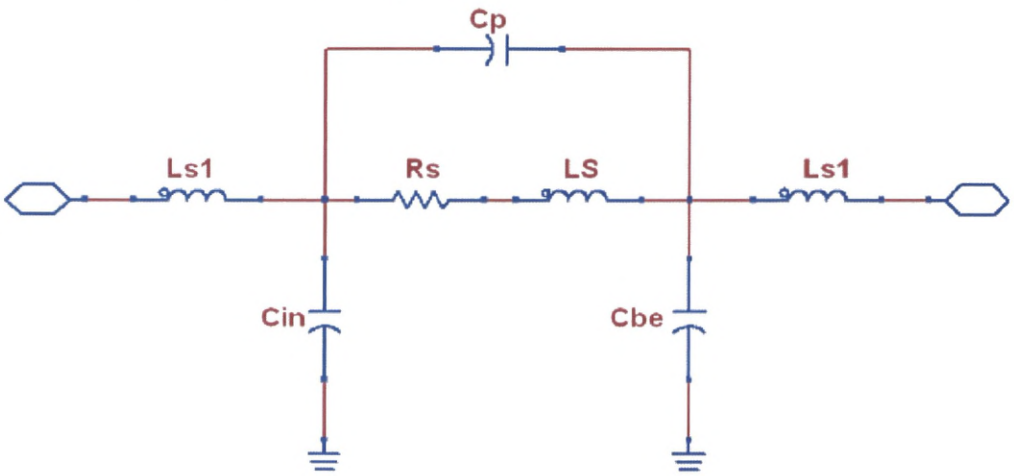


Figure 5.3 Spiral Inductor Equivalent Circuit Model.

(b) Electromagnetic simulation

An attractive alternative for the physical modeling is based on the use of electromagnetic simulation tools that allow predictive design. This is a process where the behavior of the electrical spirals can be predicted without the need for expensive and time consuming trial and error fabrication and measurement methodology. Simulation tools allow a designer to characterize a virtual spiral, which is defined in a layout drawing environment. Most electromagnetic simulation tools produce frequency dependent S-parameters and are therefore virtually equivalents to the measurement-based technique. Other advantages of the simulation-based approach are that the designer has more flexibility to try variations of the spiral layouts or even optimize the spiral layouts so that a desired behavior is obtained **[200]**. The design cycle is also much shorter than wafer processing runs. Several commercial electromagnetic simulation tools are available. They may be based on different electromagnetic simulation technologies such as finite-difference time-domain, finite element, or method-of-moments. The last one starts from

an integral equation formulation of Maxwell's equation with the currents flowing on the metallization as basic unknowns. This integral equation is solved for the currents flowing on the metallization surfaces. The concept of Green functions is used to characterize the behavior of the substrate, including the electromagnetic effects in the GaAs material. Capacitive coupling to the substrate, as well as magnetically induced eddy currents are taken into account in this manner **[201]**. During this work, in conjunction with the physical modeling technique described, extensive use of the Agilent's Momentum simulator for ADS was made to perform electromagnetic simulation for the physical layout of the designed CPW spiral inductors for accurate and dependable characterization of these elements.

Figure 5.4 illustrates an example of the CPW spiral inductor structures used for Momentum simulation, showing the mesh definition including the edge effects and input/output CPW ports. In this structure, N = 7, W=12 μm, S=10 μm, D = 320 μm, L = 6.2 mm, and the total area of the structure is 1.2 mm^2. All results of this simulation compared with the characteristics of the spiral inductor's equivalent circuit model and the measured data of the fabricated inductor will be introduced in the next sub-section.

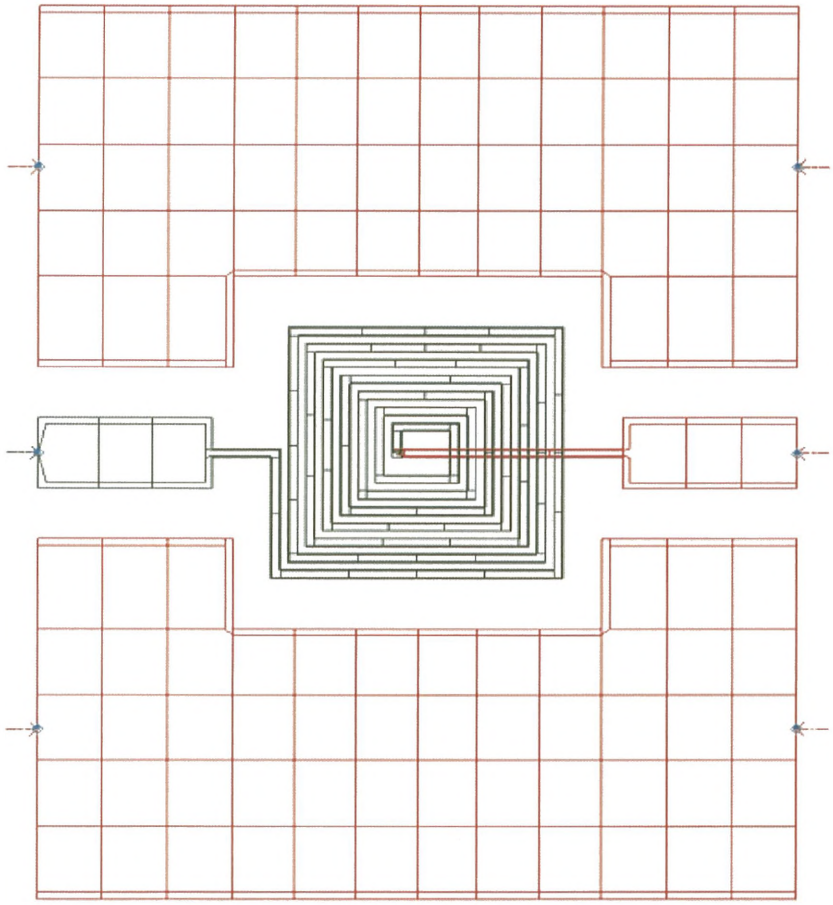


Figure 5.4 Spiral inductor's CPW structure used in the Momentum simulation on the ADS with Mesh definition and CPW ports (Total area =1.2mm^2).

5-6-1-4 Spiral inductors fabrication and measurements

During fabrication of the designed spiral inductors, a thin layer of Ti/Au (0.5 μm thick) was deposited on top of a GaAs semi-insulating substrate forming the underpass connection of the inductor. Then a thick layer of polyimide (0.9 μm thick), representing the dielectric, was deposited covering the first metal layer. A thick layer of Ti/Au (1 μm-thick), representing the spiral itself, was deposited on top of the polyimide after opening vias (windows) on the polyimide layer to allow connection between the bottom metal layer (underpass) and the centre of the spiral on the top layer.

In this work, the formula provided by **[195]** was used for the design of six different rectangular spiral inductors covering the inductance values that might be encountered in the MMIC LNA design (2.5 to 21.7 nH), and the fabrication process stated above was

applied. Inductance values and geometrical dimensions of the spirals as well as values for the lumped element equivalent circuit models are given in table5-3.

Inductance (nH)		2.5	4	10	15	18.6	21.7
No of Turns N		3	4	7	8	6	7
Line width W(μm)		10	10	12	8	8	8
Line separation S(μm)		10	10	10	10	8	8
Outer diameter D(μm)		220	250	350	350	400	400
Total length of line L(mm)		1.85	3	6.2	7.4	8.1	9.6
Spiral Inductor Model Parameters	L_s (nH)	2.4	3.778	8.89	12.63	15.88	17.78
	L_{s1} (nH)	0.052	0.115	0.559	0.983	1.28	1.76
	R_s (Ω)	7.45	10.3	17.12	27.85	31	35.27
	Cp (fF)	34	38	47.32	35	38	38.45
	C_{in} (fF)	36.48	59.55	123.84	117.68	114	123.4
	C_{be} (fF)	23.27	38.43	82	79.8	75.82	83.12

Table 5-3 In-House fabricated spiral inductors with their equivalent circuit model parameters.

On-wafer S-parameters measurements were carried out between 0.45 GHz and 15 GHz using an HP8510C vector network analyzer and Cascade Microtech RF probe station and basic quantities such as inductance values, Q-factors, and SRFs, which in general are function of frequency, were derived from the measured data. An Electromagnetic simulation for the designed inductors has also been performed using the momentum simulator on the ADS.

Excellent agreement was obtained between the measured and modeled data confirming the validity of the used circuit model and the Momentum simulation setup as shown in Figure 5.5 and Figure 5.7 for the 2.5 nH and 10 nH inductors respectively.

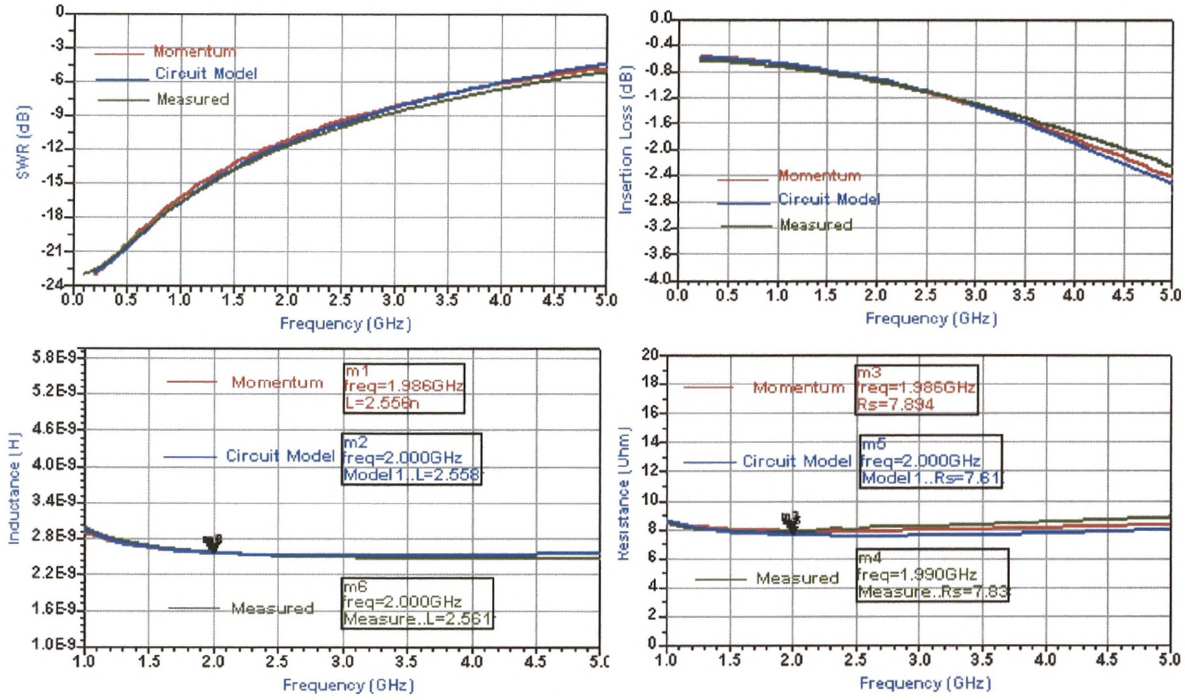


Figure 5.5 Comparison between the measured and modeled data for the 1μm-thick, 2.5 nH inductor.

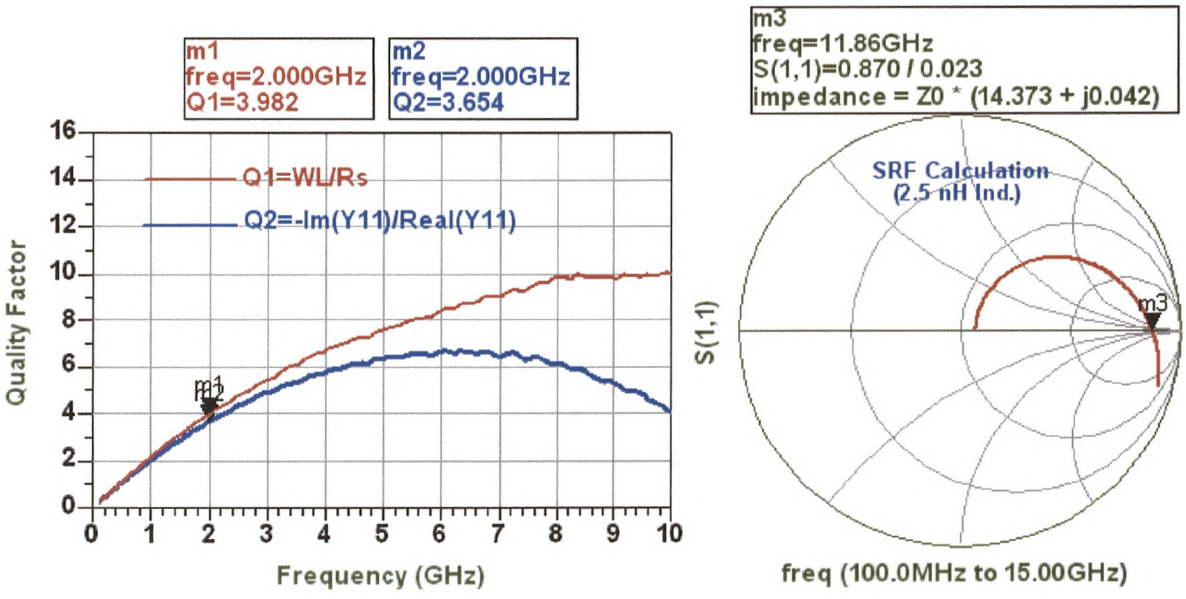


Figure 5.6 Quality factor and SRF calculations for the 2.5 nH inductor.

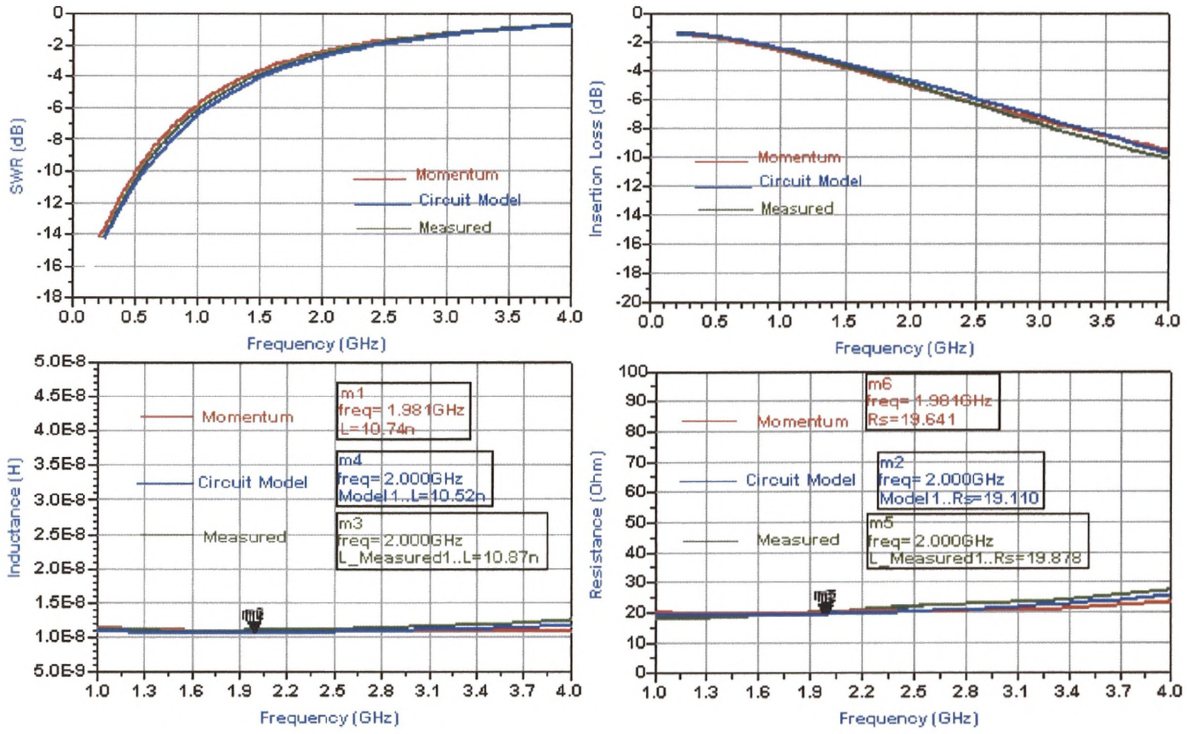


Figure 5.7 Comparison between the measured and modeled data for the 1μm-thick, 10 nH inductor.

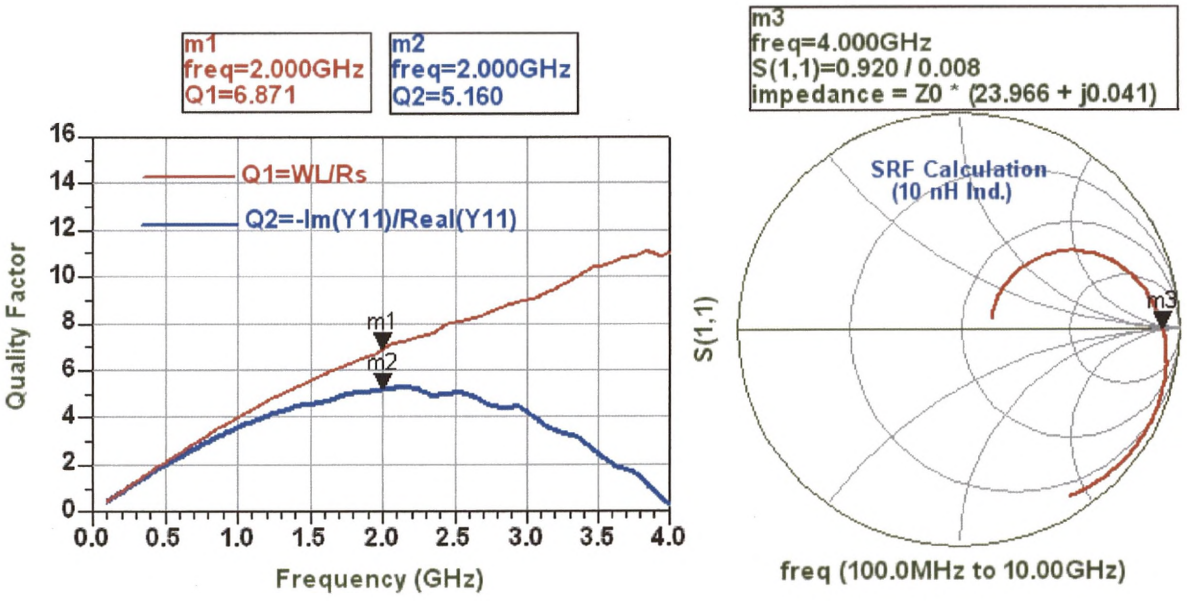


Figure 5.8 Quality factor and SRF calculations for the 10 nH inductor.

Low series resistance values have been obtained for the 1μm-thick fabricated inductors ranging from 8 Ω for the smallest inductor (2.5 nH) up to 35 Ω for the largest one (21.7 nH), representing one of the best results reported for this relatively thin metal thickness and promising for lower series resistance for thicker metal thicknesses as predicted from the extensive electromagnetic (Momentum) simulations performed.
The Q-factors of the fabricated inductors have been extracted from the measured data using the two different methods stated before and the following features have been noticed:-

•High Q-factors have been obtained ranges from 3.65 up to 5.7 @ 2 GHz.

•The difference between the methods of calculating Q is very small at low frequencies (up to 2 GHz) while it starts to increase at higher frequencies where the effect of parasitics is more pronounced, as shown in Figure 5-6 and Figure 5-8 for the 2.5 nH and 10 nH inductors.

The SRF of the fabricated inductors has been extracted from the measured S-parameters by the technique mentioned before and they were found to be high enough for safe operation at the low SKA frequency band. First SRFs of 11.86 GHz and 4 GHz were been obtained for the 2.5 nH and 10 nH inductors respectively as shown in Figure 5.6 and Figure 5.8. The first SRF of the largest fabricated inductor (21.7 nH) is 3.1 GHz.
Finally, spiral inductor models which express the practically fabricated inductors can be used in the design of LNA circuits, as will be seen later, either by inserting a black box model representing the circuit model, discussed here, into the schematic circuit of the amplifier or by inserting a layout symbol containing the S-parameters data obtained from the Momentum simulation into the schematic circuit.

5-6-2 MIM capacitors

Capacitors may be included in MMIC circuits in any of four basic configurations: an open-circuit transmission line, coupled lines or inter-digital capacitors, Schottky diodes, and metal-insulator-metal (**MIM**) capacitors. Coupled lines and open-circuit transmission lines can be used to provide fairly low capacitance values. For these two capacitor

types, the capacitance is dependent on the electrical length of the transmission lines. Therefore, they are only useful for high frequency applications and the capacitance is highly frequency dependent. The advantage of these capacitors is that they are easy to fabricate since they require only a single metal layer. The most popular type of capacitors for MMICs has become the MIM capacitor mainly used for DC blocking, de-coupling, matching, and feedback purposes. MIM capacitors have attracted great attention because of their high capacitance density that supply small area, increasing circuit density, and further reduce the fabrication costs.

5-6-2-1 MIM capacitors description

A schematic of an MIM capacitor is shown in Figure 5.9. This thin-film capacitor is composed of two metal plates separated by a dielectric material. Typically, the dielectric material overlaps the first metal layer and the upper metal layer has a smaller area than the lower metal layer. This configuration helps to minimize fringing fields to ground and shorts between the upper and lower capacitor plates. Although the air bridge shown on Figure 5.9 is not required, it is often included to further minimize parasitic capacitance.

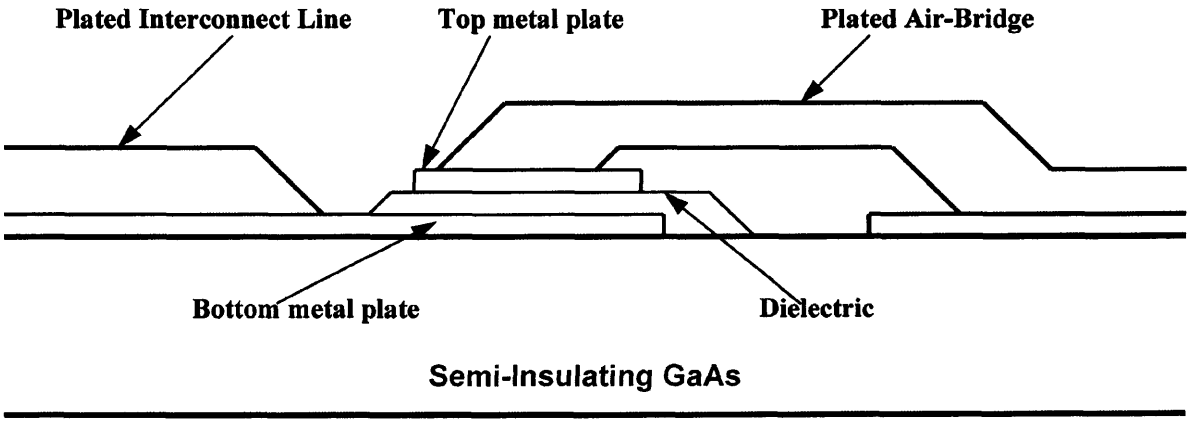


Figure 5.9 MIM capacitor using an air-bridge for top-level interconnect.

The dielectric is typically silicon nitride (Si_3N_4 0.1 to 0.4 μm thick) since it may be used in the MMIC fabrication process for circuit encapsulation or for passivating the exposed GaAs in the active devices, although silicon dioxide (SiO2) and polyimide are also used. In processes which use polyimide as the spacer dielectric for spiral inductors, the

polyimide can also be used to realize small value capacitors. Since the dielectric layer is substantially thinner than the substrate thickness, MIM capacitors exhibit significant fringing effects, which are a function of the perimeter. Careful experimentation to determine the magnitude of this effect for specific process parameters, such as dielectric type and thickness, is essential for any stable process **[142]**. The capacitance C is simply given by:

$$C = \varepsilon_0 \varepsilon_r W \frac{L}{d} \qquad (5.4)$$

Where ε_r, d are the relative permittivity and thickness of the dielectric material, while W, L are the width and length of the overlap area between the upper and lower metal plates of the capacitor.

Test capacitors should be included on the wafer for in-process verification. The yield of MIM capacitors on a wafer plays a major role in determining the total yield for the wafer. The major yield limiting factor for MIM capacitors is shorts caused by pinholes in the dielectric or sharp points on the metal plates. Pinholes are very difficult to eliminate completely, but they can be minimized by good cleaning and deposition processes. Again, trade-offs require an engineering judgment based on the experimental results and the realized yields for a particular process. In addition to pinholes, the circuit design must assure that the electric field across the capacitor does not exceed the dielectric breakdown field.

5-6-2-2 MIM capacitors modeling

It is important to accurately predict the performance of MIM capacitors in order to achieve a first-pass MMIC design success. Therefore, accurate and efficient capacitor modeling is necessary. Generally, there are two methods for modeling of MIM capacitors. The first approach is based on numerical methods **[202]**, the other on analytical methods. The numerical method is more accurate than the analytical approach, but it is complex and time-consuming but deeper physical interpretation of the model components can be obtained from analytical expressions.

There have been a number of publications on the approximate model of MIM capacitors in the last two decades **[203-207]**. However, detailed formulas on equivalent circuit models used in CAD programs are rarely disclosed. One of the most simple and

accurate MIM capacitor models, introduced in **[208]** will be used here with lumped elements values based on the physical parameters of the capacitor such as length (L), width (W), dielectric thickness (d), dielectric constant (ε_r), the thickness of top plate (t_t), the thickness of bottom plate (t_b) and loss tangent (tanδ).

The equivalent circuit model is shown in Figure 5.10. The main parameter of the model, C12, is given by the parallel-plate capacitance formula (equation.5.4)

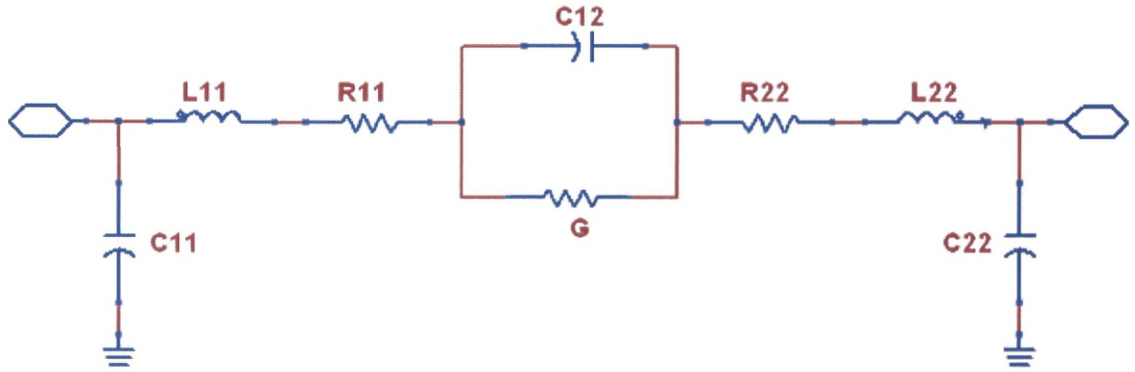


Figure 5.10 MIM capacitor equivalent circuit model.

The loss conductance, G, due to the capacitance dielectric can be obtained by;

$$G = w\, C_{12}\, \tan\delta \tag{5.5}$$

The metal plate losses resistance R_{11} and R_{22} can be obtained from the body resistance formula, if the metal thickness is smaller than the skin-depth,

$$R_{11} = \frac{\rho}{W}\frac{L}{t_t} \quad \text{(For the top plate resistance)} \tag{5.6}$$

$$R_{22} = \frac{\rho}{W}\frac{L}{t_b} \quad \text{(For the bottom plate resistance)} \tag{5.7}$$

The metal plate inductance can be worked out based on microstrip transmission line approach **[38]**.

$$L_{11} = L_{22} = \frac{0.4545\, Z_o L}{c} \tag{5.8}$$

C_{11} and C_{22} are capacitances with respect to ground of the top plate and bottom plate respectively.

$$C_{11} = C_{22} = \frac{0.5\, \varepsilon_{eff} L}{Z_o c} \tag{5.9}$$

5-6-2-3 MIM capacitors fabrication and measurements

During the fabrication of the MIM Capacitors, the base (bottom) plate metal of 1500 Å thick was deposited on the semi-insulating GaAs wafer using standard photolithography, metallization, and lift-off technique. A thin film (90 nm thick) of Si_3N_4 was then deposited to form the capacitor dielectric layer. The upper plate metal of thickness 1500 Å was formed on top of the Si_3N_4 dielectric layer. The metals used for top and bottom plates of the MIM capacitors were Ti and Au (1:2). To verify the validity of this process technique and the accuracy of the presented equivalent circuit model, seven different sizes MIM capacitors corresponding to capacitance values between 0.3–20 pF are designed using the form given in equation 5.4. Capacitances values and geometrical dimensions of the capacitors designed as well as the models elements values are given in table 5.4.

Capacitance C(pF)		0.3	1	2.5	5.5	10	15	20
Length L(μm)		4.7	15.6	39.2	86.2	156.8	235	313
Width W(μm)		100						
MIM Capacitor Model Elements	C (pF)	0.3	1	2.5	5.5	10	15	20
	G (mS)	0.028	0.1	0.236	0.518	0.094	1.4	2
	R_{11} (Ω)	0.016	0.055	0.137	0.302	0.549	0.823	1.1
	R_{22} (Ω)	0.016	0.055	0.137	0.302	0.549	0.823	1.1
	L_{11}, L_{22} (pH)	0.55	1.87	4.58	10	18.3	27.5	36.7
	C_{11}, C_{22} (fF)	0.83	2.76	6.9	15.2	27.6	41.4	55

Table 5-4 Designed capacitors dimensions and circuit model elements values.

The designed capacitors were fabricated on GaAs substrate on CPW form according to the process technique stated above and the S-parameters measurements were carried out between 0.45 GHz and 15 GHz using an HP8510C vector network analyzer and Cascade Microtech RF probe station. An Electromagnetic simulation for the designed capacitors has been carried out using the momentum simulator on the ADS and excellent agreement were obtained between the measured and modeled data as shown in Figure 5.11 for the 5.5 pF capacitor as an example.

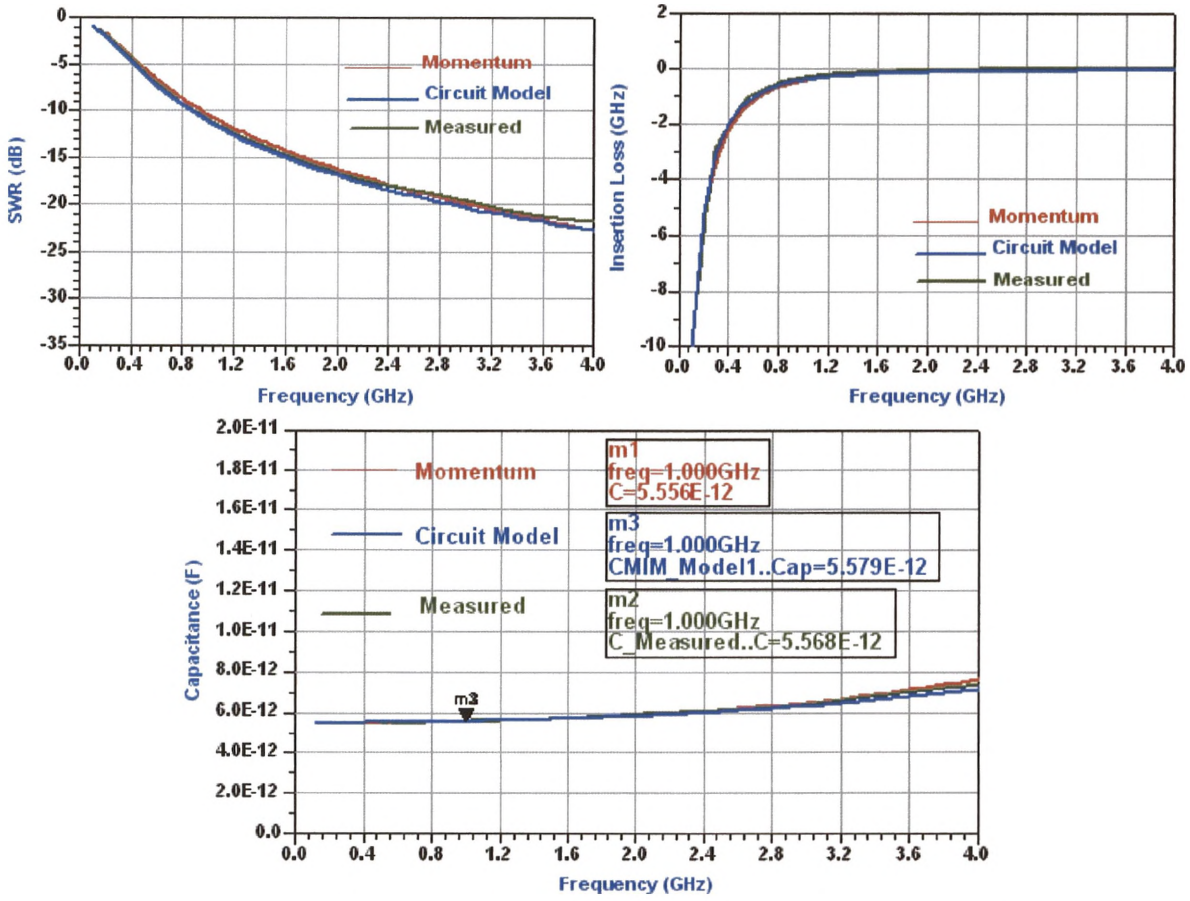


Figure 5.11 Comparison between the measured and modeled data for the fabricated 5.5 pF capacitor.

A capacitance density of 0.638 fF/μm^2 has been obtained for the fabricated capacitors. This density is not too high and so large areas will be expected especially for high capacitance values required for coupling in the IN/OUT of the MMIC LNA circuit worked out during this study. The capacitance density still can be increased up to 1 fF/μm^2 if the thickness of the dielectric material (Si_3N_4) decreased to 570 Å instead of the 900 Å used or by using a higher dielectric constant material.

5-6-3 Thin-film resistors

Resistors are used for feedback circuits, setting the bias point of active devices, isolation, and terminations in power combiners and couplers. Two types of resistors are used in MMIC fabrication: thin films of lossy metals and lightly doped GaAs active layers (mesa resistors). Figure 5.12 shows schematics of each of these two types of resistors.

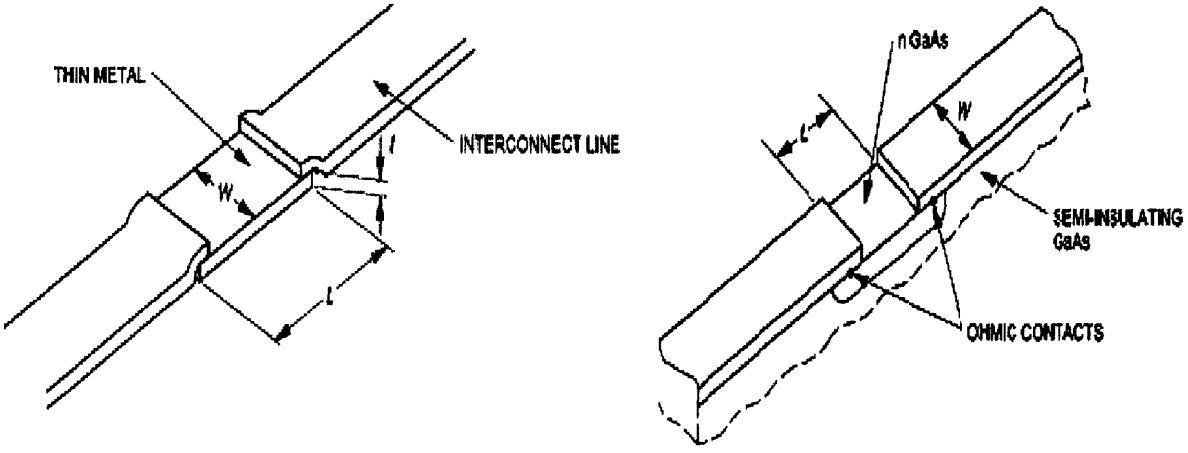


Figure 5.12 Two resistor types in MMIC fabrication: (a) Thin film resistor (b) GaAs-based resistor incorporating an n GaAs channel and ohmic contacts[142]

The resistance for both types of resistors may be given by ($R = \rho_s L/A$) where ρ_s is the sheet resistivity, $A = W*t$ is the cross-sectional area of the resistor, t is the resistor thickness, W is the width of the resistor, and L is the length.

The efficiency of the resistor as determined by the resistance per unit length is a function of ρ_s. For metal thin film resistors, ρ_s is a function of the metal. For GaAs based resistors, ρ_s is a function of the doping concentration.

But (ρ_s/t) normally gives the sheet resistance, R_{sh} ($\Omega/\square$), of the film and hence the resistance can be expressed as following, and this is the commonly used form.

$$R = R_{sh} \frac{L}{W} \tag{5.10}$$

5-6-3-1 NiCr resistors

Tantalum nitride (TaN) and nickel chromium (NiCr) are the most widely used in the fabrication of resistors for passive technologies. NiCr has the best temperature

coefficient of resistance (TCR) and voltage coefficient of resistance (VCR) and its overall process integration is easier than TaN **[209]**. However, Ni content controls the film resistivity as well as the NiCr reactivity when exposed to solutions at later processing steps, making complete passivation of the resistors necessary.

Sputtered metal thin-film resistors, which are of interest in this work, are used for accurate and low-resistance applications. They are usually fabricated from TaN and NiCr, although Cr, Ti, Ta, Ta_2N, and AuGeNi alloys have also been used. Some of the advantages of thin-film resistors are a low TCR, tight tolerances, small parasitics, and low sheet resistivity **[210]**. The major disadvantage of thin film resistors is the added processing steps required to fabricate them, although thermal dissipation difficulties and electro-migration failures are also a concern. Short resistors or those made from materials with a large resistivity have fewer parasitics, but they have a higher thermal load to dissipate. When resistors must dissipate large amounts of power, they can have the highest temperature on the MMIC and limit the MMIC reliability. Side-gating or the flow of current around the perimeter of the resistor is usually eliminated by depositing the resistor on top of an insulating film such as Si_3N_4. Electro-migration failures result from the large current densities that can flow through the thin metal films. Tantalum resistors have exhibited this problem for thin, 0.006 mm layers, with currents of 0.06 mA/mm of line width. Lastly, NiCr resistors are susceptible to degradation due to moisture. Therefore, these resistors must be passivated **[142]**.

5-6-3-2 NiCr resistors fabrication and measurements

Many different resistors sizes corresponding to resistance values (5 to 2000 Ω), were designed according to the form given in equation 5.10. Semi-insulating GaAs (100) substrates were used to optimize the parameters for repeatable sheet resistance in NiCr films. In order to address the issue of achieving repeatable values of sheet resistance, an alloy composition 80:20 Ni–Cr was deposited by DC magnetron sputtering on the GaAs substrates under varying conditions of DC power, voltage, substrate temperature and pressure of the process gas. Different thicknesses of the NiCr-alloy (50-400 nm) were sputtered under these varying conditions till reaching a machine setup and metal thickness most suitable for the required sheet resistance (≈100 Ω/□).

The sheet resistance R_{sh} and contact resistance R_C of the fabricated resistors were measured by transmission line model method (TLM) **[211]**. The DC resistance of a resistor of width W was measured for different lengths between two contact pads on the TLM test structures fabricated on the wafers. A plot of the measured DC resistance versus the resistive length (distance between two contact pads), Figure 5.13, was used to extract the values of R_{sh} and R_C according to the following relations:-

$$R_{sh} = \text{slope} \times W$$

$$2R_C = \text{intercept on y-axis}$$

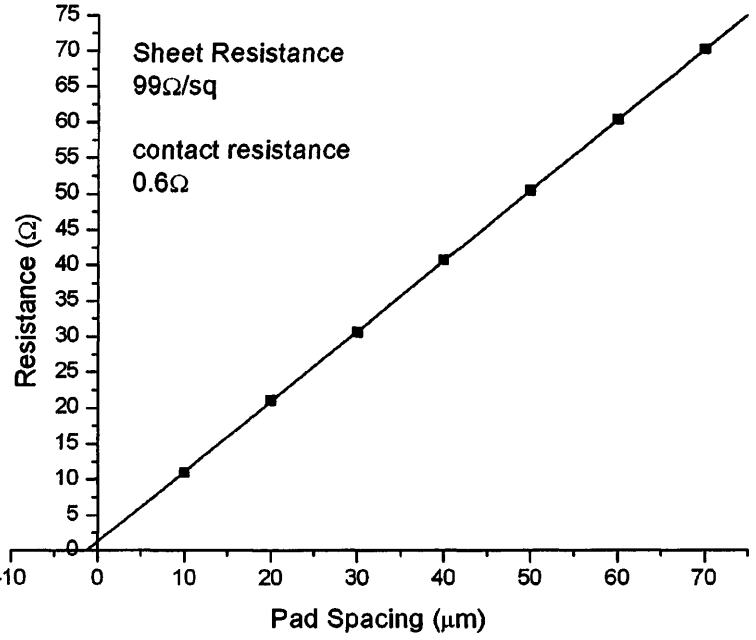


Figure 5.13 Typical TLM measurements for the fabricated 80 nm-thick NiCr resistors.

5-7 MMIC Design Methodology

The penetration of commercial radio frequency systems into the microwave and millimeter-wave bands has put increased pressure on reducing MMIC costs at all stages of production and design. In the field of circuit design, the use of CAD simulation and layout tools plays a pivotal role in first-time success and yield of a MMIC design.

Designing a MMIC involves two critical stages: performance specification, and circuit design and simulation. Other functions such as fabrication and test must also be

considered during the design stages to arrive at a manufacturable product with high yield and the desired performance.

A typical MMIC design flow chart is illustrated in Figure 5.14 **[212]** in which the designers usually begin by deriving an initial schematic topology from the design specifications. Next, they begin to perform a linear, non-linear and mixed-mode circuit analysis, tweaking circuit parameters in search of desired specifications. Not until circuit performance is optimized and yield studied that layout and other physical design related issues are given serious thought, but only after circuit performance is met in the schematic domain that layout generation and verification begin. The physical design and verification step is where most MMIC design flow bottlenecks occur. Namely, design layout generation from a schematic representation can be a challenge encompassing maximizing chip real estate while maintaining design specs, checking layout against process rules, extracting physical parasitics and back annotating them to schematic as well as final interconnects and package design. All these physical design activities play a critical role in design performance. For example, layout generation/ placement may cause cross coupling between nearby traces. Fixing Design Rule Checker (DRC) rule violations may degrade electrical performance of the design. Distributed elements often perform differently under real-world conditions. Packaging effects further impact the robustness of MMIC designs and rarely are considered at the schematic level. Intrinsic, physical design attributes often cause the MMIC design to fail specifications and the designer must go back and fourth between schematic and layout in search of possible fixes. MMIC designers cannot afford to generate the final mask before attaining a certain level of confidence in the design because failing a fabrication run can be prohibitively expensive and time consuming.

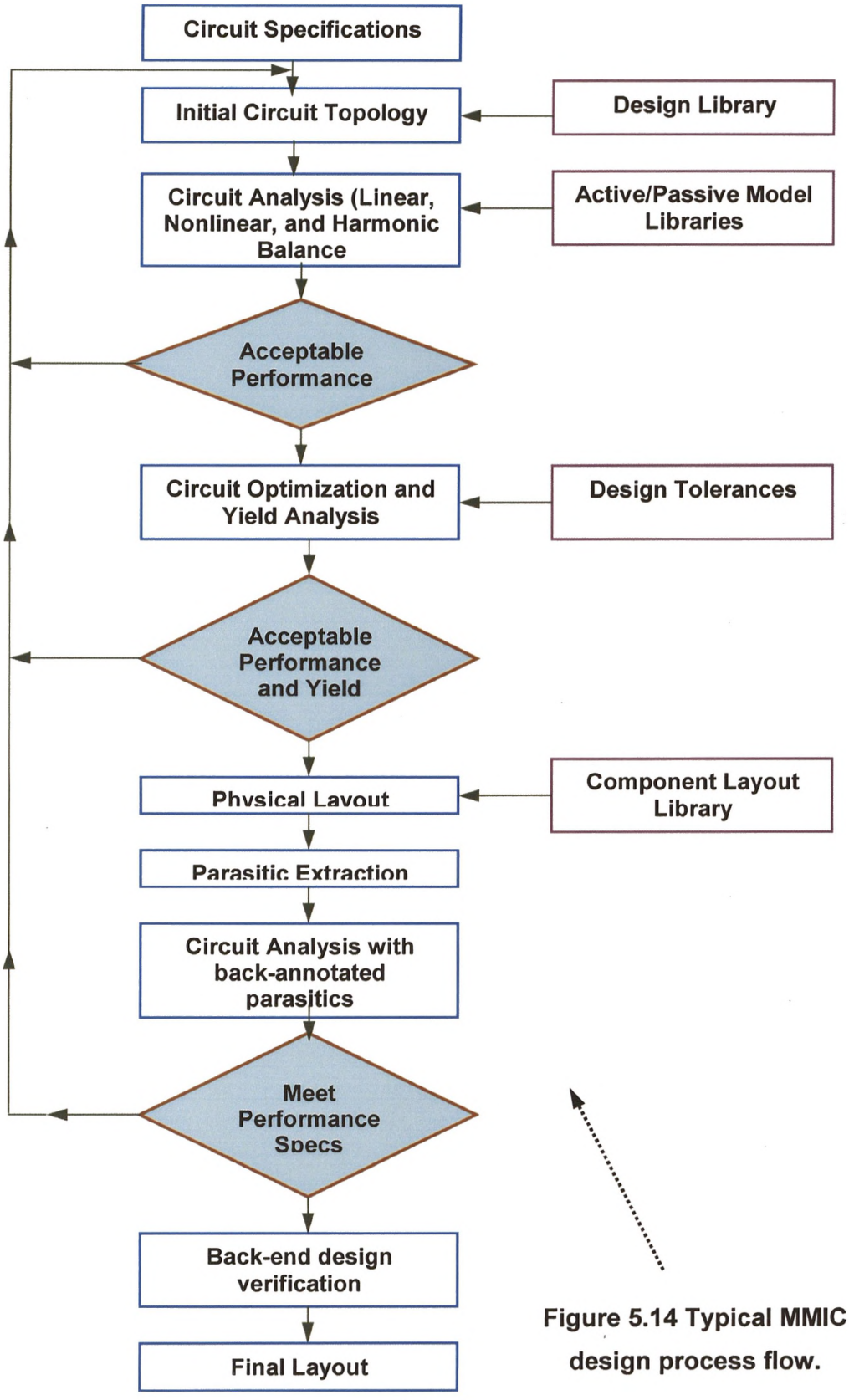


Figure 5.14 Typical MMIC design process flow.

5-8 Conclusions

In this chapter, the MMICs have been reviewed in terms of their history, design methodologies, different technologies, main applications, advantages and disadvantages compared with the conventional MICs.

In addition, a complete library of MMIC passive components in the CPW form has been developed to be used later in the design and realization of MMIC LNA circuits for SKA applications. Accurate schematic equivalent circuit models have been extracted for the designed and fabricated passive elements based on their physical structures. Also, extensive electromagnetic simulations have been performed for these elements using the Momentum simulator on the ADS. Complete agreement has been obtained between the modeled and the measured data of the fabricated spiral inductors, MIM capacitors, and NiCr thin film resistors.

- For the fabricated (2.5 nH-21.7 nH) inductors, low series resistances (8-35 Ω) and high quality factors (3.7-5.7) have been obtained. Also, the SRFs of the fabricated inductors are high enough for safe operation in the low SKA frequency band.
- Accurate MIM capacitors have been fabricated and measured with capacitance density of 0.623 $fF/\mu m^2$ which can be increased by using thinner dielectric layers.

CHAPTER-6

Design and Simulation of Broadband MMIC LNA for SKA Radio Telescope

6-1 Introduction

State-of-the-art communications and radio astronomy applications demand high-density, small size, and reliable multifunction monolithic microwave integrated circuits (MMICs). As stated previously, MMICs use microstrip or coplanar waveguide as the planar connections between semiconductor devices. These open waveguides contain a significant portion of electromagnetic energy above the circuit substrate. Furthermore, as advanced circuits are made more complex and more compact, inter-element coupling begins to affect overall circuit performance. For example, if a transmission line is placed too close to a rectangular spiral inductor that is used in a filter, the parasitic coupling between the two elements could change the value of the inductor and detune the filter. Although MMIC density is still low relative to that of most advanced digital integrated circuits, MMIC designers are faced with competing objectives. A circuit design must simultaneously accommodate the area required by the largest structures in an MMIC (typically inductors or inductive lines), maintain a "reasonable" distance from nearby transmission lines and other elements, and minimize the use of chip real estate **[213]**. On the other hand, low noise, low power consumption, high linearity and small chip size are the key requirements during the design and realization of MMIC LNAs.

The performance of low-frequency microwave MMIC low-noise amplifiers is usually limited by the noise performance of the active devices (typically a GaAs MESFET or HEMT) and the losses of the input and output matching circuits. These factors make the simultaneous realization of an ultra low-noise figure, high input and output return loss, and high gain difficult. In addition, at the lower microwave frequencies (< 8 GHz), the use of distributed matching elements is prohibited in monolithic circuits because of the large size they would require. The lumped element matching approach can lead to additional losses that can further compromise performance.

In this chapter, two different generations of the MMIC LNA circuits required for the low frequency band of the SKA radio telescope were designed and realized in CPW form as a part of the European SKA design study (SKADS). The first generation was based on the old process samples of the thin gate metallization, which had relatively high parasitic elements, and modest noise performances. The second one was based on the new process devices with the enhanced RF and noise characteristics due to the much thicker gate metallization and the multi-gate finger technique employed. For the sake of completeness, however, a commercial 0.2 μm HJ-FET device was also used in the designed of the same circuit to check the advantages or disadvantages of using sub-micron devices in the low frequency bands of the SKA.

6-2 Circuit Specifications

For the up-coming SKA radio telescope front-end receivers, it is required to design HJ-FET MMIC broadband LNAs covering the frequency range 0.3 – 2 GHz, and to realize these circuits in the CPW form, mainly for cost reduction purposes. The desired specifications of the circuit are given in Table 6.1. SOI and TOI are the second and third order intercepts respectively while PAE is the power added efficiency of the amplifier circuit. It is also required to use reasonable values of passive elements (spiral inductors, MIM capacitors, and thin film resistors) so that the total circuit area does not exceed 2 mm^2 for a single-stage circuit and 3 mm^2 for double-stage designs.

Parameter	*Target Goal*	*Accepted Tolerance*
Gain (dB)	15	±20 %
Noise figure (dB)	< 0.5 (36 K)	±10 %
Input SWR (dB)	-10	±15 %
Output SWR (dB)	-10	±15 %
1-dB Compression (dBm)	> 5	-
TOI (dBm)	>15	-
PAE (%)	50	±5

Table 6.1 LNA circuit desired Specifications.

6-3 LNA Design Using Commercial Sub-micron HJ-FET

It has been traditional in radio astronomy applications to use the latest, highest f_T devices available in the design and realization of very low noise amplifiers. However, despite their superior noise performances (extremely low N_{Fmin}), there are many difficulties in using sub-micron HJ-FETs for low noise amplification purposes at very low microwave frequencies (< 4 GHz), as discussed in chapter-3. A clear evidence for this will be given by using such one device in the design of the MMIC LNA circuit required for the SKA project.

The device used here is an NEC (0.2 x160 μm) HJ-FET, NE-3210S01 **[214]**. The DC and RF characteristics of this device will be discussed in the next sub-section. Note that this device has a gate width of 160 μm which was the largest periphery provided by this vendor. This, of course, is a typical value for devices optimised for high frequency operation.

6-3-1 Device DC and RF characteristics

The DC characteristics of the used device are shown in Figure 6.1 from which it can be noticed that the device exhibits a threshold voltage of –0.75 V with an absolute maximum transconductance of 500 mS/mm obtained at V_{DS} = 1V and V_{GS} = -0.25 V (I_D = 23.7 mA), which will be the main DC bias point of interest during this design process.

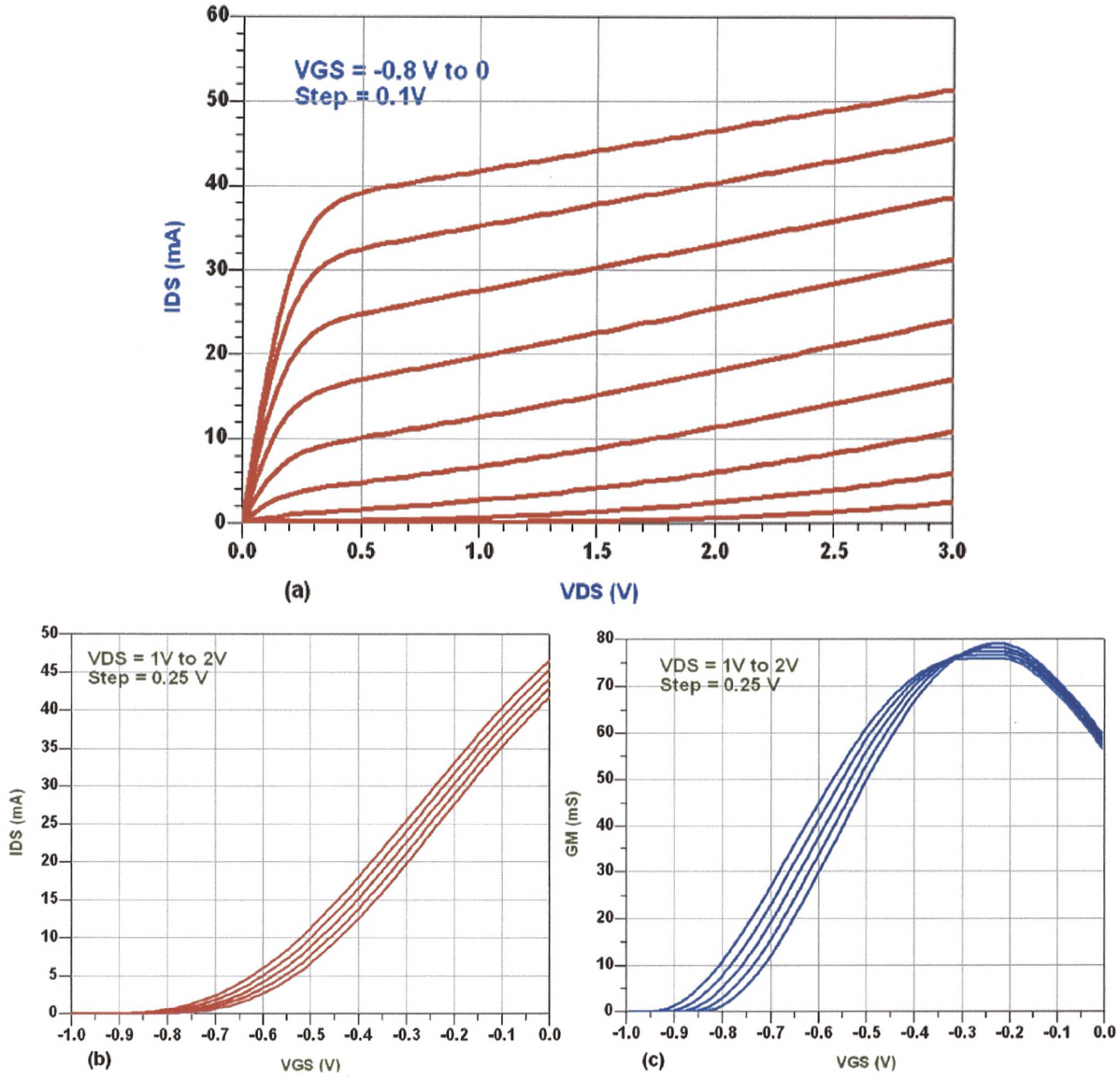


Figure 6.1 DC characteristics of the 0.2 µm commercial HJ-FET used for LNA design (a) IV-Curves (b) ID-VGS Curves (c) Transconductance.

The RF characteristics of the used commercial sub-micron device are shown in Figure 6.2. Examining these characteristics it can be easily noticed that this device is well suited for X-band (8-12 GHz) low noise applications providing the lowest noise resistance and noise figure together with the best in-out SWR over this frequency band. For the low SKA frequency band of interest (0.3 – 2 GHz), the device exhibits much worse noise performance with the worst possible input SWR (~0 dB) and so, a great

deal of difficulties were encountered during the design of the required LNA circuit using this device in such a low frequency band.

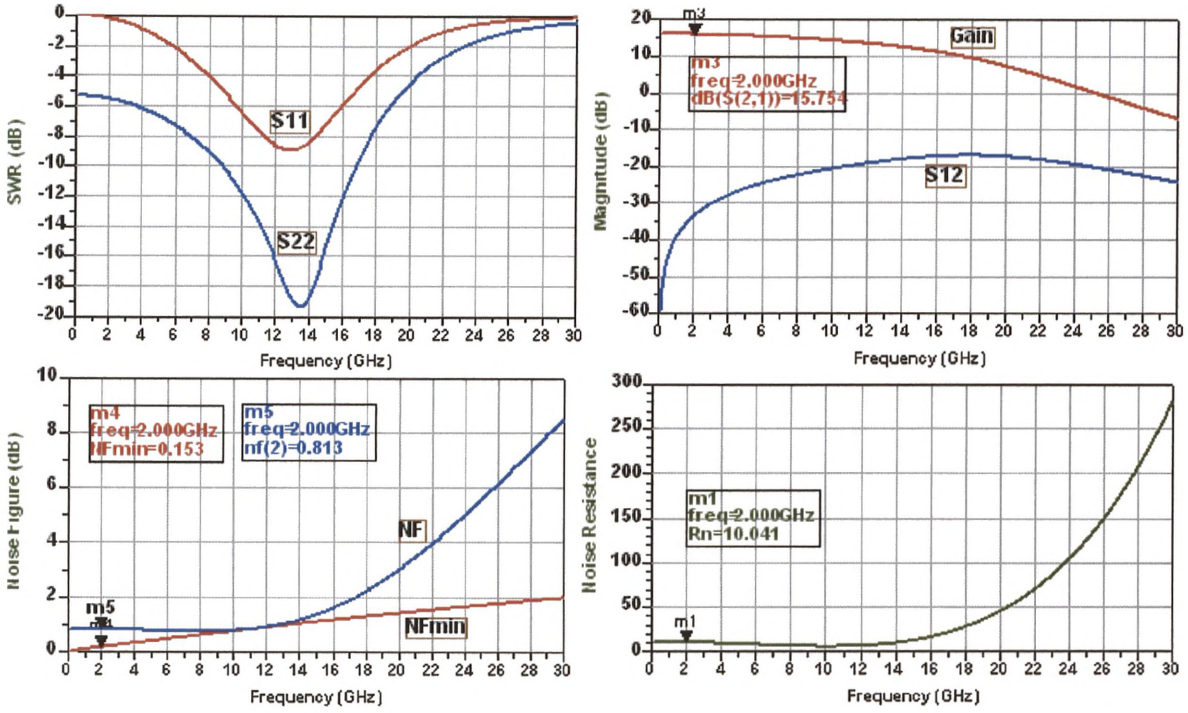


Figure 6.2 RF characteristics of the 0.2 µm commercial HJ-FET used for LNA design.

6-3-2 Circuit design and simulation

The TOM nonlinear large-signal model of the sub-micron device used provided by NEC company has been used for the circuit design using the Agilent's ADS software package **[215]**. The designed LNA circuit using this device is shown in Figure 6.3. The DC bias condition chosen for the transistor was V_{DS} = 1 V with I_D = 23.7 mA (V_{GS} = -0.25 V). In this circuit:-

- Resistors RD, Rbias, capacitor Cbias, and Inductor LD are dedicated for applying the required DC bias for the drain while the corresponding inductor at the gate side has been replaced by a large resistor RG (8 kΩ) to avoid the effect of the series resistance of the large inductor on the noise performance of the circuit **[216]**.
- Inductor LS is used for enhancing the circuit stability and input SWR and inductor LG is used for input matching while capacitors Cin and Cout are the in/out coupling capacitors.

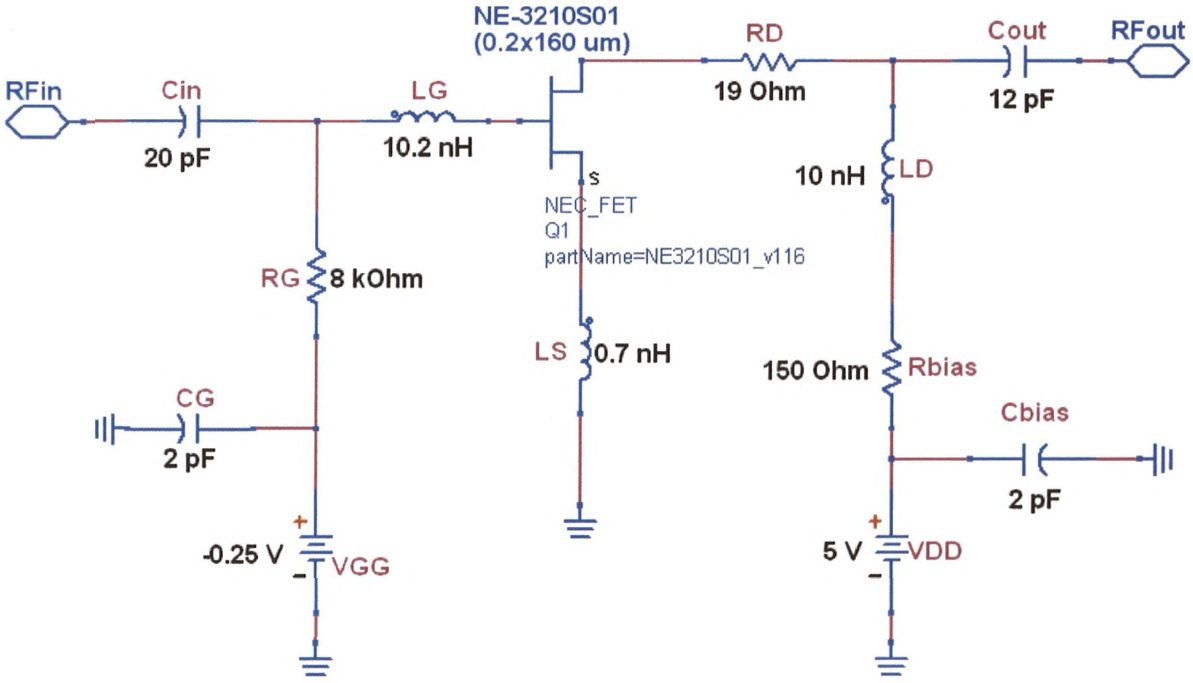


Figure 6.3 Schematic circuit diagram of the designed LNA, using 160 µm commercial sub-micron (0.2 µm) HJ-FET.

The S-parameters and noise simulation results of the LNA circuit designed using the commercial sub-micron device are shown in Figure 6.4 from which it can be seen the poor noise characteristics obtained for this circuit with an average noise figure of 0.8 dB (64 K) and a very poor in/out SWR over the frequency band of interest. Note that in this circuit the input inductor LG (10.2 nH) was assumed to be ideal, i.e. with a zero series resistance. A realistic inductor series resistance of ~ 16 to 18 Ohm, typical for the value of inductor used, would have worsened the noise figure even further.

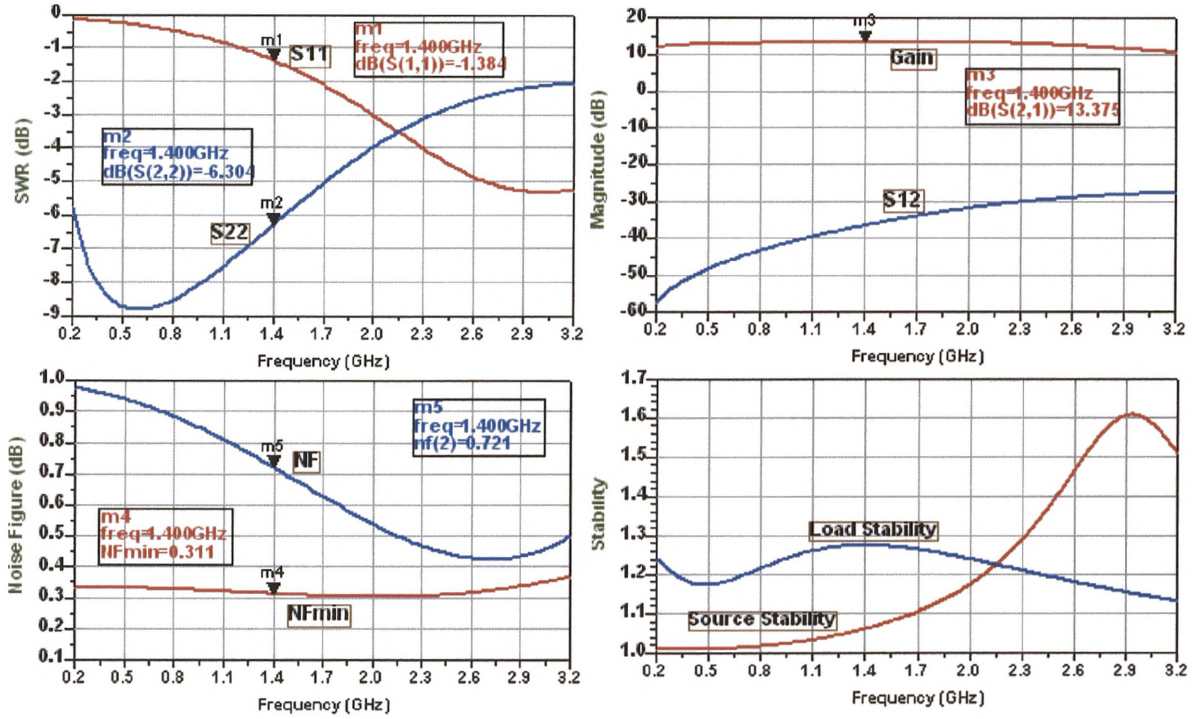


Figure 6.4 S-Parameters and noise simulation results of the designed LNA circuit, using 160 µm commercial sub-micron (0.2 µm) HJ-FET.

6-4 LNA Design Using Old Process Devices

For the desired LNA design objective, sample VMBE-1841 was chosen from the old process fabricated samples for its high transconductance, low leakage, small threshold voltage, and high cut-off frequency. The gate length of the device was 1 µm.

6-4-1 Device description and modeling

The linear small-signal and nonlinear large-signal models extraction techniques, introduced in chapter-4, were applied to a 2x100 µm from the chosen sample and excellent agreements were obtained between the measured and modeled data as shown in Figure 6.5 for the DC and Figure 6.6 for the RF characteristics. The device's room temperature minimum noise figure predicted from the small-signal model using Fukui's analysis is compared with that obtained from a nonlinear large-signal model as shown in Figure 6.7, giving a noise figure around 1.1dB at 2GHz for V_{DS} =1.5 V, I_{DS}= 20 mA = 35 % of I_{DSS}. However, a better noise performance may be obtained at a different

bias point and that could be investigated by plotting the noise parameters over a wide range of DC bias as will be shown in the next sub-section.

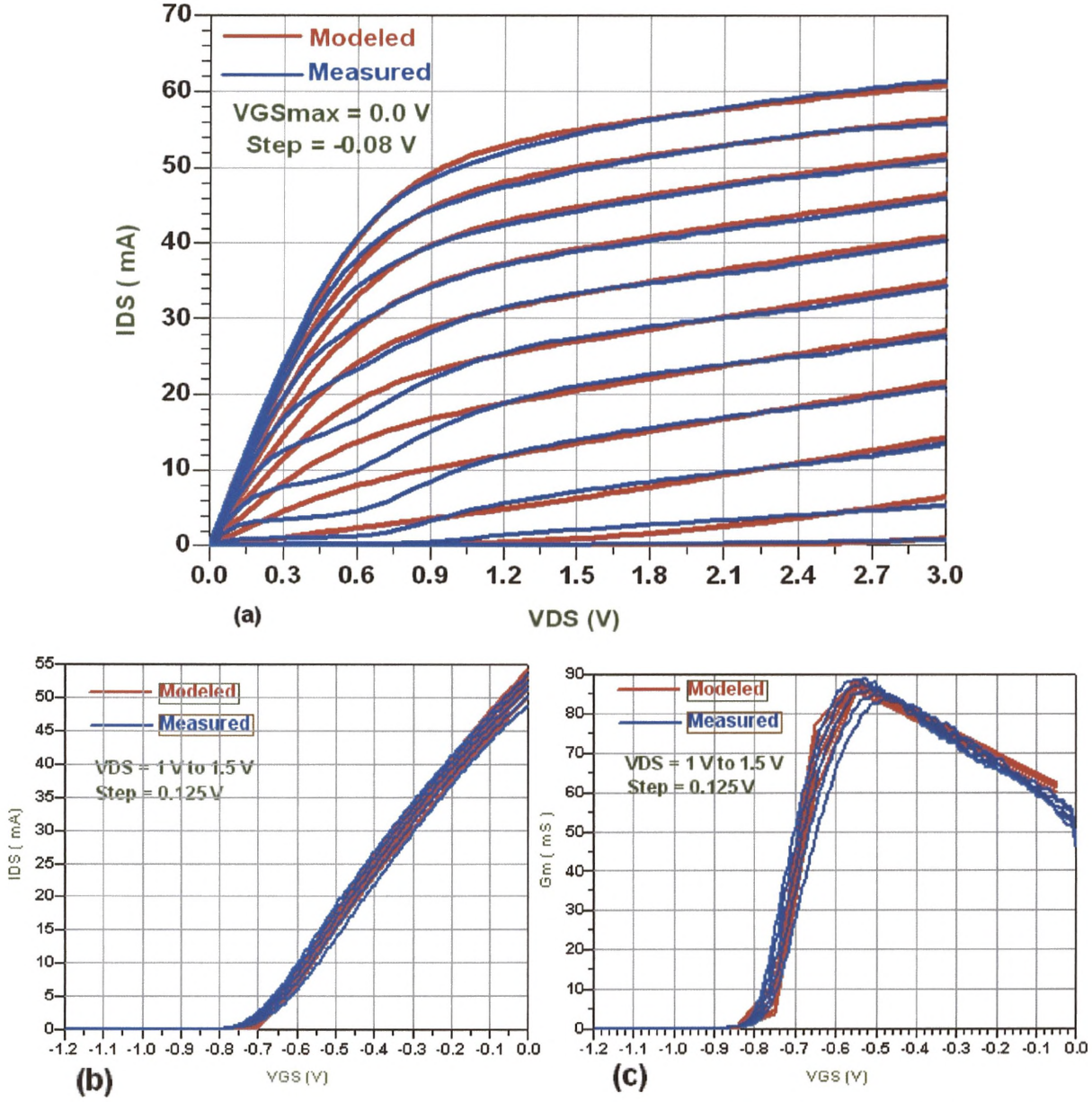


Figure 6.5 Comparison between measured and modeled DC characteristics of the 2x100 µm device used (a) IV-Curves (b) ID-VGS Curves (c) Transconductance.

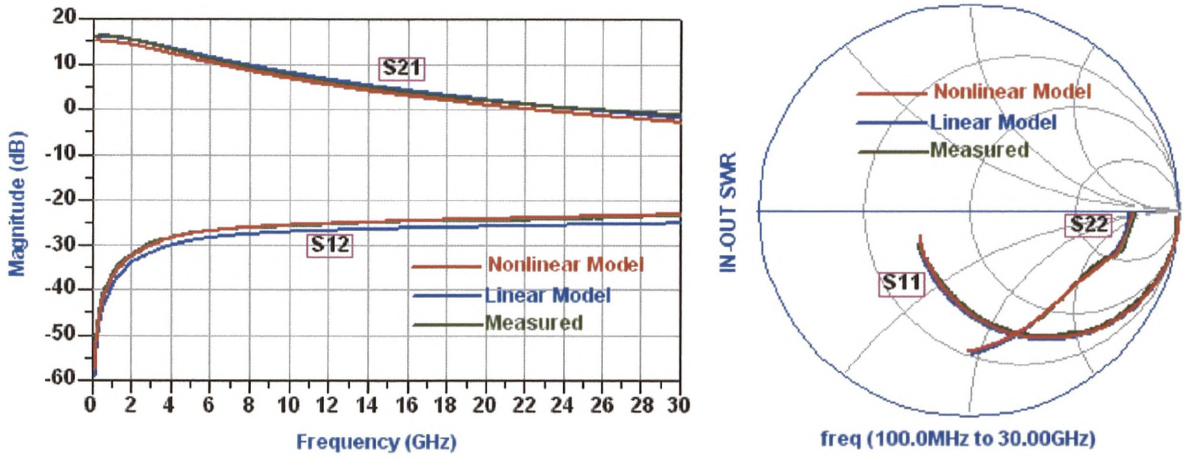


Figure 6.6 Comparison between measured and modeled RF characteristics of the 2x100 µm device used.

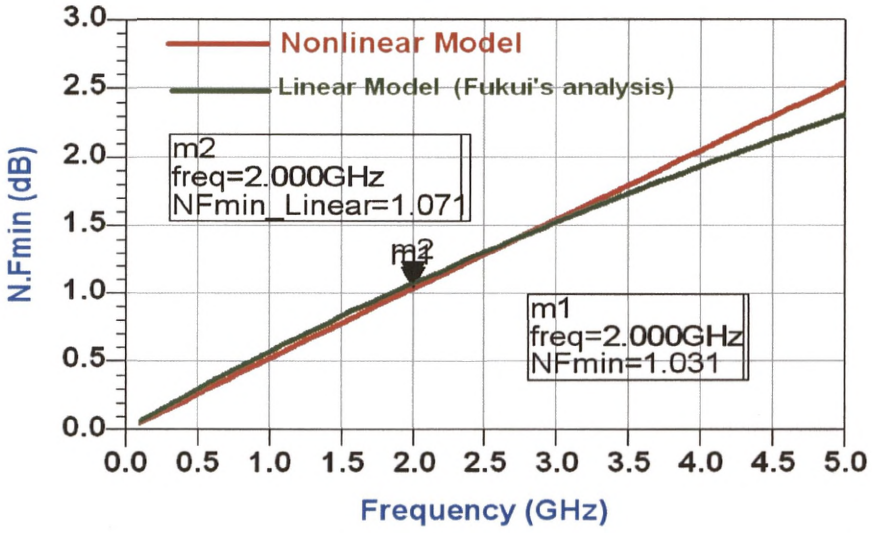


Figure 6.7 Predicted room temperature minimum noise figure of the used transistor (sample VMBE-1841).

6-4-2 Choice of the DC bias point

It is always recommended to operate the FET as an amplifier in the saturation region of its output characteristics **[217]**. It is also well known that the transistor starts to saturate at V_{DS} value very close to the threshold voltage. The device used here, sample VMBE-1841, exhibits a threshold voltage of -0.78 V and so a drain voltage of 1 V will guarantee deep saturation region operation.

Figure 6.8 illustrates the gain and noise parameters of the used device versus drain current at V_{DS} = 1V and at a frequency of 2 GHz. From these plots, the optimum bias point for the best noise and gain performance to be V_{GS} = -0.63 V and I_D = 5 mA = 10 % of I_{DSS}, can easily be determined. At this bias point, NFmin = 0.858 dB, R_n = 26.6 Ω, NF = 1.97 dB and Gain = 16.73 dB.

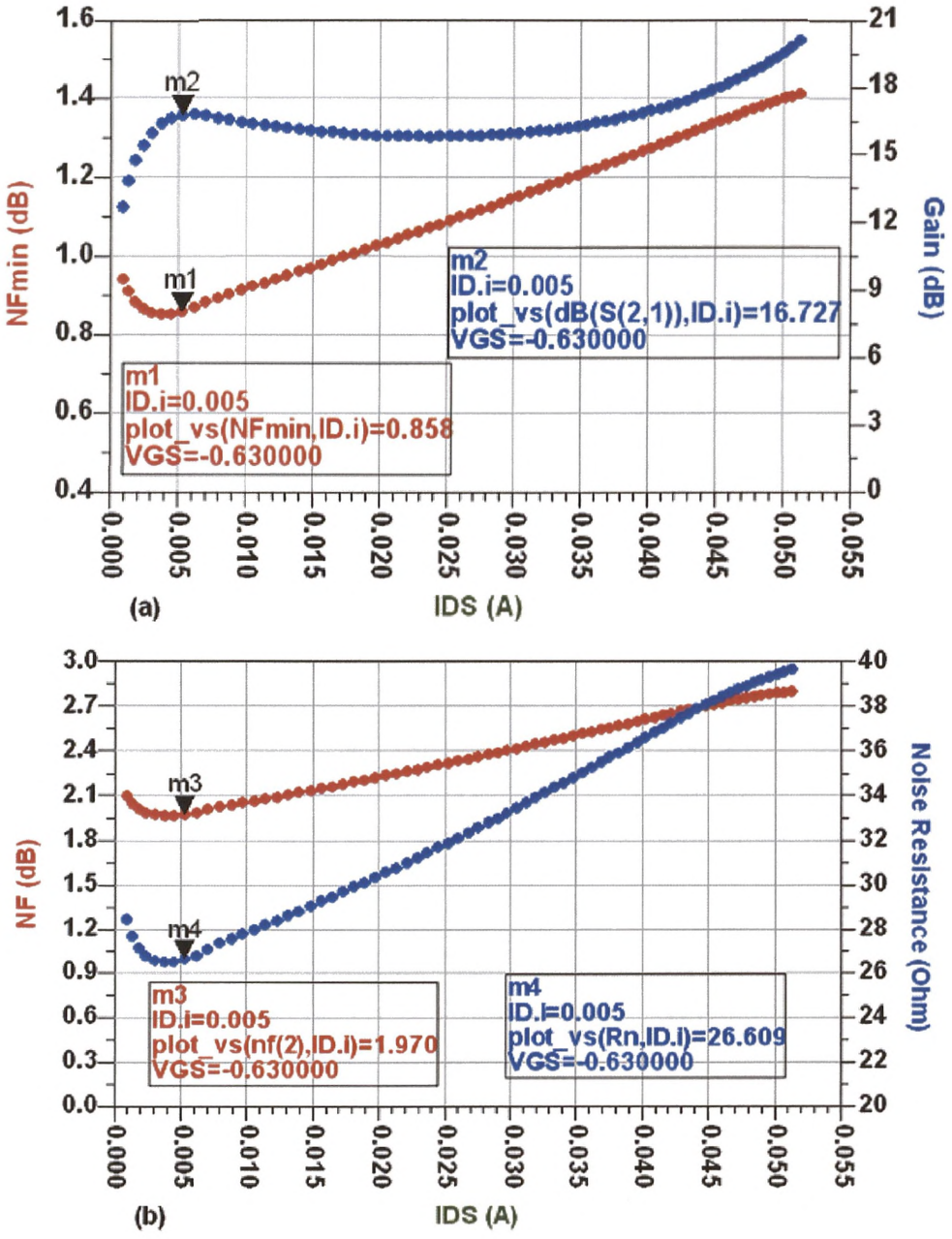


Figure 6.8 Investigation of the optimum DC bias point for the 2x100 µm device used at V_{DS} = 1 V and f = 2 GHz. (a) N_{Fmin} and Gain (b) NF and Rn.

6-4-3 LNA circuit design

Although negative feedback techniques for designing wide-band LNAs can be used to flatten the gain response, improve the input and output match/SWR, and improve the device's stability, this is always at the expense of gain level and noise performance, as discussed in chapter-3.

In the case discussed here, the only way that could be found to keep the circuit stable with adequate IN/OUT SWR at such low frequency band was the use of negative feedback.

Aided by the ADS software package and the EE-HEMT nonlinear large-signal models extracted, an initial design of the amplifier circuit was obtained, and then the necessary DC, S-parameters and noise simulations were performed. Finally, the optimization techniques, available in ADS are applied for the designed circuit in attempts to fulfill the specified goals as much as possible. The final circuit schematic with components' values is given in Figure 6.9. In this circuit:-

- Resistor RG, Inductor LD, and Capacitor Cbias are dedicated for applying the required DC bias conditions for the transistor.
- Feedback branch (Rfb, Lfb, and Cfb) is used for stabilizing the transistor over its entire band of operation (0-35GHz) to prevent oscillations at any frequency.
- The T-section (Li, Ci1, and Ci2) is the input matching network that transfers the input impedance of the circuit into 50 Ω.
- The T-section (Lo, Co1, and Co2) is the output matching network that transfers the output impedance of the circuit into 50 Ω.

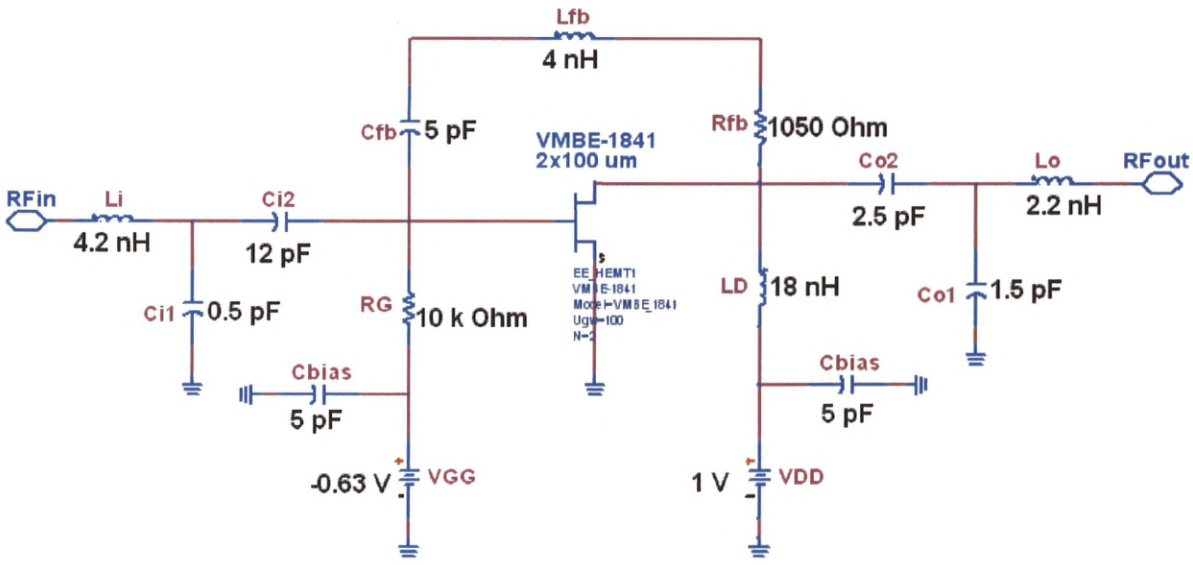


Figure 6.9 Schematic circuit diagram of the designed feedback LNA using 2 x100 µm, sample VMBE-1841 (old process).

6-4-3-1 Gain and noise simulations

The S-parameters and noise simulation results of the designed feedback LNA circuit are shown in Figure 6.10, from which it can be seen that the designed circuit does not satisfy all of the desired goals, providing an average gain of 16 dB, nearly flat over the frequency band of interest. An average, room temperature, noise figure of 1.35 dB corresponding to an equivalent noise temperature of 107 K, is obtained over the same frequency band with adequate input/output SWR.

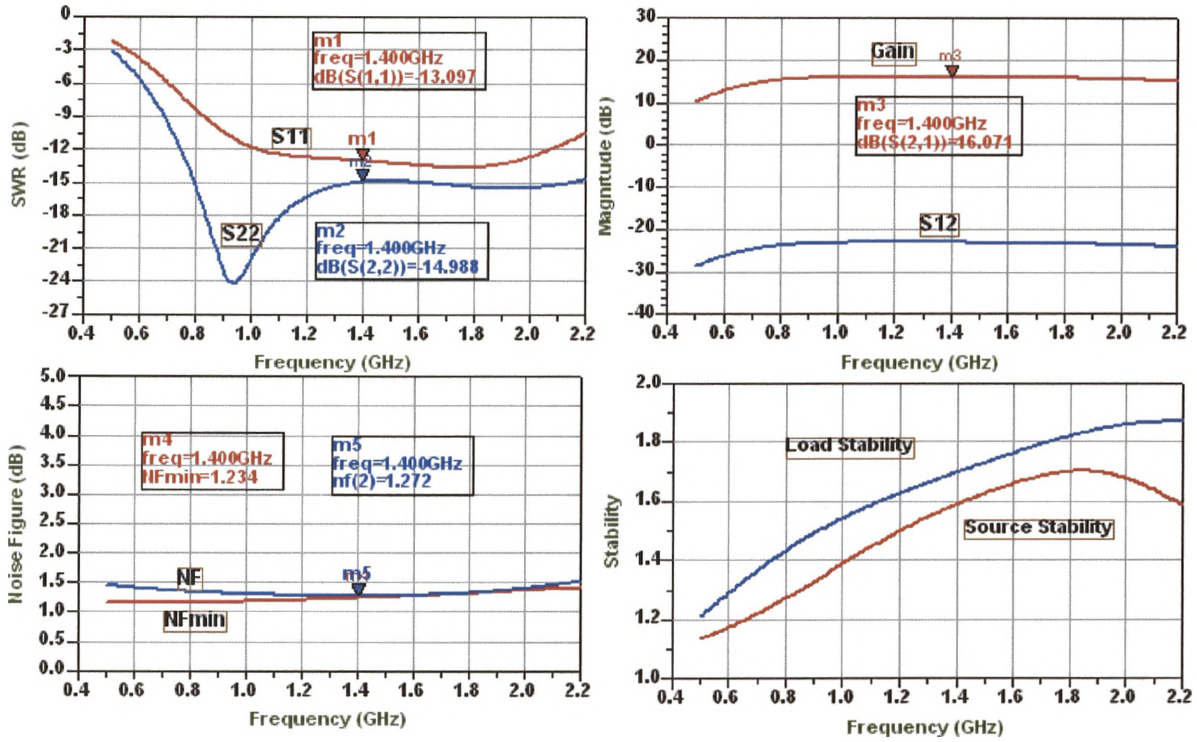


Figure 6.10 S-Parameters and noise simulation results of the designed LNA circuit, using 2x100 µm device VMBE-1841 (old process).

6-4-3-2 LNA linearity simulation

The 1 dB compression point, discussed in chapter-3, could be calculated using one of two different techniques as shown in Figure 6.11.

(1) Firstly by plotting both the ideal (linear) and real output powers versus the input power and searching for the point at which the difference between them is 1 dB, Figure 6.11a.

(2) The second technique is plotting the amplifier gain versus the input power and looking for the point at which the gain decreases by 1 dB from the constant (flat) gain, Figure 6.11b.

Very similar results were obtained from the different techniques providing a 1-dB compression point of -2.5 dBm (of the output power).

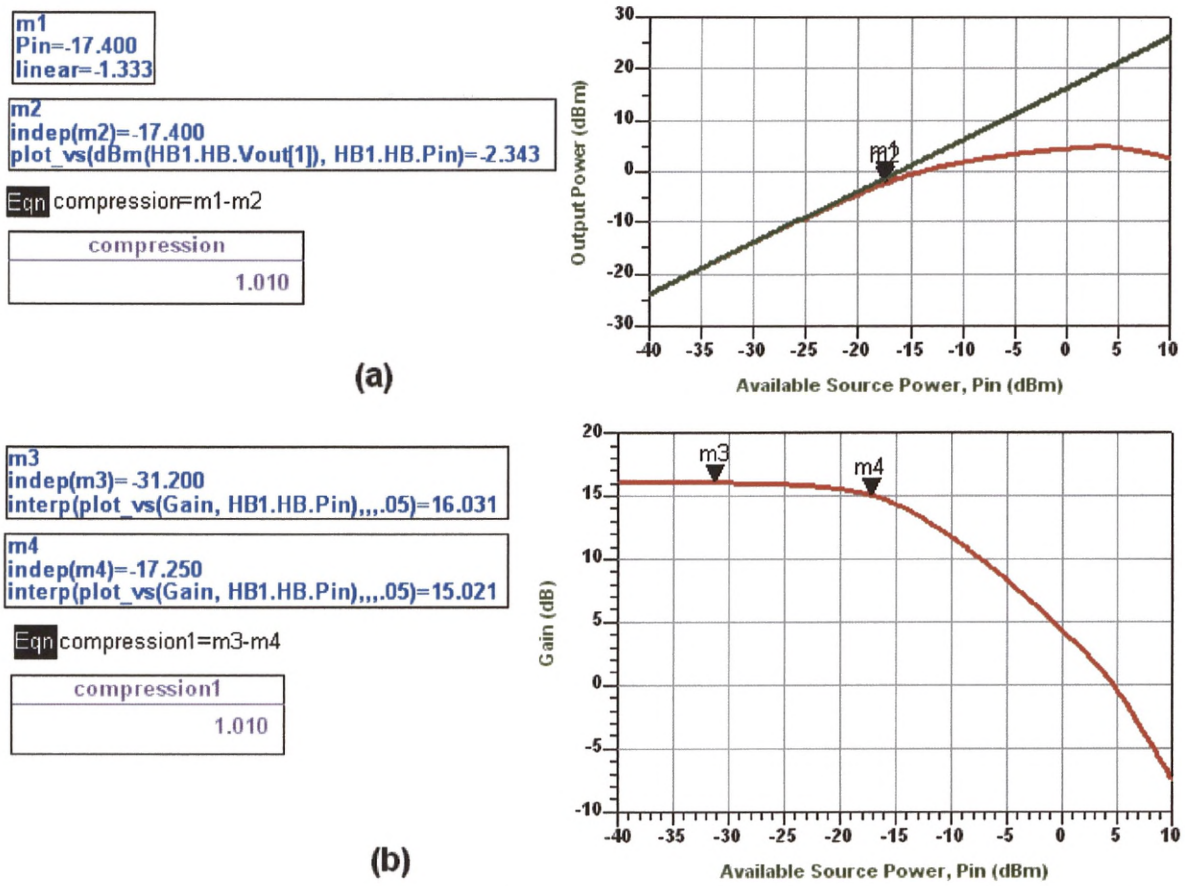


Figure 6-11 Linearity Simulations of the designed LNA circuit using 2x100 µm device VMBE-1841 (old process) at f = 1.4 GHz.

The second order intercept (SOI) and third order intercept (TOI) simulations of the designed feedback LNA are shown in Figure 6.12. The circuit exhibits a SOI over 25 dBm and TOI over 6 dBm and both of them are safely far from the 1-dB compression point.

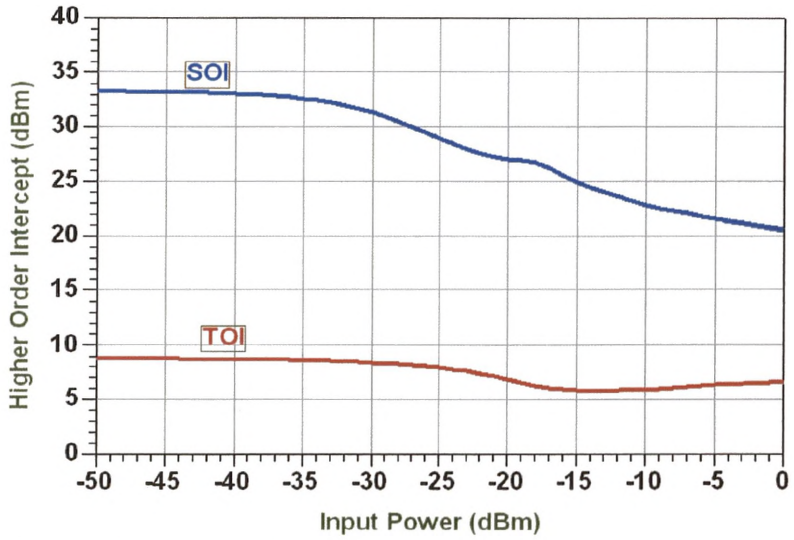


Figure 6-12 Second and third order intercepts of the designed LNA circuit using 2x100 µm device VMBE-1841 (old process) at f = 1.4 GHz.

6-4-3-3 Efficiency calculations

Different efficiency terms , discussed previously in Chapter-3 , were calculated for the designed first generation LNA circuit and the results are shown in Figure 6.13 providing a maximum PAE of less than 40 % over the entire frequency band of interest (because of the fairly flat gain).

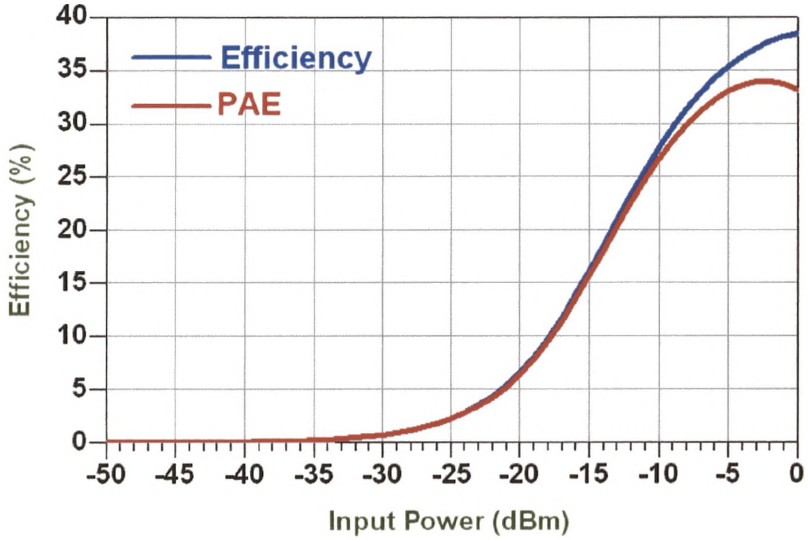


Figure 6-13 Efficiency calculations of the designed LNA circuit using 2x100 µm device VMBE-1841 (old process) at f = 1.4 GHz.

6-4-4 Effect of spiral inductors' series resistance

The designed LNA circuit contains four different rectangular spiral inductors, the effect of each on the circuit performance can be singled out as follows:-

- Inductor (LD = 18 nH) has an approximate series resistance of 30 Ω and the only effect of this resistance is to slightly shift the DC bias point. In this case, the same performance of the circuit can be kept if the applied DC drain voltage is increased from 1 V to 1.15 V to maintain the same DC current.
- Inductor (Lfb = 4 nH) with a series resistance of about 12 Ω, does not have any effect on the circuit performance because the feedback branch already contains a very large resistor (Rfb = 1050 Ω) in series with the spiral inductor.
- Inductor (Lo = 2.2 nH) with series resistance of approximately 7 Ω, also does not affect the noise behavior of the circuit because this resistance receives the amplified signal and thermal noise of the resistor and does not exhibit any amplification.
- Inductor (Li = 4.2 nH), which is the real problem of this circuit because the thermal noise of the 12 Ω-resistance, associated with this inductor, gets added to the input useful signal decreasing the input signal to noise ratio and hence increasing the noise figure of the circuit by (0.3-0.4 dB).

In fact, all inductors that may be inserted at the gate side will have a great effect on the noise performance of the circuit and so in the next LNAs circuits' designs, inserting inductors at the gate side will be avoided as much as possible and if necessary, they will be kept out of the MMIC chip.

6-5 LNA Design Using New Process Devices

Although the DC and RF characteristics of sample VMBE-1841 have been slightly changed in the new process compared with the old process such as a higher threshold voltage, lower transconductance and a slightly higher leakage current, it is still the best sample in the new process and it is the optimum choice for the LNA design process.

6-5-1 LNA design using 400 μm devices

The LNA design process employing sample VMBE-1841 fabricated in the new process will start with a 2x200 μm device whose DC and RF characteristics are described in the next sub-section.

6-5-1-1 Device DC and RF characteristics

Figure 6.14 shows a comparison between the measured and modeled DC characteristics obtained from the EE-HEMT large-signal model of the chosen 2x200 μm device. Complete agreement is obtained between the modeled and measured data with a threshold voltage of –1.1 V, and maximum transconductance of 110 mS obtained at a gate voltage very close to the pinch-off (-1 V).

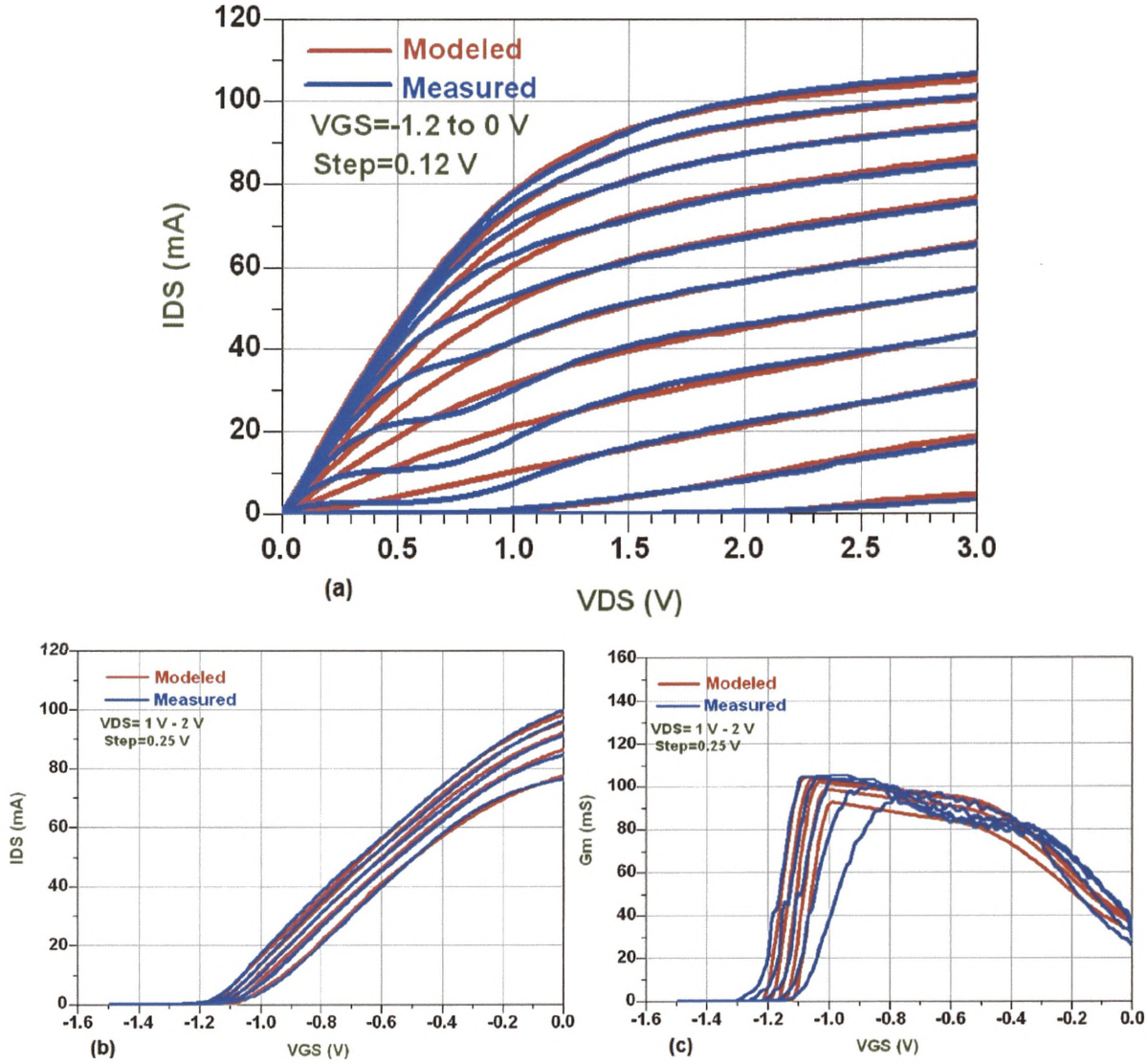


Figure 6.14 Comparison between measured and modeled DC characteristics of the 2x200 µm device used (a) IV-Curves (b) I_D-V_{GS} Curves (c) Transconductance.

Figure 6.15 illustrates a comparison between the measured and modeled RF characteristics obtained from the small-signal and large-signal models of the same device and again very good agreement between all of them is obtained.

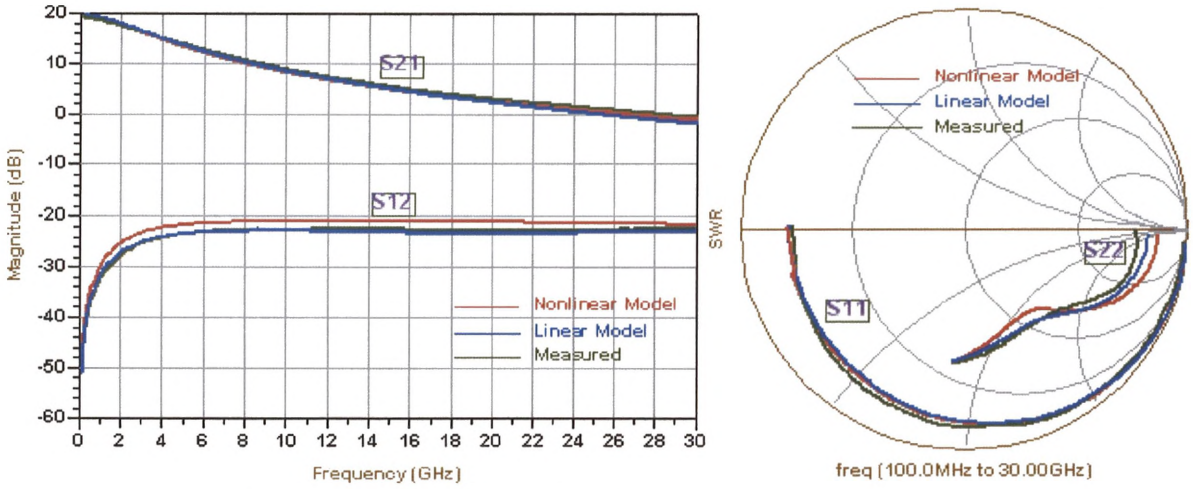


Figure 6.15 Comparison between measured and modeled RF characteristics of the 2x200 µm device used.

6-5-1-2 Choice of the DC bias point

For the purpose of investigating the optimum DC bias point for the best noise performance of the used 2x200 µm device used, the gain and noise parameters are plotted versus I_D/I_{DSS} ratio at different drain voltages (1 V and 1.5 V), as shown in figure 6.16. The desired bias point at V_{DS}= 1.5 V, V_{GS} = -1 V, and I_{DS} = 10% I_{DSS} = 9.7 mA is obtained. At this bias point, NFmin = 0.53 dB, R_n = 8.8Ω, NF = 0.9 dB, and G= 17 dB. The most interesting feature of these results is that the best noise performance has been achieved simultaneously with the maximum possible gain and transconductance so no trade-off had to be done between noise and gain.

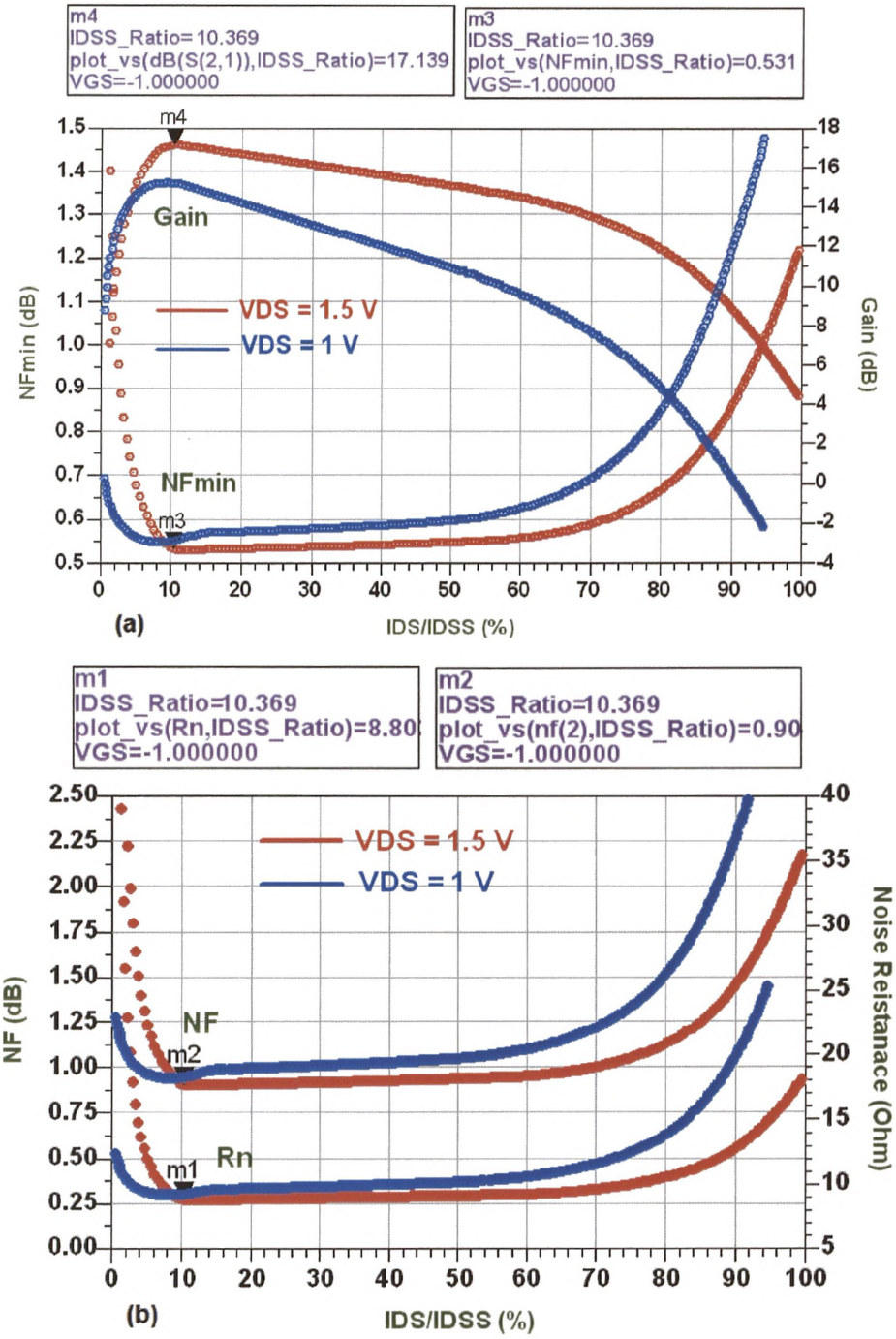


Figure 6.16 Investigation of the optimum DC bias point for the 2x200 µm device used at f = 2 GHz. (a) NFmin and Gain (b) NF and R_n.

6-5-1-3 Design and simulation of LNA circuit with all components on-chip

The only circuit configuration found to satisfy the SKA LNA design requirements without employing the feedback technique is the double-stage configuration. Figure 6.17 illustrates the double-stage circuit designed using a 2x200 µm device without inserting any inductors at the gate side (no input matching) to avoid the effect of their series resistances on the noise performance of the circuit.

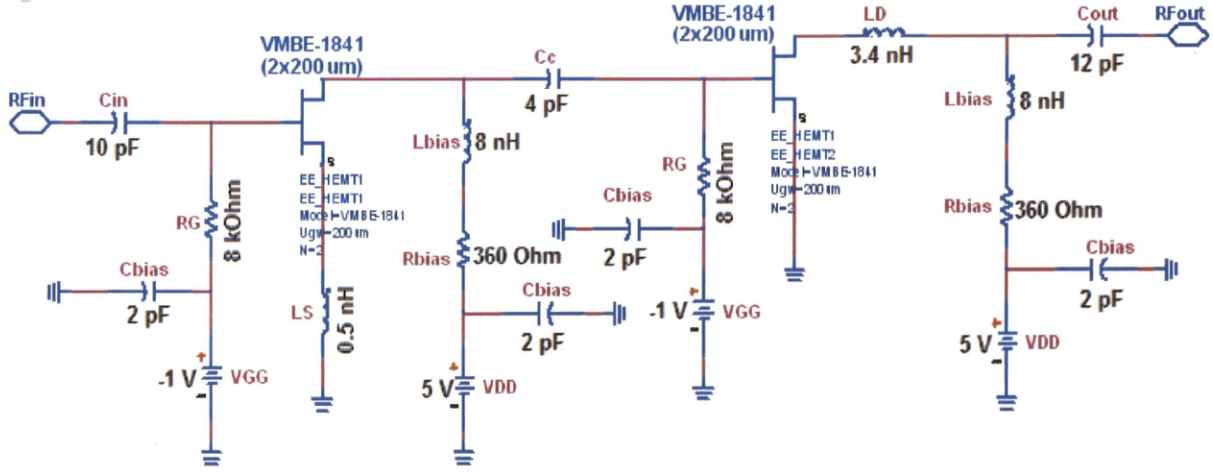


Figure 6.17 Schematic circuit diagram of the double-stage LNA designed using 2x200 µm device, sample VMBE-1841 (new process).

The S-parameters and noise simulation results of the above circuit are shown in Figure 6.18. The designed circuit with no input matching exhibits an average gain of 35 dB with an average noise figure of 0.87 dB (65 K) over the desired frequency band which is approximately 0.45 dB above N_{Fmin}. Also, poor SWR characteristics have been obtained below 1 GHz , all due to the absence of input matching.

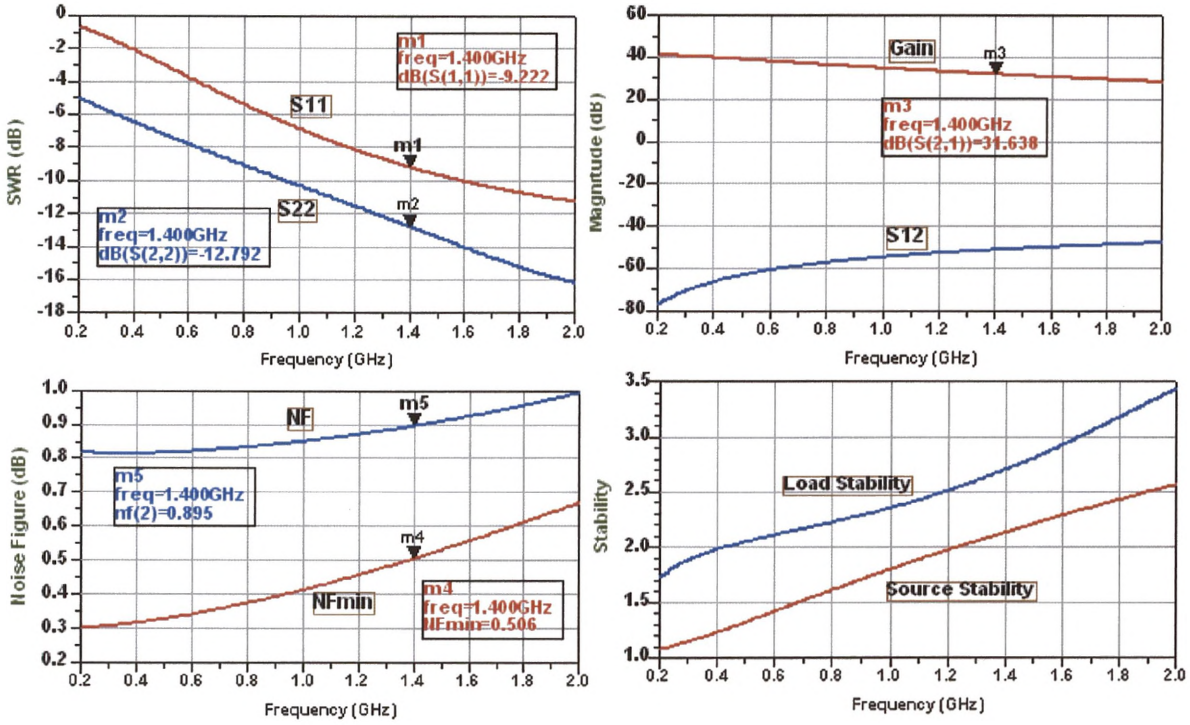


Figure 6.18 S-Parameters and noise simulation results of the double-stage LNA designed using 2x200 µm device, sample VMBE-1841 (new process).

6-5-1-4 Design and simulation of LNA circuit with some components off-chip

Due to the extreme importance of the input matching, as shown in the previous circuit, a 9.5 nH inductor was inserted at the gate side for this purpose but this inductor will be placed outside of the MMIC chip as shown in the circuit given in Figure 6.19. Also, the 8 k Ω resistor used for connecting the gate DC bias has been replaced by an off-chip 35 nH, a feature that will enhance the noise characteristics of the circuit. The main reason for using off-chip inductors is that compact air-core inductors have negligible series resistance (<< 1 Ω) .

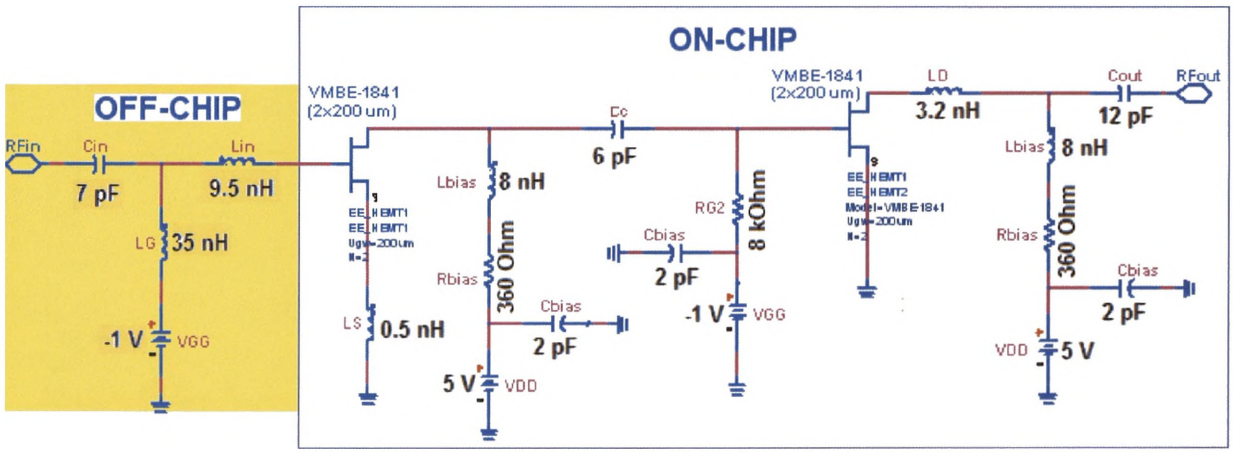


Figure 6.19 Schematic circuit diagram of the double-stage LNA designed using 2x200 µm device, sample VMBE-1841 (new process), with some elements off-chip.

The S-parameters and noise simulation results of the double-stage LNA circuit with some components off-chip are shown in Figure 6.20, from which can be noticed the great enhancement in the noise performance of the circuit, exhibiting an average noise figure of 0.55 dB (40 K). Also, much better SWR characteristics have been obtained over the entire frequency band of interest achieving most of the desired SKA specifications.

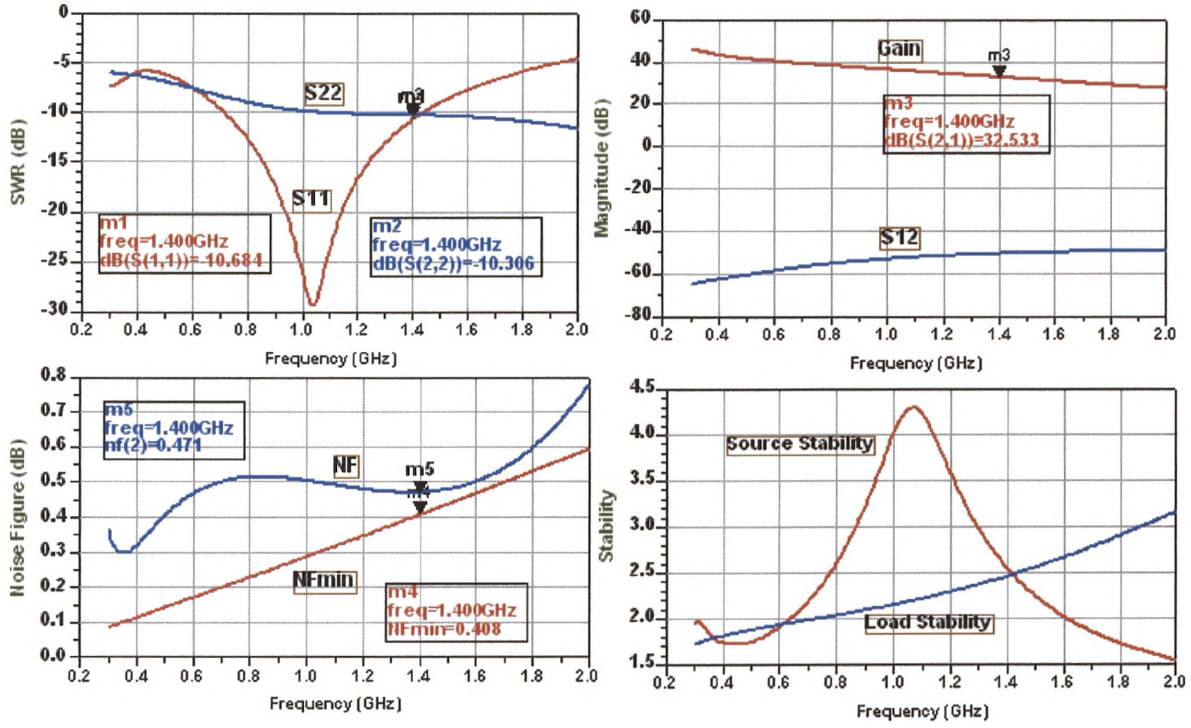


Figure 6.20 S-Parameters and noise simulation results of the double-stage LNA designed using 2x200 µm device, sample VMBE-1841 (new process), with some elements off-chip.

6-5-1-5 Linearity simulations of the 400 µm devices' LNAs

The two different LNA circuits designed using the 2x200 µm devices exhibit almost the same linearity characteristics providing a 1-dB compression point of 6 dBm as shown in Figure 6.21 and third-order intercept of 12 dBm of the output power as shown in Figure 6.22.

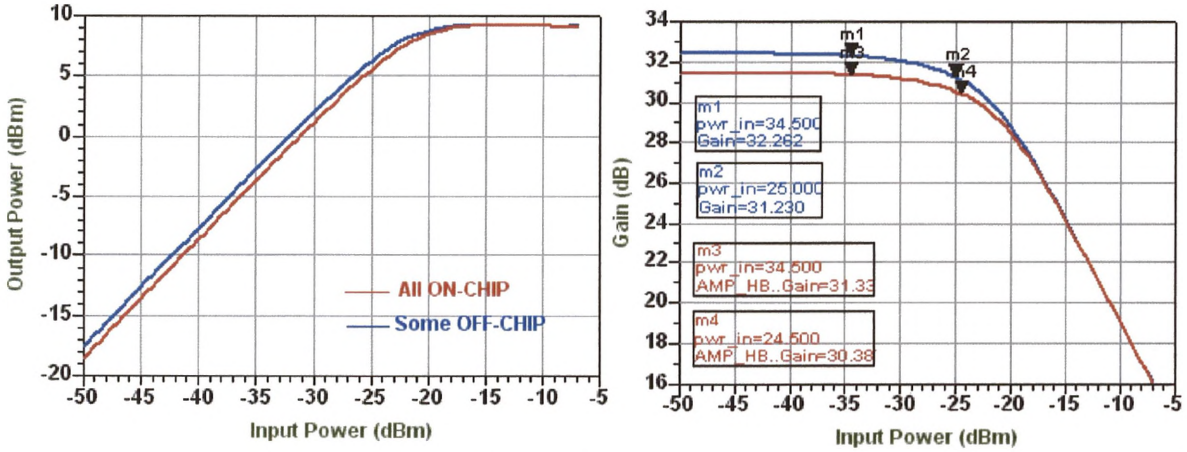


Figure 6-21 Linearity Simulations of the designed LNAs using 2x200 µm device, VMBE-1841 (new process) at f = 1.4 GHz.

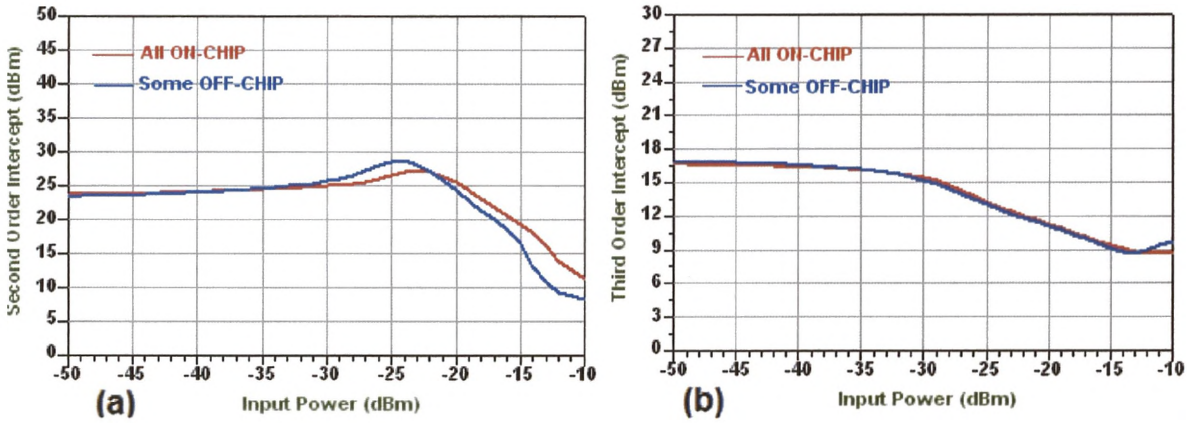


Figure 6-22 Second and third order intercepts of the designed LNAs using 2x200 µm device, VMBE-1841 (new process) at f = 1.4 GHz.

6-5-1-6 Efficiency calculations of the 400 µm devices' LNAs

Figure 6.23 shows the efficiency calculations of the 2x200 µm LNA circuits, illustrating the worst amplifier efficiencies among all designed circuits (28 %) due to their relatively low gain and high DC power consumption.

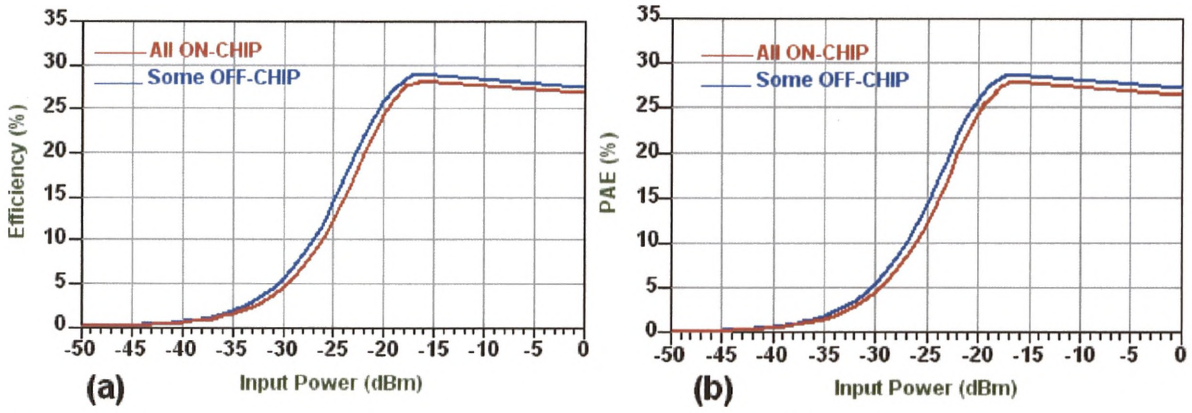


Figure 6-23 Efficiency calculations of the designed LNAs using 2x200 µm device, VMBE-1841 (new process) at f = 1.4 GHz.

6-5-2 LNA design using 800 µm device

As the MMIC LNA circuit designed using the 400 µm devices does not satisfy all of the desired goals, especially the noise, input SWR, and higher order intercepts, thoughts were directed towards the use of larger gate width and multi-gate finger devices as they should exhibit better gate resistances and lower noise resistances as discussed in chapter-4.

6-5-2-1 400 µm device model scaling

Unfortunately, the multi-gate finger process employing the air-bridges technique has not yet been applied for the best sample in the new process, VMBE-1841. Since this the main sample of interest during this work, the EE-HEMT large-signal nonlinear model of a 400 µm (2x200 µm) device was scaled in terms of (number of gate fingers, gate-source capacitance, transconductance parameter.....etc) to represent the 800 µm (4x200 µm). Figure 6.24 shows a comparison between the gain and noise parameters of these devices illustrating the much better performance of the 800 µm device (higher gain, lower Rn, NF), the slight degradation in N_{Fmin} can be easily recovered by using multi-finger devices.

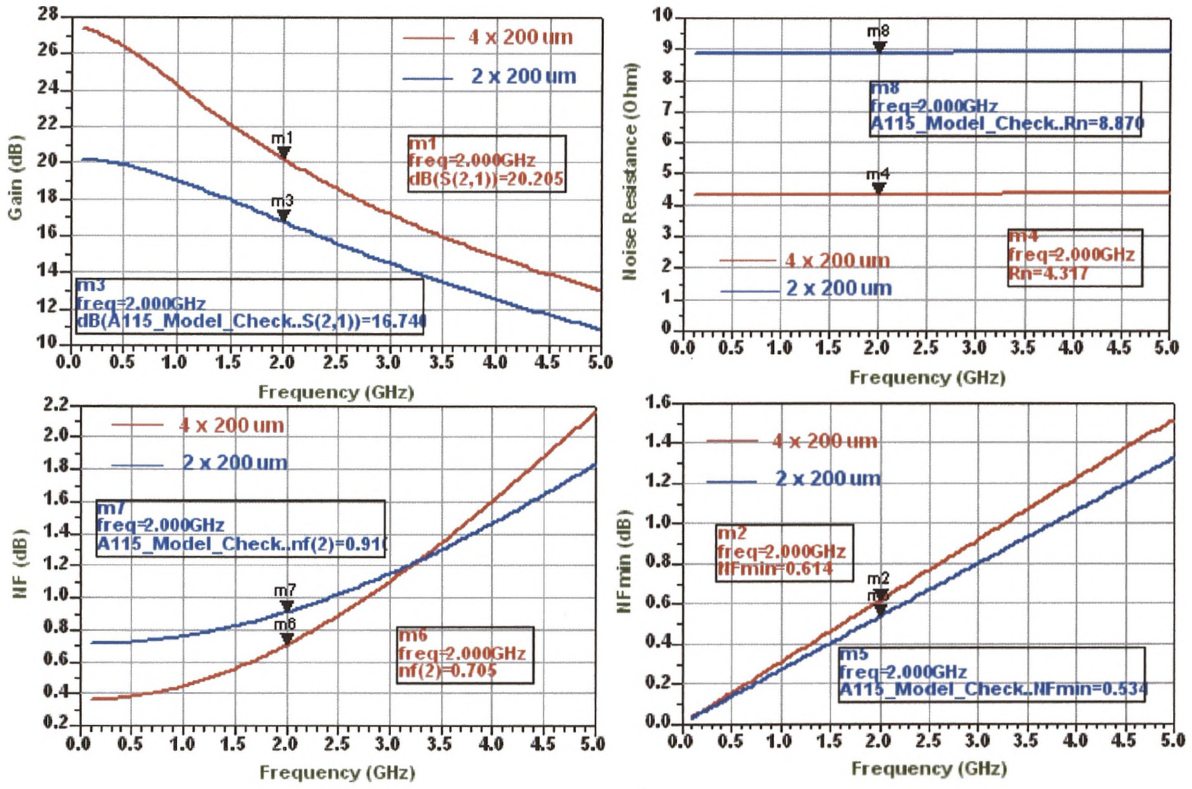


Figure 6.24 Comparison between gain and noise parameters of the 2x200 µm and 4x200 µm devices, sample VMBE-1841 (new process).

6-5-2-2 Design and simulation of LNA circuit with all components on-chip

Figure 6.25 shows a single-stage LNA circuit designed using the scaled model of the 4x200 µm device biased under the same DC biasing conditions as the 400 µm device. The S-parameters and noise simulation results of the circuit are shown in Figure 6.26. The designed circuit with no input matching exhibits an average gain of 18 dB with average noise figure of 0.5 dB (36 K) which is only 0.15 dB above N_{Fmin} and with acceptable in/out SWR over the desired frequency band illustrating the great enhancement in the overall circuit performance compared with the corresponding 400 µm device's circuit.

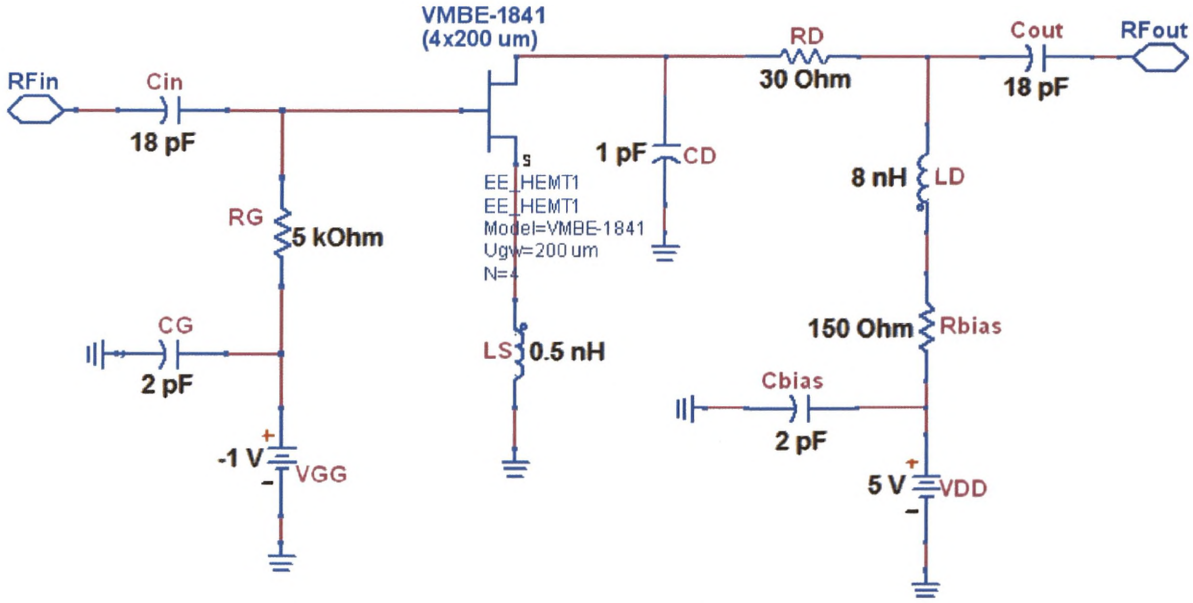


Figure 6.25 Schematic circuit diagram of the LNA circuit designed using 4x200 µm device, sample VMBE-1841 (new process).

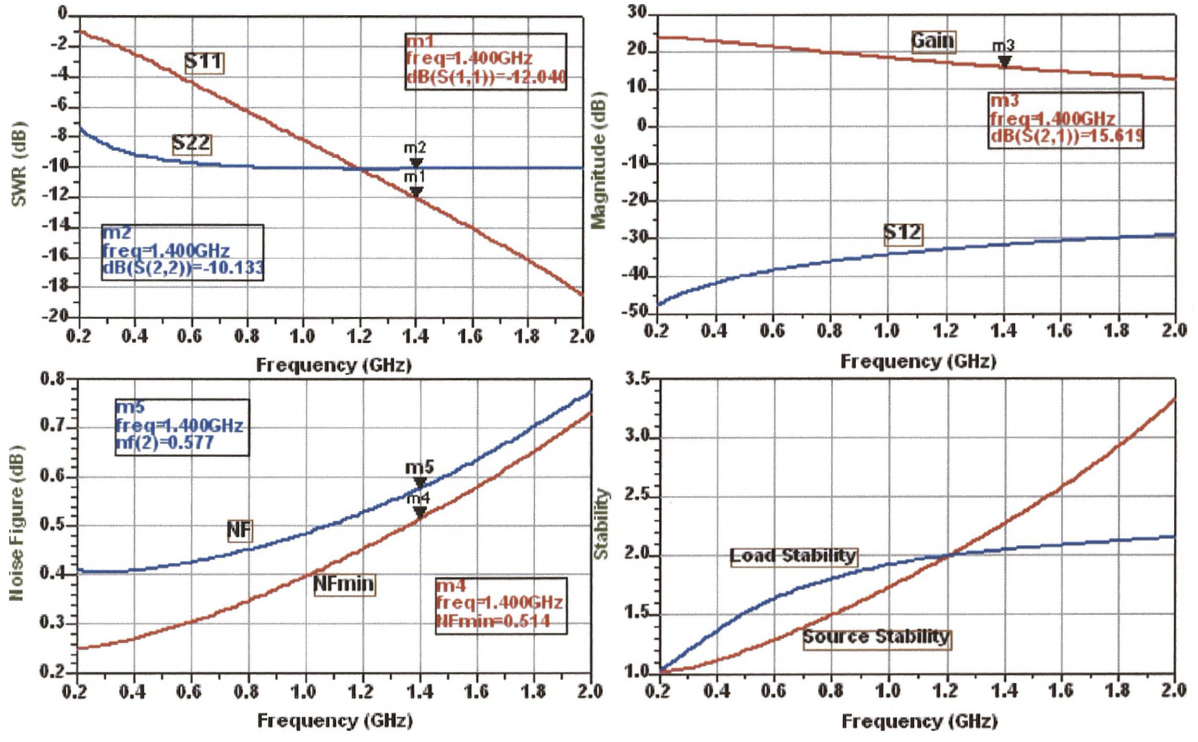


Figure 6.26 S-Parameters and noise simulation results of the LNA circuit designed using 4x200 µm device, sample VMBE-1841 (new process).

6-5-2-3 Design and simulation of LNA circuit with some components off-chip

The LNA circuit designed using the 4x200 µm device with an off-chip input matching inductor is shown in Figure 6.27. It should be noticed that the inductor value required for input matching in this circuit is much lower than the corresponding one in the 400 µm device circuit, 3.3 nH instead of 9.5 nH, reflecting the great simplicity of matching the input impedance of the larger gate width devices to Γ_{opt} compared with smaller gate width devices.

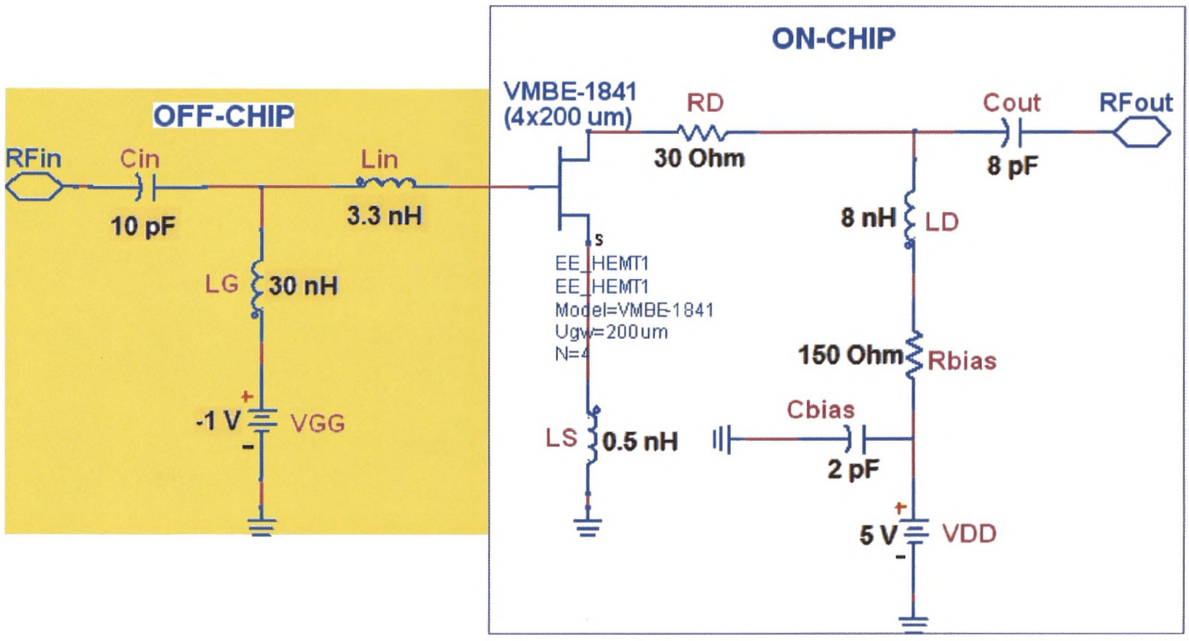


Figure 6.27 Schematic circuit diagram of the LNA circuit designed using 4x200 µm device, sample VMBE-1841 (new process) with some elements off-chip.

The S-parameters and noise simulation results of the above circuit are shown in Figure 6.28, from which it can be seen that the designed circuit satisfies all of the desired goals, providing an average gain of 19 dB. An average, room temperature, noise figure of 0.45 dB corresponding to an equivalent noise temperature of 32 K, is obtained over the frequency band of interest with adequate input/output SWR

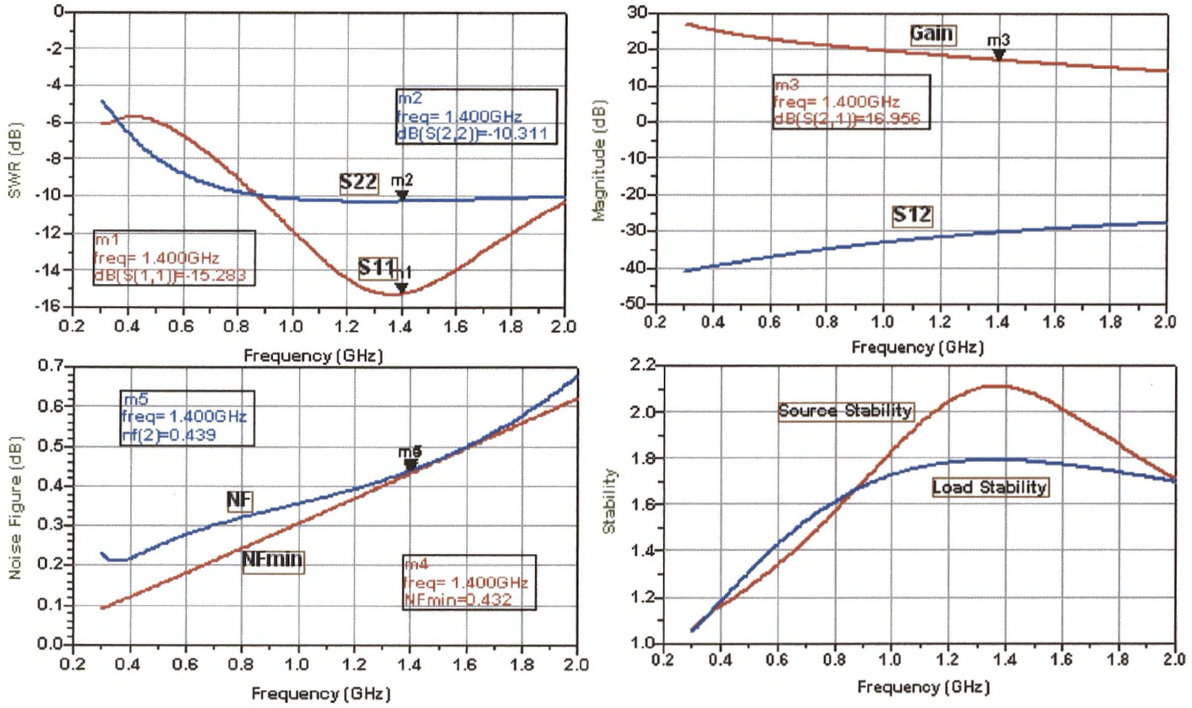


Figure 6.28 S-Parameters and noise simulation results of the LNA circuit designed using 4x200 µm device, sample VMBE-1841 (new process) with some elements off-chip.

6-5-2-4 Linearity simulations of the 800 µm devices' LNAs

The LNA circuits designed using the 800 µm devices exhibit 1-dB compression points over 10 dBm of the output power, as shown in Figure 6.29, and third-order intercept points over 20 dBm as given in Figure 6.30 satisfying all of the desired linearity requirements.

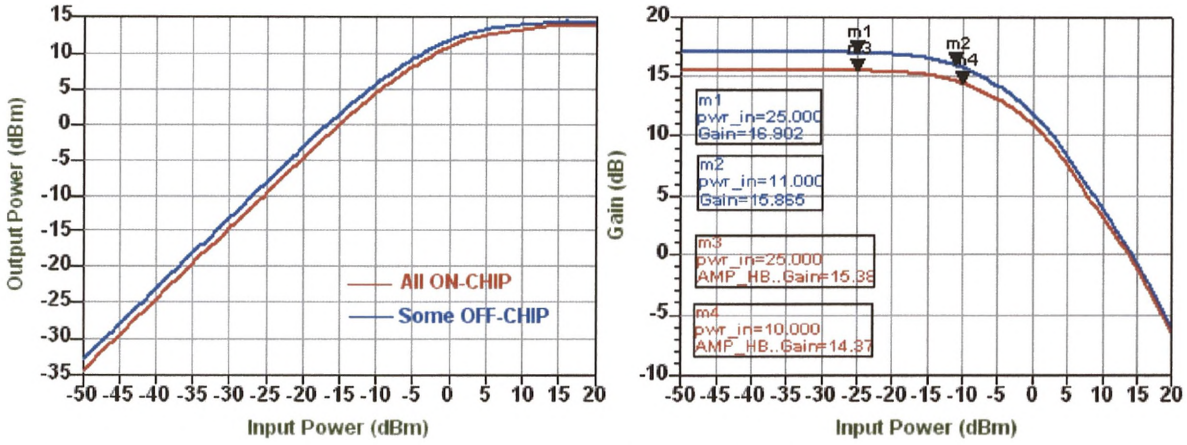


Figure 6.29 Linearity simulations of the LNA circuits designed using 4x200 µm device, sample VMBE-1841 (new process) at f = 1.4 GHz.

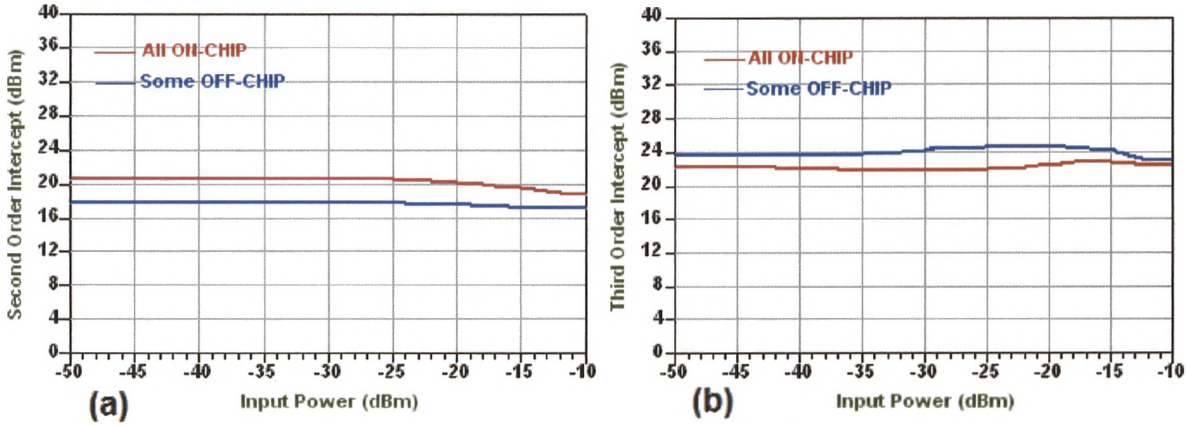


Figure 6.30 Second and third order intercepts of the LNA circuits designed using 4x200 µm device, sample VMBE-1841 (new process) at f = 1.4 GHz.

6-5-2-5 Efficiency calculations of the 800 µm devices' LNAs

high power added efficiency has been obtained for the 4x200 µm device's circuits (~50 %), as shown in Figure 6.31, satisfying the efficiency requirements of the LNA circuit design.

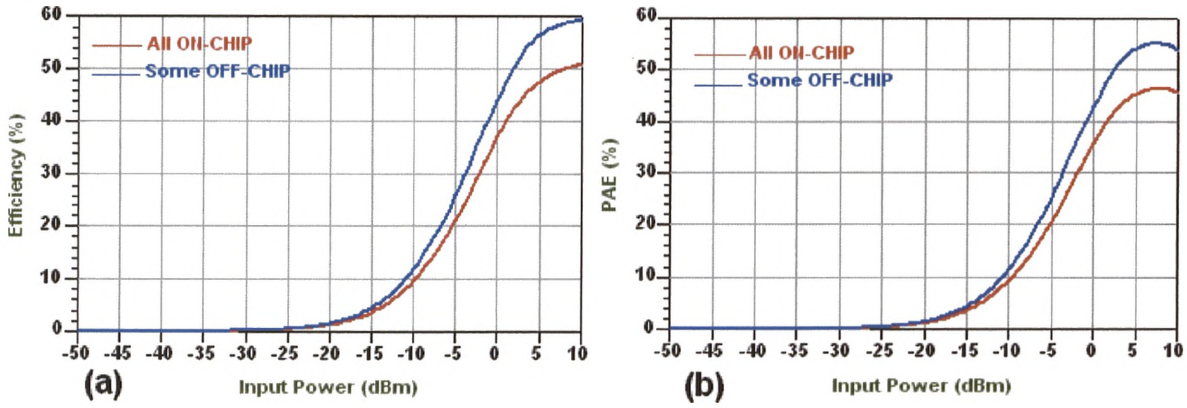


Figure 6.31 Efficiency calculations of the LNA circuits designed using 4x200 µm device, sample VMBE-1841 (new process) at f = 1.4 GHz.

6-6 Masks Generation

Conversion of the MMIC design into a layout (mask) can be accomplished in two ways; the first uses a commercially available CAD software program to manually perform the layout from a hard copy of the schematic or net-list. The second uses advanced software tools, such as Cadence or HP/EEsof, to transfer the schematic to layout in real time. The output from these programs can then be modified to comply with foundry design rules.

In this work, although the ADS software package, used in the design and simulation, can automatically generate a circuit layout from the schematic it, unfortunately, does not contain any libraries for passive components in the CPW form (inductors, capacitors, resistors, Tee- or Cross-junctions.... etc) and thus the first method was used.

The circuit layouts were generated to satisfy the requirements of a ten-steps (eight-masks) process for fabricating the MMIC LNA circuit, described as below: -

(1) MASK-1 (Mesa definition)

In this step, the unwanted active layers are removed by chemical etching to access the semi-insulating substrate or the undoped buffer layer.

(2) MASK-2 (Metal-1)

A photoresist-masking step used for defining the desired ohmic-metal contacts for the transistor's source and drain.

(3) MASK-3 (Metal-2)

In this step, a thin metal layer of Ti/Au (0.5 μm thick) is evaporated forming all of the following: -

-Gate metallization, giving the desired Schottky contact

-Ground plane metallization

-Spiral inductors and MIM capacitors bottom plates

(4) A layer of silicon nitride (Si_3N_4) covering all areas and forming the dielectric layer for capacitors is then applied.

(5) MASK-4 (Si_3N_4-Etch)

A photoresist-masking step used to remove (Etch) Si_3N_4 from all areas except of capacitor plates.

(6) MASK-5 (NiCr-deposition)

A thin layer of NiCr is then sputtered at certain positions forming the desired thin film resistors. Thickness of this layer will be specified according to the required sheet resistance value, as discussed in Chapter-5.

(7) MASK-6 (Metal-3)

Another layer of Ti/Au metal (0.5 μm thick) is now deposited identifying the MIM capacitors top plates along with NiCr resistors Ohmic-contacts and the inter-connects between different components.

(8) A thick layer of polyimide (900 nm thick), is applied covering all areas and forming the spiral inductor dielectric layer (insulation).

(9) MASK-7 (Vias)

A photoresist-masking step used for identifying Vias (windows) to access the spiral inductors' bottom plate and ground plane (for the grounded components).

(10) MASK-8 (Metal-4)

Finally, a thick layer of Ti/Au metal (1 μm thick) is evaporated forming the inductors top plates (spirals).

Figure 6.32 illustrates the physical layout of the MMIC LNA circuit of the 2x100 μm device, sample VMBE-1841 (old process) generated according to the fabrication process flow discussed above with total circuit area of approximately 2 mm^2.

The physical layout of the MMIC LNA circuit, designed using a 4x200 μm device, sample VMBE-1841 (new process), is shown in Figure 6.33 with total circuit area of 2 mm^2.

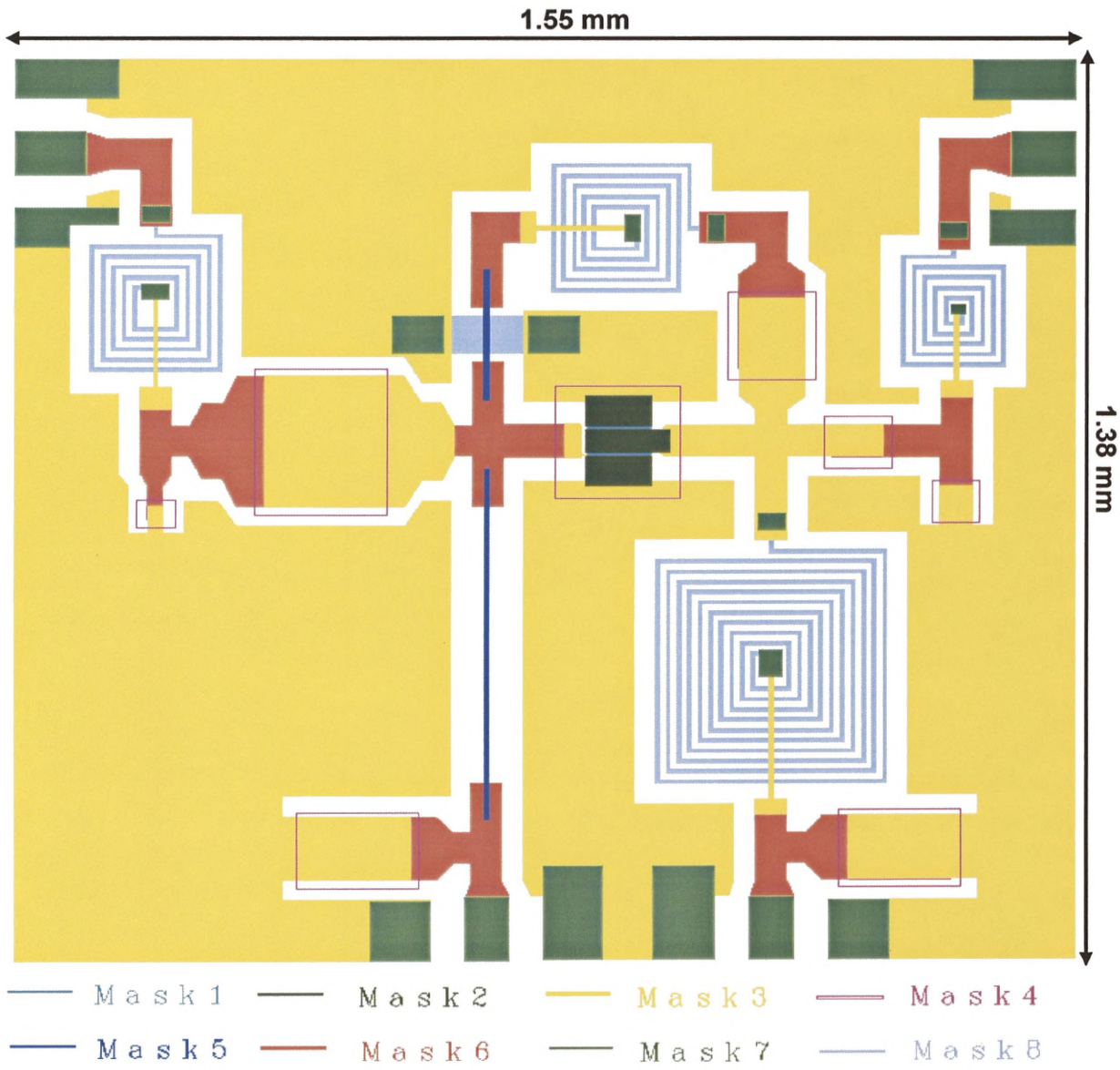


Figure 6.32 Circuit layout (Mask) of the MMIC LNA designed using 2x100 µm device, sample VMBE-1841 (old process).

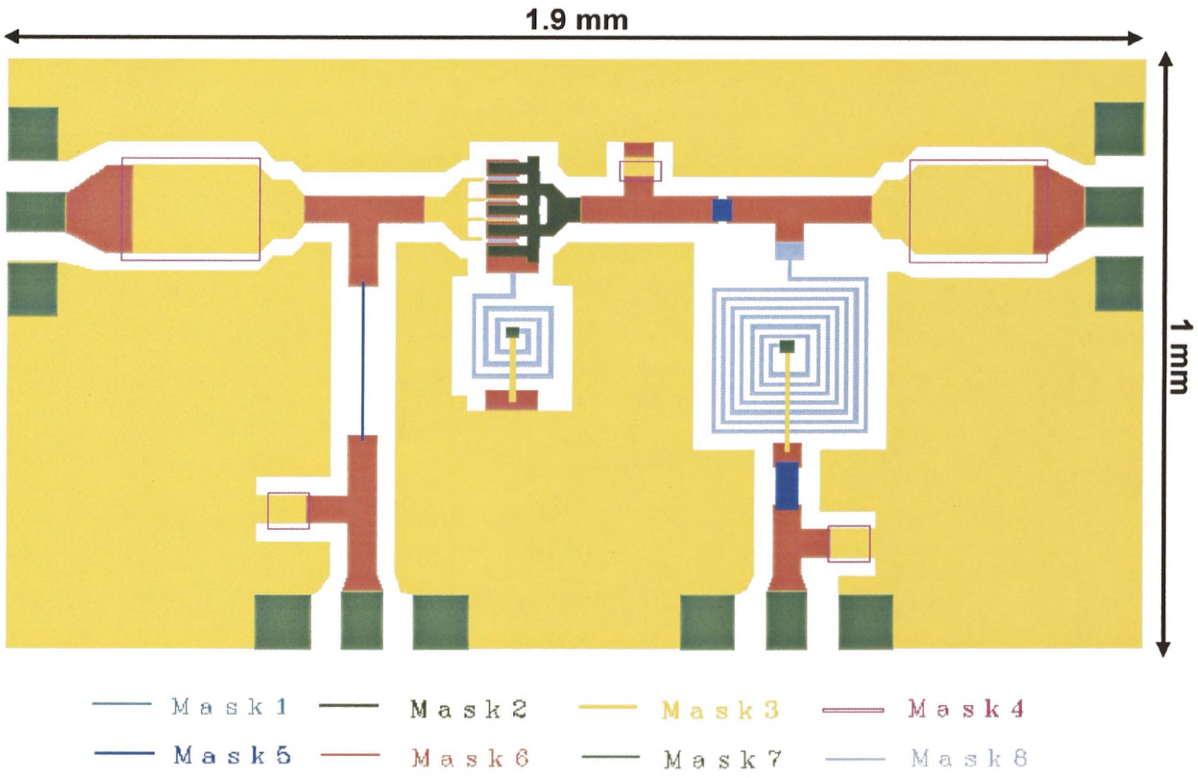


Figure 6.33 Circuit layout (Mask) of the MMIC LNA designed using 4x200 µm device, sample VMBE-1841 (new process).

6-7 Chapter Summary

In this chapter, a family of MMIC LNA circuits was designed based on the in-house fabricated 1 µm strained gate, InGaAs/InAlAs/ InP pHEMT devices in the frequency band of 0.3–2 GHz for potential use in the SKA radio telescope being now internationally planned.

The first generation of the designed LNA circuits, based on the old process samples, exhibited a relatively poor noise performance unsatisfying all of the desired specification due to all of the following:-

- Relatively poor noise characteristics of the single devices because of thin gate metallization scheme applied increasing NFmin of the transistors.
- Relatively small gate widths (200 µm) of the used devices providing them with high noise resistances and poor input impedance characteristics.

- The negative feedback technique applied further increased the noise performance of the designed circuits.

The second generation of the designed LNAs based on the new process samples, with the thick gate metallization, exhibited much better noise performance satisfying all of the desired specifications especially the large gate-width (800 μm) and multi-gate finger devices.

Finally, a great deal of difficulty was found during the design of the required LNAs using the commercial sub-micron HJ-FETs due to their high noise resistance and very poor input impedance features at low microwave frequencies (< 4 GHz).

CHAPTER-7

Conclusions and Future Work

7-1 Conclusions

Realizing a high performance, small size, reliable, and low cost Monolithic Microwave Integrated Circuits (MMICs) is one of the key issues for satellite communication and radio astronomy applications, especially for the upcoming world's largest radio telescope, the square kilometer array (SKA), which is now internationally planned.

In a typical receiver systems, the low noise amplifier (LNA) is the primary key component sitting in the RF front-end which should not only supply sufficient gain to suppress the overall noise figure but also have adequate bandwidth to cover the desired frequency band of operation.

The work presented here focused on designing MMIC broadband LNAs based on InP material system that are tailored to the SKA telescope requirements.

During this work, an extensive experimental microwave characterization and device modeling, together with numerical simulations using suitable linear and non-linear transistor models has been carried out for a University of Manchester in-house fabricated 1 μm strained gate high breakdown InGaAs-InAlAs InP-based pHEMTs. Complete agreements with experimental data were found on different transistor

processes. DC, RF, and noise behaviours of the new devices were successfully modeled.

Also in the scope of this work, different MMIC passive Components such as spiral inductors, MIM capacitors, and thin film resistors were designed, fabricated, and measured. Then, accurate lumped element circuit models were extracted for these components.

All of the extracted models for active and passive components have been used for the design, simulation, and circuit mask generation of an L-band MMIC CWP InP-pHEMT LNA. The designed circuits satisfy most of the desired specifications providing a room temperature noise figure as close as possible to NF_{min} with adequate gain and return loss properties especially for the large gate width and multi-gate finger devices.

Many difficulties were found during the design of MMIC broadband LNAs at the SKA low frequency band using small gate width (< 400 μm) and short gate length (< 0.5 μm) devices due their high noise resistance and poor input impedance nature. The real breakthrough came from the development of a high breakdown, low leakage InGaAs-InAlAs pHEMT material synthesized at the University of Manchester which was then successfully used in the design and fabrication of 1 um gate length, very large gate width low noise transistor which were both stable and had low noise resistance in the 0.3 to 2GHz band of interest of the SKA.

7-2 Suggestions for Further Work

A great deal of work has been done in the area of producing high performance wide-band LNAs suitable for radio-astronomy applications especially for future telescopes such as the square kilometer array (SKA) system. The work performed so far has led the foundation for future LNA circuits, already under way, and which will include:

- Nonlinear large-signal models for the multi-gate finger devices based on real (practical) measurements of the fabricated four/six gate finger pHEMTs from the best samples structures grown in house (VMBE-1841 or equivalents).

• Using in-house fabricated InP-pHEMTs for more enhanced noise behavior with shorter gate lengths (0.5-0.6 μm) using a special photo-lithography technique (deep-uv), avoiding the high-cost E-beam technique for gate formation.

• Enhancing the electrical characteristics and physical areas of the used passive elements by using:-

- Different topologies of spiral inductors such as circular spirals with smaller line widths and separations (5-6 μm).
- Higher dielectric constants or smaller thickness for the dielectric material of the MIM capacitors

This work has hopefully laid down the foundation for compact, high efficiency, low power dissipation low noise amplifiers for use in the Square Kilometer Array telescope.

Appendix-A

Useful Expressions for HEMTs

(1) Quantised energy levels in Triangular QW (E_i) **[21]**

$$E_i=\left(\frac{h^2}{2m^*}\right)^{\frac{1}{3}}\left(\frac{3\pi}{2}q\xi_s\right)^{\frac{2}{3}}\left(i+\frac{3}{4}\right)^{\frac{2}{3}},\ i = 0, 1, 2,..... \quad (A.1)$$

ξ_s..... Effective electric field at the interface.

For GaAs, the lowest sub-bands are given by:-

$$E_0=1.83x10^{-6}x\xi_s^{2/3}\ \ eV \quad (A.2)$$

$$E_1=3.23x10^{-6}x\xi_s^{2/3}\ \ eV \quad (A.3)$$

(2) 2DEG charge density (n_s) **[31]**

$$n_s(y)=\frac{C_i\left[V_{GS}-V_{TH}-V_{DS}(y)\right]}{q} \quad (A.4)$$

$$C_i=\frac{\varepsilon_0\varepsilon_s}{d_d+d_i+\Delta d} \quad (A.5)$$

C_i..... Depletion layer capacitance

d_d.....Thickness of the doped AlGaAs region

d_i.....Thickness of the undoped AlGaAs region

Δd is the effective width of the 2DEG, given by:-

$$\Delta d=\frac{\varepsilon_0\varepsilon_s a}{q} \quad (A.6)$$

(3) Source-Drain Saturation Current (I_{DS})

$$I_{DS} = \frac{W}{L_g}\mu_n C_i (V_{GS}-V_{TH})^2 \quad (A.7)$$

(4) Source Parasitic Resistance (Rs) **[68]**

$$R_S = R_C + r_S \quad (A.8)$$

R_C is the Ohmic contact resistance and r_S is the sheet resistance of the material out side the intrinsic channel region, given by:-

$$R_C = \frac{1}{W}\sqrt{\frac{\rho_c}{q\mu n_S}} \quad (A.9)$$

$$r_S = \frac{L_{sg}}{q\mu N_S W} \quad (A.10)$$

W.....Gate Width

ρ_C.....Contact resistivity

L_{sg}.....Gate-source separation

(5) Transconductance (g_m)

$$g_{mi} = \frac{\partial I_{DS}}{\partial V_{GS}}\bigg|_{V_{DS}=\text{constant}} = \frac{2I_{DS}}{(V_{GS}-V_{TH})} \quad (A.11)$$

g_{mi} is the intrinsic transconductance and the extrinsic transconductance, g_m, is given by

$$g_m = \frac{g_{mi}}{1+g_{mi}R_S} \quad (A.12)$$

(6) Drain (output) conductance (g_{ds})

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}}\bigg|_{V_{GS}=\text{constant}} = \frac{\lambda}{(1+\lambda V_{DS})} I_{DS} \quad (A.13)$$

(7) Threshold voltage (V_T)

$$V_T = \Phi_b - (\Delta E_c - E_F) - V_p \quad (A.14)$$

Φ_b----------Schottky barrier height on n-doped AlGaAs

ΔE_c----------The conduction band discontinuity at the AlGaAs/GaAs Hetero-interface

V_p ---------- Pinch-off voltage

(8) Pinch-off Voltage (V_p)

$$V_p = \frac{qN_{d(AlGaAs)}d_d^2}{2\varepsilon_0\varepsilon_s} \tag{A.15}$$

(9) Cut-off Frequency

$$f_T = \frac{\upsilon_{sat}}{2\pi L_g} = \frac{g_m}{2\pi C_{gs}} \tag{A.16}$$

(10) Maximum Frequency of oscillation **[67]**

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_S+R_g+R_i}{R_{ds}}+2\pi f_T R_g C_{gd}}} \tag{A.17}$$

Appendix-B

Linear Model Extraction Technique in the ADS

The small-signal linear model parameters extraction technique incorporated in the ADS, according to the numerical analysis discussed in chapter-4, is shown here. Figure B.0.1 shows the extraction algorithm of the eight extrinsic parameters from the pinched device measurements.

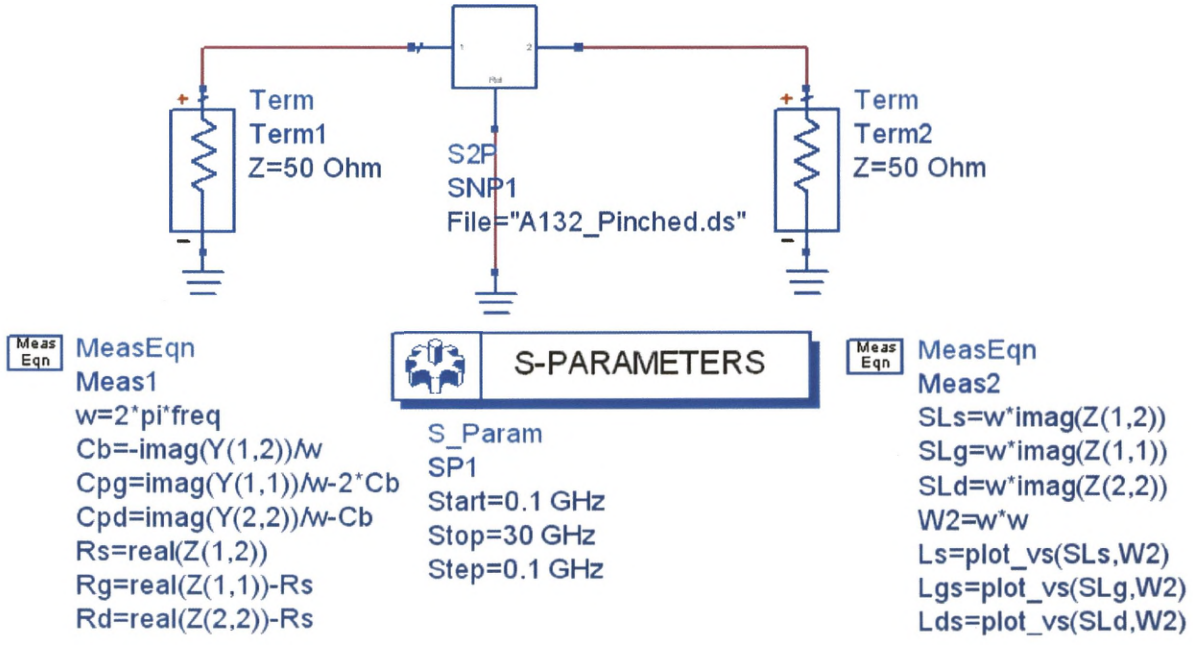


Figure B.0.1 Extraction of the eight extrinsic parameters from the pinched device measurements.

Figure B.0.2 shows the extraction algorithm of the seven intrinsic parameters from the hot (active) device measurements after de-embedding the measured S-Matrix with the extracted parasitic elements through a series of matrix transformation.

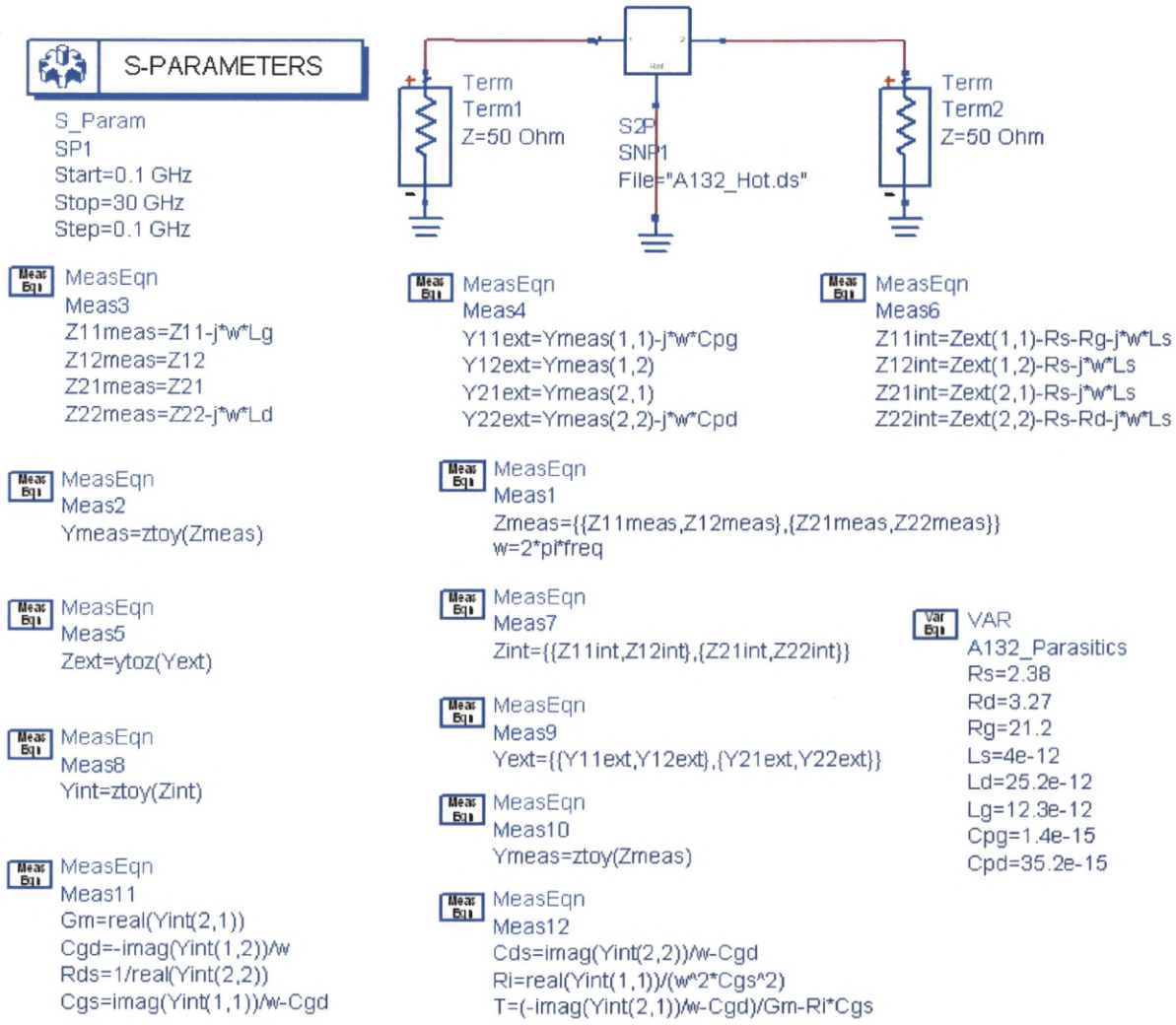


Figure B.0.2 Extraction of the seven intrinsic parameters from the hot (active) device measurements.

Table B.0.1 shows the linear small-signal model parameters extracted for different gate width devices (sample-1832, old process), all biased at V_{DS} = 1.5 V, V_{GS} = -0.6V. Table B.0.2 shows the noise parameters calculated for the same devices.

Size (μm) →		2x100	2x80	2x60	2x40	2x20
Intrinsic Model Parameters	G_m (ms)	55	45	36	25	14
	T(psec)	1.9	1.95	1.9	2	2
	R_i (Ω)	4.6	4.8	5.2	6.25	9.3
	R_{ds} (Ω)	380	495	660	1240	1840
	C_{gs} (pF)	0.4	0.36	0.29	0.17	0.083
	C_{ds} (pF)	0.041	0.033	0.028	0.019	0.017
	C_{gd} (pF)	0.037	0.027	0.02	0.017	0.014
Extrinsic Model Parameters	R_s (Ω)	2.25	2.5	3.5	3.9	7.4
	R_g (Ω)	17.2	15.3	13.5	11.8	11.2
	R_d (Ω)	3.2	3.8	4.2	4.5	5.7
	L_s (pH)	5.5	5.8	4.5	4.2	4
	L_g (pH)	14.35	11.4	10.2	8.5	4.8
	L_d (pH)	14.3	12.1	10.2	7.8	5.4
	C_{pg} (fF)	2.5	1.5	1.5	1.2	1.2
	C_{pd} (fF)	28.4	26.3	22.5	21.2	20

Table B.0.1 Linear small-signal model parameters for different gate width devices from sample VMBE-1832 (old process), all biased at V_{ds} = 1.5 V and V_{gs} = -0.6 V.

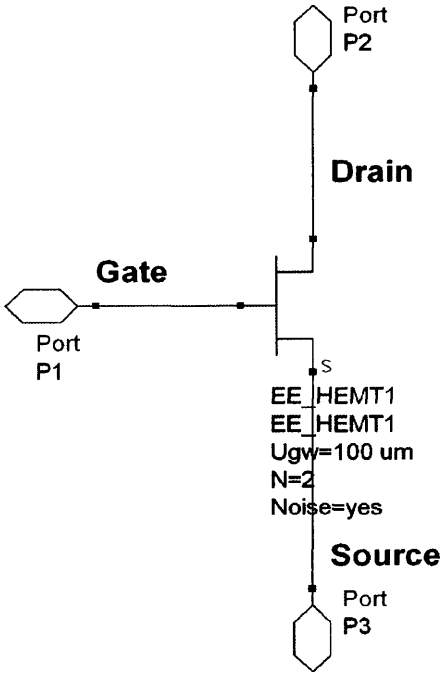
Size →	2x100	2x80	2x60	2x40	2x20
Bias Point	1.5, -0.6, 35.4 mA	1.5, -0.6, 27.8 mA	1.5, -0.6, 20.7 mA	1.5, -0.6, 14.1 mA	1.5, -0.6, 6.6 mA
F_T (GHz)	29.4	29	30.6	28.6	28.3
NFmin@2GHz	0.937	0.887	0.74	0.68	0.66
R_n (Ω)	28.7	44.3	69.7	143.7	458

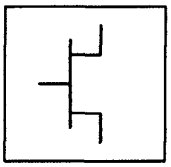
Table B.0.2 Predicted room temperature noise parameters of different gate width devices from sample VMBE-1832 (old process).

Appendix-C

EE-HEMT Nonlinear Large-Signal Model Parameters

The EE-HEMT nonlinear Large-signal model parameters of a 2x100 µm device from sample VMBE-1841 (old process) are given below as an example for the extracted nonlinear models. A detailed description for all model parameters is given in the tables below.





EE_HEMT1_Model
EEHEMTM1

Vto=-0.78 V	Cdso=44.85356 fF	Lambda=0.726	Mu=0.1
Gamma=0.02	Rdb=0.61 GOhm	C12sat=29.50 fF	Deltgm=0.044
Vgo=-0.56 V	Cbs=65.1552 fF	Cgdsat=98.38 fF	Deltgmac=0.01145
Vch=1.75 V	Vtoac=-0.776 V	Kbk=0.0298	Alpha=0.2 V
Gmmax=90 mH	Gammaac=0.098	Vbr=24.88 V	Tnom=25
Vdso=1.6 V	Gmmaxac=0.146	Nbr=1.99	
Vsat=0.8 V	Kapaac=35.42 mS	Idsoc=61.5 mA	
Kapa=98 mS	Peffac=1.118	Rd=3.16 Ohm	
Peff=1.8	Vtsoac=-47.89 V	Rs=2.138 Ohm	
Vtso=-100.0 V	Gdbm=59.21 uF	Rg=19.73 Ohm	
Is=192 nA	C11o=0.929 pF	Ugw=100 um	
N=1.623	C11th=0.557 pF	Ngf=2	
Ris=240.57 mOhm	Vinfl=1 V	Vco=-0.49 V	
Rid=216.237 mOhm	Deltgs=0.626 V	Vba=1.000 V	
Tau=2.16412 psec	Deltds=0.189 V	Vbc=0.58 V	

Parameter	Definition	Unit
Vto	Zero-bias threshold parameter	V
Gamma	Transconductance parameter	1/V
Vgo	Gate-source voltage where Gm is a maximum	V
Vch	VGS where Gamma no longer effects I-V	V
Gmmax	Peak transconductance parameter	mH
Vdso	Drain voltage where Vo dependence is nominal	V
Vsat	Drain-source current saturation parameter	V
Kapa	Output conductance parameter	mS
Peff	Channel to backside self-heating parameter	W
Vtso	Sub-threshold onset voltage	V
Is	Gate junction reverse saturation current	nA
N	Junction ideality factor	-
Ris	Source end channel resistance	Ω
Rid	Drain end channel resistance	Ω

Parameter	Definition	Unit
Tau	Gate transit time delay	Psec
Cdso	Drain source inter-electrode capacitance	fF
Rdb	Dispersion source output impedance	GΩ
Cbs	Trapping-state capacitance	fF
Vtoac	Zero-bias threshold parameter (AC)	V
Gammaac	Transconductance parameter (AC)	1/V
Gammaxac	Peak transconductance parameter (AC)	-
Kapaac	Output conductance parameter (AC)	mS
Peffac	Channel to backside self-heating parameter (AC)	W
Vtsoac	Sub-threshold onset voltage (AC)	V
Gdbm	Additional d-b branch conductance at Vds = Vdsm	µF
C11o	Maximum input capacitance for VDS=Vdso	fF
C11th	Min. (threshold) input capacitance for Vds = Vdso	fF
Vinfl	Inflection point in C11-Vgs characteristic	V
Deltgs	C11th to C11o transition voltage	V
Deltds	Linear to saturation region transition parameter	V
Lambda	C11-Vds characteristic slope parameter	1/V
C12sat	Input trans-capacitance for Vgs = Vinfl	fF
Cgdsat	Gate drain capacitance for Vds > Deltds	fF
Kbk	Breakdown current coefficient at threshold	-
Vbr	Breakdown onset voltage	V
Nbr	Breakdown current exponent parameter	-
Idso	Open channel (maximum) value of Ids	mA
Rs	Source contact resistance	Ω
Rd	Drain contact resistance	Ω
Rg	Gate metallization resistance	Ω
Ugw	Gate width of device	µm
Ngf	Number of device gate fingers	-
Vco	Voltage where Gm compression begins	V
Vba	Gm compression tail-off parameter	V

Parameter	Definition	Unit
Vbc	Gm roll-off to tail-off voltage	V
Mu	Vo dependent transconductance compression parameter	-
Deltgm	Slope of Gm compression characteristics	-
Deltgmac	Slope of Gm compression characteristic (AC)	-
Alpha	Gm saturation to compression transition	V
Tnom	Nominal ambient temperature	C

Appendix-D

GaAs/AlGaAs Fabricated devices

D-1 Epitaxial Layer Structures

Layer	VMBE-1864	VMBE-1891	
Cap	GaAs (50 Å)	GaAs (50 Å)	
Supply	$Al_{0.45}Ga_{0.55}As$ (200 Å)	$Al_{0.36}Ga_{0.64}As$ (200 Å)	
δ-doping	$5x10^{12}$ cm^{-2}	$5x10^{12}$ cm^{-2}	
Spacer	$Al_{0.45}Ga_{0.55}As$ (50 Å)	$Al_{0.36}Ga_{0.64}As$ (150 Å)	
Channel	$In_{0.15}Ga_{0.85}As$ (110 Å)	GaAs	**5340 Å**
	$Al_{0.36}Ga_{0.64}As$ (486 Å)	GaAs	
	GaAs (5000 Å)	GaAs	
Buffer	GaAs (54 Å)	GaAs (50 Å)	**X10**
	$Al_{0.36}Ga_{0.64}As$ (55 Å)	$Al_{0.34}Ga_{0.66}As$ (50 Å)	
	GaAs (1000Å)	GaAs (1000Å)	
S. I. Substrate	GaAs (0.5 μm)	GaAs (0.5 μm)	

Table D.0.1 Epitaxial layer structures of the fabricated GaAs/AlGaAs samples.

D-2 Hall Measurements

Sample	n_H ($x10^{12}$ cm^{-2})		μ_H ($cm^2/V.s$)	
	RT	77 K	RT	77K
VMBE-1864	1.49	1.64	6525	23600
VMBE-1891	0.536	0.52	8220	106000

Table D.0.2 Hall measurement results of the fabricated GaAs/AlGaAs samples.

D-3 DC Measurements

D-3-1 Forward and reverse Schottky diode characteristics

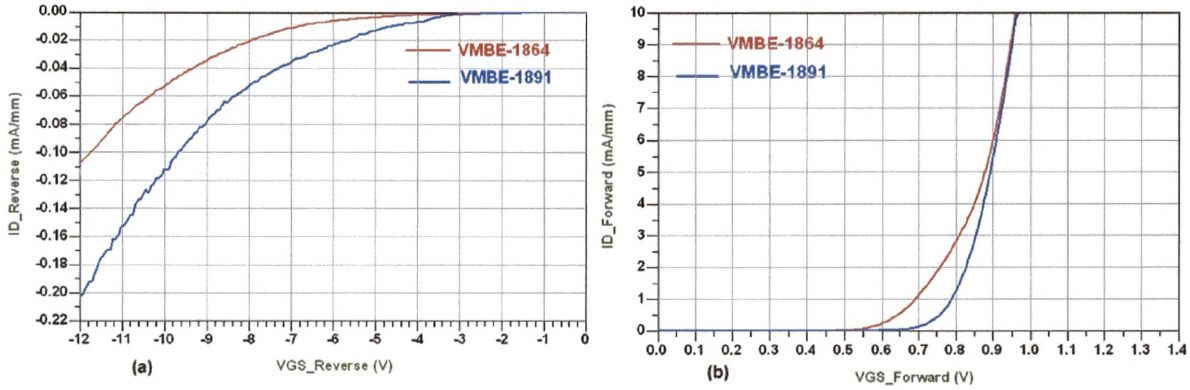


Figure D.0.1 Schottky diode characteristics of the GaAs/AlGaAs devices (a) Reverse (b) Forward.

D-3-2 On-State leakage current

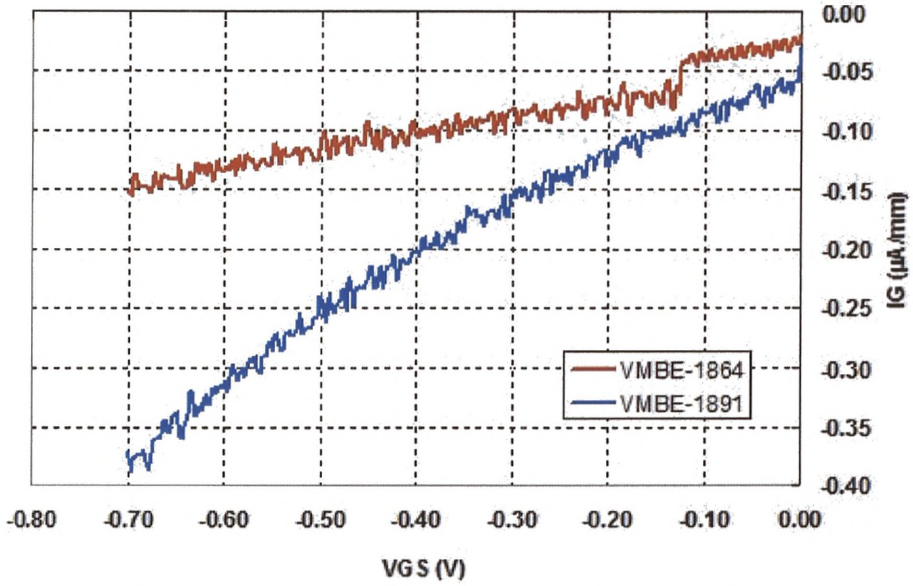


Figure D.0.2 On-state leakage current of the GaAs/AlGaAs samples at V_{DS} = 1 V.

D-3-3 Transconductance characteristics

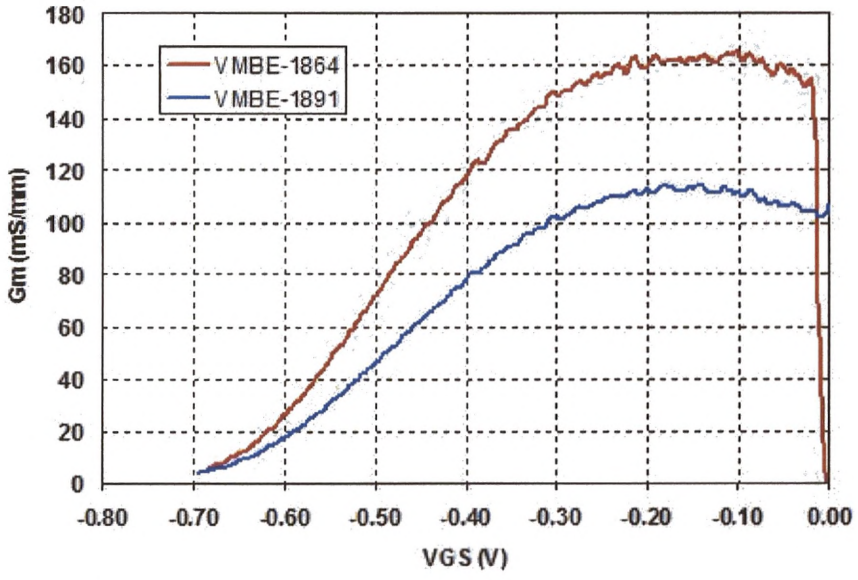


Figure D.0.3 Transconductance characteristics of the GaAs/AlGaAs samples at V_{DS} = 1 V.

D-3-4 I_D-V_{GS} characteristics

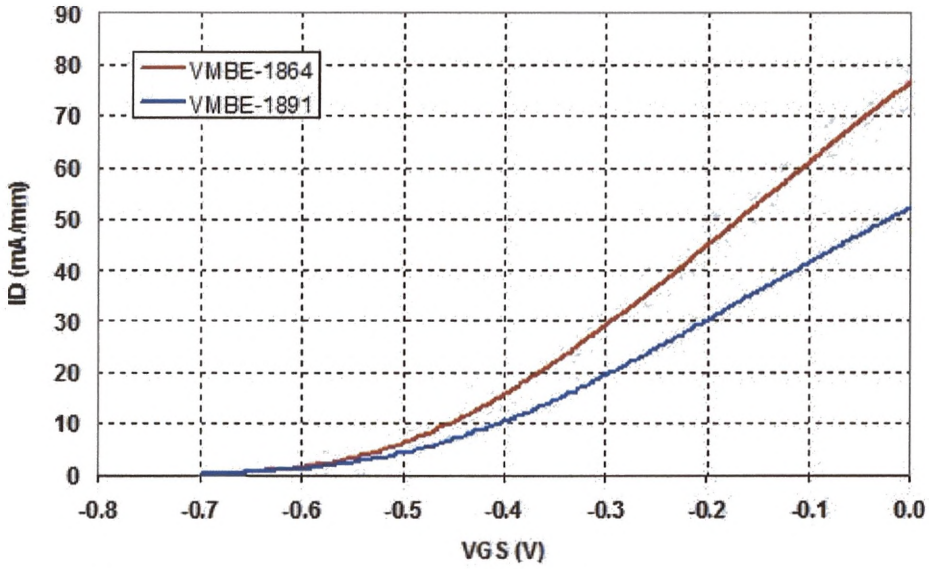


Figure D.0.4 I_D-V_{GS} curves used the extraction of V_{TH} of the GaAs/AlGaAs samples at (V_{DS} = 1 V).

D-3-5 Common-source output characteristics

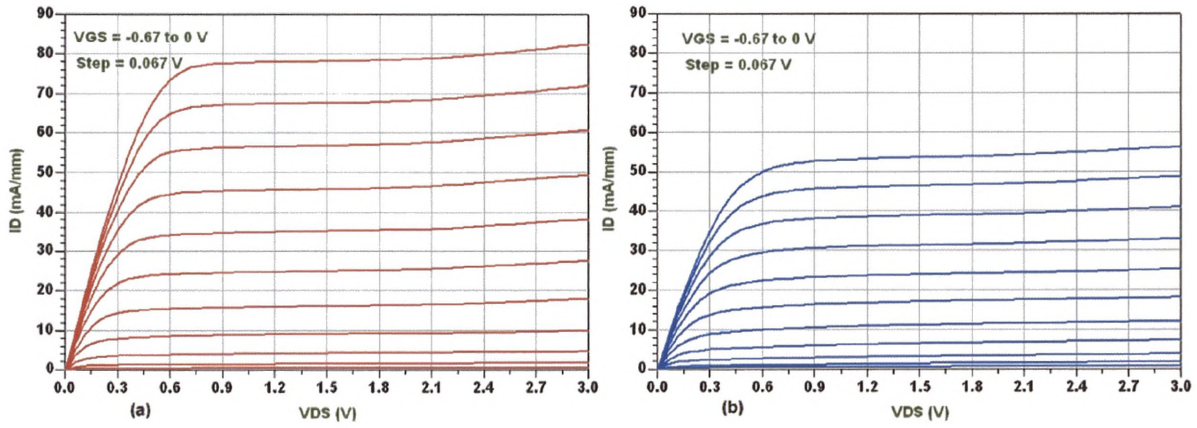


Figure D.0.5 Common source IV-curves for the GaAs/AlGaAs samples (normal size 2x100 µm) (a) VMBE-1864 (b) VMBE-1891.

D-4 RF Measurements

The unity current gain cut-off frequency, f_T, is given by H_{21} and the unity power gain maximum frequency of oscillation, f_{max}, is given by **MAG**.

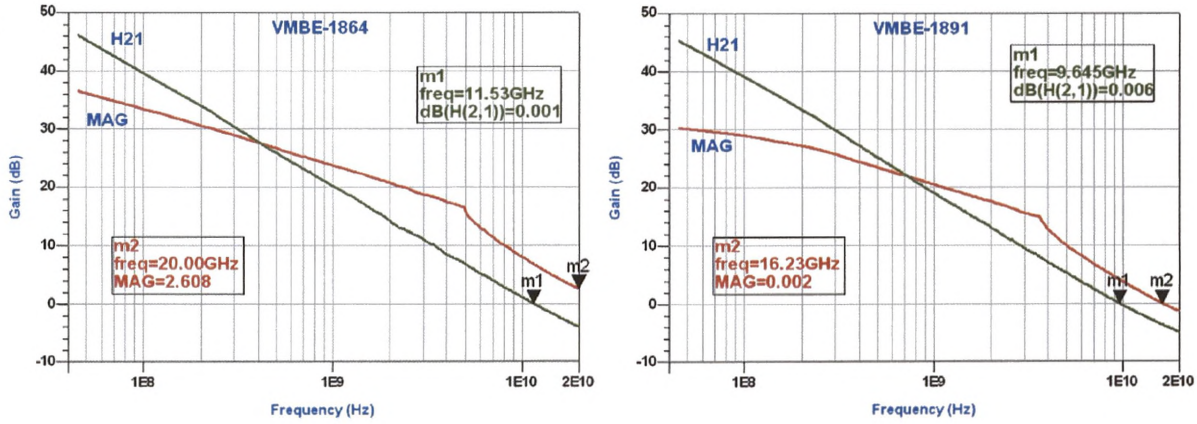


Figure D.0.6 RF characteristics of the fabricated GaAs/AlGaAs samples (device size is 2x100 μm biased for maximum G_m at V_{DS} = 1 V).

D-5 Linear Small-Signal Model Parameters

Sample →		VMBE-1864	VMBE-1891
Intrinsic Model Parameters	g_m (ms)	37	27
	T (psec)	3.65	2.5
	R_i (Ω)	9.5	9
	R_{ds} (Ω)	2250	670
	C_{gs} (pF)	0.56	0.46
	C_{ds} (pF)	0.004	0.003
	C_{gd} (pF)	0.027	0.031
Extrinsic Model Parameters	R_s (Ω)	4	8.7
	R_g (Ω)	15.5	19
	R_d (Ω)	3.8	5
	L_s (pH)	5.2	8.3
	L_g (pH)	12.8	21.1
	L_d (pH)	30.4	14.7
	C_{pg} (fF)	2	2.2
	C_{pd} (fF)	31	32

Table D.0.3 Linear small-signal model parameters for 2x100 μm devices of the GaAs/AlGaAs samples biased for maximum transconductance at 1 V drain voltage

D-6 Noise Calculations

Sample →	VMBE-1864	VMBE-1891
Bias Point	1 V, -0.2 V, 9 mA	1 V, -0.2 V, 5.88 mA
F_T (GHz)	11.5 GHz	9.65 GHz
NFmin@2GHz	1.46	1.7
R_n (Ω)	37	44

Table D.0.4 Predicted room temperature noise parameters of the GaAs/AlGaAs samples (device size 2x100 μm).

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