Feedforward Linearization of Microwave Transmitter Amplifiers

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by

K. Konstantinou

Department of Electrical Engineering and Electronics

University of Manchester Institute of Science and Technology

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Abstract

The feedforward linearization technique is assessed both theoretically and practically for use in the microwave frequency range where the limited output power of currently available devices makes linearization of power amplifiers particularly attractive. The resulting theory and design criteria developed permit the calculation of the nonlinear distortion suppression for specific circuit parameters. Nonlinear CAD techniques are employed to verify the theoretical predictions, to investigate the viability of high efficiency configurations and to compare the performance of feedforward linearization with that of conventional combining techniques.

A novel method for optimizing the performance of feedforward linearizers over a specified operating bandwidth is developed based on a single frequency excitation. The method is further developed to allow a linear approach for the design of feedforward systems permitting, thus, the use of active devices and comercial amplifier modules characterized only with small signal parameters. This method of optimization is employed in the practical set-up of the experimental linearizer and could, also, be used to allow the implementation of an adaptive feedforward system.

The feedforward linearization is practically assessed through the implementation of an experimental feedforward system and the nonlinear simulation of a CAD linearizer, both operating over the 5.9 - 6.4 GHz satellite communication band. The excellent distortion cancellation achieved with these systems indicates that feedforward linearization is a practical solution for achieving high efficiency and linearization of microwave transmitter amplifiers.

Declaration

No part of the work referred to in this thesis has been submitted in support of an application for another degree of this or any other university or other institution of learning.

Acknowledgements

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Introduction

Information handling capacity of current communication systems is limited by the nonlinearity of the output power amplifiers used in the transmitters. The nonlinearity of these amplifiers causes amplitude distortion, phase ambiguities and intermodulation noise, effecting, thus, the performance of the overall system. Modern communication systems are required to operate in multi-carrier environments carrying a large number of signals. Furthermore, spectrum being a scarce resource, there is a considerable interest in using high level digital modulation formats. In these systems the information is contained in both the amplitude and the phase of the carrier which makes these modulation schemes very efficient but, also, highly sensitive to the nonlinearities of the output power amplifier.

The most common solution to the above problems is to operate the power amplifier backed-off from saturation level by several dB, in order to keep distortion low. This approach, however, has a number of disadvantages including poor efficiency, increased running costs, high capital requirements and reduced output power and traffic handling capability. As a result, alternative configurations have been developed to improve the linearity and efficiency of power amplifiers including design techniques at device level and several techniques for the artificial linearization of amplifiers.

Improvement due to linearization can be translated either into increase in information handling capacity or into DC power saving and output power increase. Therefore, linearization can be used to improve efficiency and cost or to allow more signals to be transmitted or more efficient modulation schemes to be implemented in practice. Either way, artificial linearization offers particular advantages in millimetre wave applications, where the output power of currently available devices is limited. Irrespective of the power output levels achievable, the ever growing needs of communications systems will always demand provision of greater linearity.

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Linearization techniques have been evolving for the last two decades and some configurations have already been successfully employed in various systems. The techniques most commonly used today are RF predistortion, adaptive predistortion, feedback and feedforward linearization. RF predistortion is, currently, the only technique fully developed for microwave frequency applications. The cartesian loop, a form of the feedback method, and the adaptive predistortion are linearization techniques recently investigated for application in cellular systems. The feedforward technique has not yet been fully developed because of its increased size and the need for an auxiliary amplifier. However, the excellent distortion correction capabilities of this method make it a promising linearization technique for microwave power amplifiers competing with the well established predistortion technique. This thesis describes the results of a program of work undertaken to study and develop the feedforward technique for use in the microwave frequency range.

Chapter 1 of this thesis presents a brief review of the theory, technology and applications of microwave power amplifiers with particular emphasis on the solid state amplifier design considerations. Design procedures that are further used in the development of the feedforward linearizer are, also, included. In Chapter 2, a review of the linearization techniques most commonly used today is provided. The principle of operation, the state of the art performances and the areas of application of these techniques are discussed in detail. Furthermore, a comparative study of these techniques discusses the advantages and disadvantages of each method and highlights the potential advantages of the feedforward linearization.

The initial assessment of feedforward linearization is attempted in Chapter 3 through the simulation of a 6 GHz feedforward linearizer. Fundamental design criteria for feedforward linearizers are established based on requirements for system efficiency. A systematic and effective method of optimizing the performance of feedforward systems over a specified operating bandwidth is developed and the optimized design is, also, presented. This design is used in Chapter 4 to investigate further the potentials of

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feedforward linearization techniques and evaluate the viability of high efficiency configurations. Computer Aided Design (CAD) techniques are employed to investigate the effect of the auxiliary amplifier power rating on the performance of the linearizer and compare the feedforward amplifier with conventional combining techniques. A theoretical analysis is, also, presented to determine the effect of phase and amplitude imbalance on the distortion cancellation achieved by the feedforward system. The resulting theory and design graphs permit the calculation of the feedforward linearizer distortion suppression for specific circuit parameters.

Chapters 5 and 6 describe the design, construction and practical evaluation of the components used in the experimental feedforward linearizer. In particular, Chapter 5 includes the results for the two amplifiers and the couplers incorporated in the feedforward linearizer circuit. Chapter 6 is concerned with the evaluation of phase and amplitude control circuits for use in the feedforward system. Schiffman and quadrature phase shifters are assessed.

The design of an experimental linearizer system operating over the 5.9-6.4 GHz satellite communication band is presented in Chapter 7. A novel optimization method that allows a linear approach to the design of feedforward systems was developed and used to design the system. The final design and construction details of the linearizer are, also, included.

The practical evaluation of the experimental linearizer is presented in Chapter 8. Two and three tone tests are presented to demonstrate the improvement in the power amplifier linearity due to the linearizer circuit. Several carrier combinations are included to cover the full operating band indicating that feedforward linearization is an effective technique for improving the performance of microwave power amplifiers over wide bandwidths. Efficiency calculations are,also, presented to demonstrate the potential advantages of the feedforward linearization technique in systems where high linearity is a major concern. Overall conclusions and recommendations for further work are presented in Chapter 9.

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CHAPTER 1

The Theory, Technology and Applications of Microwave Power Amplifiers

1.1 Introduction

Power amplifiers are important components in many microwave systems. Examples include satellite, terrestrial and mobile communication systems and radars. Before the advent of the microwave transistor, power amplification in the microwave region was achieved mainly with Travelling Wave Tube Amplifiers (TWTA). The development and maturing of the microwave Gallium Arsenide Field Effect transistors (GaAs FETs) has taken place in the last two decades and Solid State Power Amplifiers (SSPAs) are now replacing the TWTAs in several applications. However, both types of power amplifiers introduce nonlinear signal distortion and, therefore, limit the performance of modern communication systems where a high degree of linearity is essential.

This chapter provides a brief background review of microwave power amplification with special emphasis on the solid state amplifier design considerations. The various figures of merit applicable to power amplifiers are defined in section 1.2. A review of microwave power amplifier types and modern microwave power transistors are given in sections 1.3 and 1.4 respectively. The problem of designing microwave power amplifiers so that the power capabilities of modern devices are fully exploited, is addressed in section 1.5. Design procedures that are further used in the development of the linearized amplifier are, also, included. Some applications for microwave amplifiers are discussed in section 1.6, including areas of application anticipated for amplifiers using the linearization technique developed in the remainder of the thesis.

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1.2 Performance parameters for Microwave Power Amplifiers

1.2.1 Amplifier Gain

There are several definitions for the gain of power amplifiers depending upon how the input and output powers are defined. The three most common definitions of power gain are given by:

$$\text{Available Power Gain} \qquad G_a = \frac{P_{ao}}{P_{as}} \qquad\qquad (1.1)$$

$$\text{Transducer Gain} \qquad G_t = \frac{P_l}{P_{as}} \qquad\qquad (1.2)$$

$$\text{Power Gain} \qquad G_p = \frac{P_l}{P_i} \qquad\qquad (1.3)$$

where P_i and P_l are the powers delivered to the amplifier input port and to the output load respectively, and P_{as} and P_{ao} are the available powers from the source and the amplifier output respectively. When the amplifier is fully matched to the source and load then, $P_i = P_{as}$ and $P_{ao} = P_l$. The transducer gain is the most useful concept, because it shows the insertion effect of the total amplifier, while the power gain and the available power gain are used in the design procedure of solid state microwave amplifiers.

In the majority of microwave systems, individual components and measurement systems have a nominal impedance, Zo, of 50 ohms at each port. If the source and load impedances are both equal to Zo then:

$$G_t = |S_{21}|^2 \qquad\qquad (1.4)$$

where $\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$ is the scattering matrix of the amplifier.

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1.2.2 Amplifier Efficiency

The RF to DC efficiency of a microwave amplifier is defined as:

$$n = \frac{P_o}{P_{DC}} \qquad (1.5)$$

where P_o is the output RF power of the amplifier and P_{DC} is the DC power consumed by the amplifier. This establishes the efficiency of the amplifier as a power converter changing DC energy into microwave RF energy.

The power-added efficiency n_{add} of an amplifier is defined as:

$$n_{add} = \frac{P_o - P_i}{P_{DC}} \qquad (1.6)$$

where P_i is the RF power input to the amplifier.

From eq.1.5 and eq.1.6:

$$n_{add} = \frac{P_o}{P_{DC}} \left(1 - \frac{1}{G}\right) = n \left(1 - \frac{1}{G}\right) \qquad (1.7)$$

where G is the gain of the amplifier. The gain of power devices is considerably limited at high frequencies and solid state amplifiers, usually, require more than one stage of amplification. The particular importance of power added efficiency is that it takes into account not only the output power but, also, the associated gain.

As the RF drive to a power amplifier is increased the RF to DC efficiency, n, and the power added efficiency, n_{add}, are increased. Thus, microwave power amplifiers, when possible, are operated at large signal conditions to improve efficiency.

1.2.3 Signal Distortion Characteristics

The analysis of the effect of the nonlinearity of microwave amplifiers is discussed in this section. This study is based on the power series analysis technique, in which the output voltage V_o of a nonlinear circuit can be described as a power series of the input voltage V_i:

$$V_o = a_1 V_i + a_2 V_i^2 + a_3 V_i^3 + a_4 V_i^4 + a_5 V_i^5 + ... \qquad (1.8)$$

The above representation assumes that the amplifier is memoryless and neglects the phase characteristics of the system. Using the above equation the most important parameters that describe the nonlinearities of power amplifiers will be discussed next, including the gain compression, the generation of higher harmonics and intermodulation products.

Gain Compression - Generation of Harmonics

If the input voltage to the microwave amplifier is a sinusoidal signal $V\cos(\omega t)$ then, from eq.1.8, the output voltage is:

$$V_o(t) = a_1 V\cos\omega t + a_2 V^2 \cos^2\omega t + a_3 V^3 \cos^3\omega t$$
$$+ a_4 V^4 \cos^4\omega t + a_5 V^5 \cos^5\omega t + ... \qquad (1.9)$$

For mild nonlinearities only the first three terms of eq.1.9 need to be considered. Application of standard trigonometric relations in eq.1.9 gives for the output voltage:

$$V_o(t) = \frac{1}{2}a_2 V^2 + (a_1 V + \frac{3}{4}a_3 V^3)\cos\omega t + \frac{1}{2}a_2 V^2 \cos 2\omega t$$
$$+ \frac{1}{4}a_3 V^3 \cos 3\omega t \qquad (1.10)$$

From the above equation it can be seen that the output signal consists of a component at the fundamental frequency ω and spurious signals at dc, the second harmonic frequency 2ω, the third harmonic frequency 3ω, etc.

The generation of higher order harmonics in power amplifiers is a serious problem in microwave transmitters because it can cause interference with other communication systems bands and it is usually reduced by appropriate filtering. Furthermore, the generation of harmonics is accompanied by a change in the amplitude of the fundamental. This phenomenon is called gain compression or gain expansion depending on the sign of the coefficients. From eq.1.10, the amplitude of the fundamental

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component of the output voltage V_{of} is:

$$V_{o\,f}(t) = (a_1 V + \frac{3}{4}a_3 V^3)\cos\omega t \qquad (1.11)$$

which is greater or smaller than the linear output $a_1 V$. Practical amplifiers are compressive, that is, $a_3 < 0$. Consequently, above a certain level of input voltage the output voltage remains the same due to the saturation of the amplifier.

The output power of microwave amplifiers is usually characterized at the 1 dB compression point, shown in Fig.1.1. The 1 dB compression point is defined as the signal level where the gain of the amplifier at the fundamental frequency is reduced by 1 dB compared to the small signal gain:

$$G_{1dB} = G_o - 1 \text{ dB} \qquad (1.12)$$

where G_o is the linear small signal gain in dB, defined as $G_o = 20 \log a_1$.

Intermodulation distortion

If the input signal consists of two sinusoids equal in amplitude, but at two different frequencies ω_1 and ω_2, then, from eq.1.8, the output voltage is:

$$
\begin{aligned}
V_o(t) = {} & a_1 V(\cos\omega_1 t + \cos\omega_2 t) + a_2 V^2(\cos\omega_1 t + \cos\omega_2 t)^2 \\
& + a_3 V^3(\cos\omega_1 t + \cos\omega_2 t)^3 + a_4 V^4(\cos\omega_1 t + \cos\omega_2 t)^4 \\
& + a_5 V^5(\cos\omega_1 + \cos\omega_2 t)^5 + \dots
\end{aligned}
\qquad (1.13)
$$

Expansion of the above equation and application of standard trigonometric properties shows that, in addition to generating the harmonic components of each signal, intermodulation products (IM) are also produced at the following frequencies:

$(\omega_1 +/- \omega_2)$	2nd order
$(2\omega_1 +/- \omega_2)$, $(2\omega_2 +/- \omega_1)$	3rd order
$(3\omega_1 +/- \omega_2)$, $(3\omega_2 +/- \omega_1)$, $(2\omega_1 +/- 2\omega_2)$	4th order
$(3\omega_1 +/- 2\omega_2)$, $(3\omega_2 +/- 2\omega_1)$, $(4\omega_1 +/- \omega_2)$, $(4\omega_2 +/- \omega_1)$	5th order

The most significant of the these intermodulation products are the 3rd and 5th order IM at frequencies $(2\omega_1-\omega_2)$, $(2\omega_2-\omega_1)$, $(3\omega_1-2\omega_2)$ and $(3\omega_2-2\omega_1)$, because they fall within the operating bandwidth and cannot be filtered out. In several communication systems, especially in multi-carrier ones, intermodulation distortion is required to be at least 60 dB lower than the carrier power level. In these cases, a useful figure of merit of the amplifier's linearity is the carrier to intermodulation product power ratio (C/I).
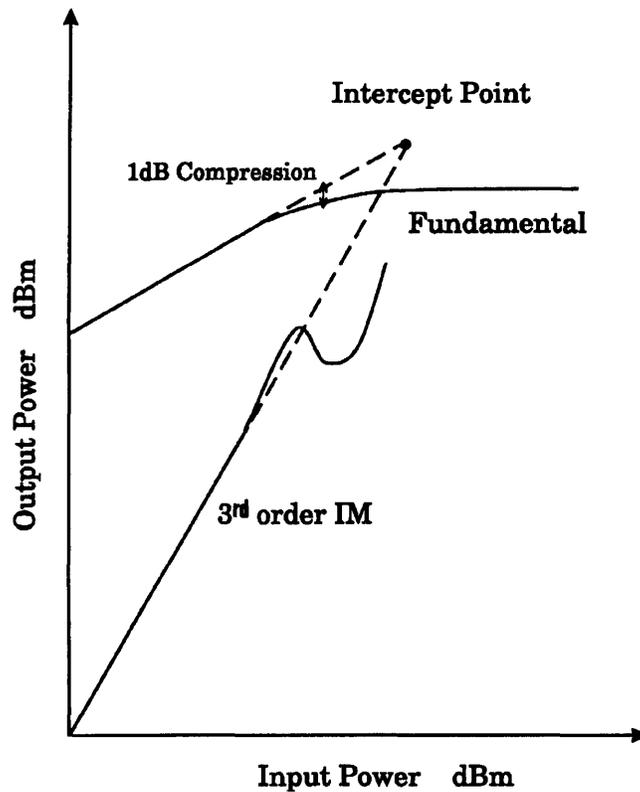
Fig.1.1 Amplitude characteristics of amplifier

The amplitude of a particular distortion product will not only depend on the amplifier's nonlinear characteristics, which are represented by the coefficients, but also on the input signal amplitude V. Specifically, n^{th} order products vary as V^n. If this distortion product is plotted against the input signal amplitude V in a dB scale, the nth order product will show a slope of n times the unity slope of the fundamental signal. Therefore, the 3rd order intermodulation products should follow a line with a slope 3:1, the fundamental

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being a line with slope 1:1, as shown in Fig.1.1. Nevertheless, at higher input power levels the IM_3 curve clearly deviates from the 3:1 line and as the amplifier goes into compression region it can perform some anomalous dips and peaks. The reason for this behaviour is that the 3:1 slope is followed precisely only for third order products which arise from the third order term of eq.1.13. If this equation is expanded, it can be seen that the third order IM products have contributions from higher order terms as well. At low signal levels the higher order contributions are insignificant and the third order IM distortion appears to have a 3:1 slope. At higher power levels, depending on the nonlinear characteristics of the amplifier, they may start to dominate the lower order products and result in the behaviour shown in Fig.1.1. This figure describes the behaviour of a typical solid state amplifier where, near compression, 3rd order IM products are reduced because 5th order IM products rise significantly. From that point of view, solid state amplifiers are considered to be fifth order nonlinear systems in contrast to travelling wave tube amplifiers which are third order systems.

A useful measure of the nonlinearity of an amplifier is the intercept point because it is independent of the input power. It is defined as the output power P_i at which the output power P_{IMn} of the nth order distortion product would intercept the output power P_o of the fundamental signal, if low level results were extrapolated into the large signal region. The third order intercept point is shown in Fig.1.1. In systems with bandwidth more than one octave, where second order intermodulation products and harmonics may fall within the band, the second order intercept point is, also, of significance.

It can be shown that for weak nonlinearities, i.e. signal output power levels away from the 1 dB compression point, the power of the third intermodulation product, for two equal amplitude tone excitation, is[1]:

$$P_{IM_3} \approx 3P_o - 2P_{I_3} \qquad dBm \qquad (1.14)$$

where P_o is the power of the fundamental signals at the output and P_{I3} the intercept point of the amplifier in dB.

Phase Distortion

In nonlinear systems variation in the amplitude of the input signal affects both the amplitude and the phase of the system transmission coefficient. This form of phase distortion is called AM to PM conversion and may have serious consequences in phase modulated communication systems. From eq.1.11 the output voltage V_{of} at the fundamental frequency ω in a nonlinear circuit is the sum of first and third order components of the input voltage at the same frequency. These components are not necessarily in phase. This possibility is not considered in eq.1.11, because the equations so far presented describe only memoryless systems. It is, however, possible for a phase difference to exist between these components. The response of the nonlinear circuit at the fundamental frequency is, then, the vector sum of two phasors:

$$V_{of}(t) = \left(a_1 V + \frac{3}{4} a_3 V^3 \, e^{j\theta} \right) \cos \omega t \qquad (1.15)$$

where θ is the phase difference. Even if θ remains constant with amplitude, the phase of V_{of} changes with variations of the input voltage amplitude V because the higher order terms become more significant when the power level increases. Consequently, the AM to PM conversion will be most serious as the circuit is driven into saturation.

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1.3 Review of Microwave Power Amplifiers Technologies

Travelling Wave Tube Amplifiers (TWTAs) and Solid State Power Amplifiers (SSPAs) are the two types of devices most commonly used for power amplification in microwave frequencies. TWTAs were first developed and exclusively used until recent advances in microwave transistors enabled SSPAs to replace tube amplifiers in several applications. Both TWTAs and SSPAs are briefly reviewed in the next sections and their advantages and disadvantages are discussed.

1.3.1 Travelling Wave Tube Amplifiers

Travelling Wave Tube Amplifiers (TWTA) are still widely used in microwave applications mainly because of their large power handling capabilities and wide bandwidth. Their principle of operation is based on the interaction of the input electromagnetic wave with an electron beam, while they are both travelling at approximately equal speed in the tube. The schematic diagram of a helix TWTA is shown in Fig.1.2.
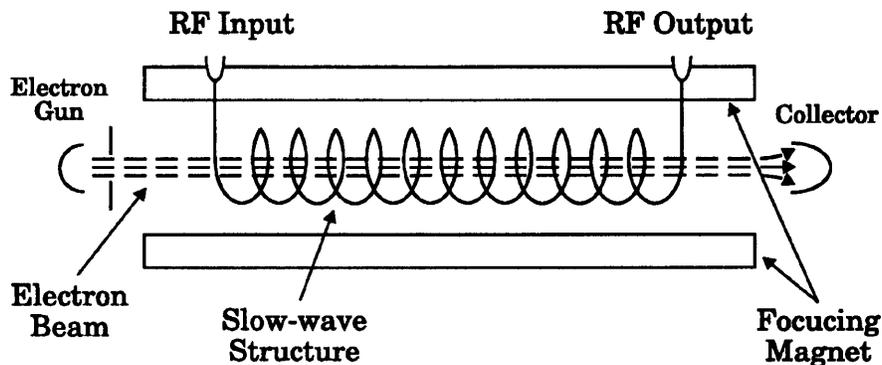
Fig.1.2 Travelling Wave Tube Amplifier

The TWTA consists of an electron beam and a slow wave structure. The electric field is focused by a constant magnetic field along the electron beam and the helical slow wave structure. The applied signal propagates around the turns of the helix and produces an electric field at the centre of the helix directed along the helix axis. When the

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electrons enter the helix tube, an interaction takes place between the moving axial electric field and the moving electrons and on the average, the electrons transfer energy to the microwave signal on the helix, amplifying this way the input signal wave. The first helix TWTA was invented in 1944 by Kompfner[2]. Typical values for commercially available TWTAs performance are: frequency range tens of GHz, bandwidth up to one octave, gain up to 60 dB, 20-40% efficiency and up to 10 kW average power.

Microwave TWTAs are usually bulky and heavy since they handle output power up to hundreds of kW. Metal parts are employed for appropriate heat conduction and heavy permanent magnets are often necessary because their effect on the electron beam is the principle of operation. Also, much space and weight is occupied by built-in power supplies that must deliver both high voltage (tens of kV) and current (tens of Amps), which are extremely difficult to regulate. Their major advantage is their ability to operate over wide bandwidth at frequencies up to tens of GHz and to produce very high output power. These characteristics, often, make them the only choice for several systems. In communication systems, however, extremely high power levels are not required and the development of amplifiers, for systems on satellites and at earth stations, is concentrated on the specific problems of reduction of operating voltages, minimization of weight and dimensions of the tubes and their power supplies. Recent developments in Russia are focused in multiple beam technologies leading to efficiency improvement by a factor of 1.5, lowering of supply voltage by one tenth with consequent reduction in volume as well[3]. Mini TWTAs at Ku band have been reported [4], employing a new collector principle to achieve 40% reduction in volume. These TWTAs provide 40 W output power over 12 - 12.5 GHz and were developed for user satellite communication earth stations in time domain multiple access systems.

1.3.2 Solid State Power Amplifiers

During recent years microwave transistors have shown considerable improvements with regard to output power, efficiency and bandwidth. Consequently, transistor power

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amplifiers have been developed extensively and are now used in number of applications. The research in the field is continuing and improved performances are, constantly, being reported for Solid State Power Amplifiers (SSPA). Pulsed output power 12 kW over 2.7 - 2.9 GHz[5], 200 W pulsed output power at 5 GHz across a 40 MHz bandwidth[6], 30 W over 14 - 14.5 GHz[7], and 5.5 W at 20 GHz with 500 MHz bandwidth[8] are reported to have been achieved. The DC to RF efficiency of SSPAs ranges from 16% to 26% and bandwidths are typically of the order of 5-10%. A important advantage of SSPAs is the potential for integration of several amplifiers and other required circuitry on a single semiconductor chip, in what has become known as MMIC (Monolithic Microwave Integrated Circuit) technology. Although MMIC amplifiers are, still, restricted to few watts of output power, they achieve bandwidths of more than an octave. Enhanced power performances are expected to be achieved in the near future. MMIC amplifiers are, also, compact and complete units and can be incorporated in conventional microstrip MIC (Microwave Integrated Circuits) to produce higher output power.

Due to power limitations of active devices at microwave frequencies, SSPAs are usually designed by power combining several power transistors. The disadvantage of this approach is the loss through the combiners and dividers, but it offers the advantage of continuing operation even in the case of some devices failure. In general, SSPAs exhibit high reliability with typical Mean Time to Failure (MTTF) of the order of 10^5 hours of operation which compares very favourably to the MTTF of 10^4 that TWTAs achieve[9]. Solid state amplifiers are the main competitors for the TWTAs and in many systems they have successfully replaced tube amplifiers. The main advantages SSPAs offer are small size and weight, low supply voltages, high reliability and improved linearity. Compared to TWTAs they exhibit much lower amplitude and phase distortion as shown in Fig.1.3, which illustrates the performance for an SSPA and a TWTA of the same power capabilities[10]. The higher linearity of SSPAs allows them to operate nearer to their saturation point and, therefore, enhanced efficiency can be achieved. Their main constrains are, limited output power and/or relative narrow bandwidth at high frequencies.

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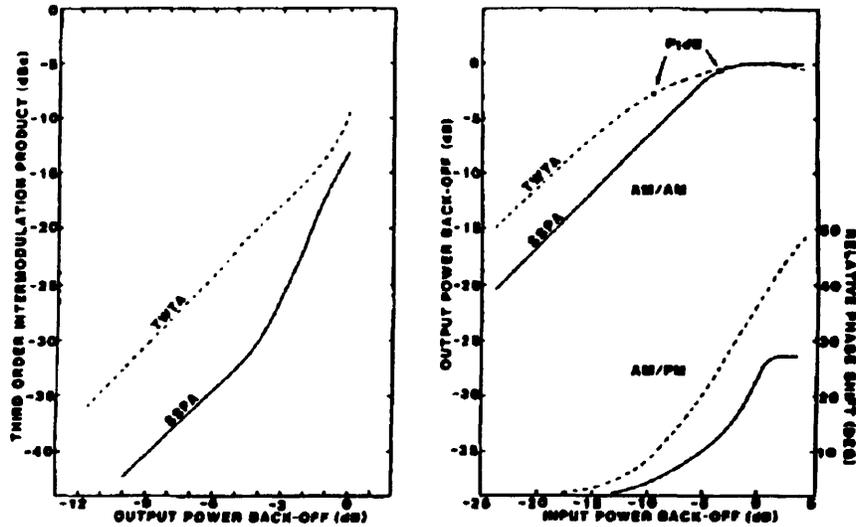
Fig.1.3   Linearity characteristics of TWTA and SSPA [10] (a) 3rd order IM and
(b) Amplitude and Phase Characteristics.

1.4 Review of Modern Microwave Power Transistors

Experimental GaAS FETs were first made in the early 1970s, and rapid development throughout the 1970s and 1980s led to the commercial availability of power devices, capable of amplification into the mm-wave region. GaAs MESFETs are microwave devices fully mature today and widely developed for power by all the companies. The structure of a typical device is shown in Fig.1.4. A fuller acronym for the device is MESFET, for MEtal Semiconductor Field Effect Transistor. The junction between the gate metal and the n-type semiconductor material is a Schottky junction. This causes a charge depletion layer to form in the semiconductor material. The thickness of the depletion layer varies with the applied negative bias between the gate and the source terminals. As more negative bias is applied to the gate, the depletion layer becomes thicker, so that the conducting channel between the drain and the source becomes thinner and the current from drain to source is reduced for a given drain voltage. This basic principle of operation was first described by Shockley in 1952 [11]. The power

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capabilities of the device are limited by the approximate power-frequency squared limit for microwave transistors derived by Johnson [12]:

$$Pf^2 \approx \left(\frac{E_c \upsilon_s}{2\pi}\right)^2 \frac{1}{X_c}$$

(1.16)

where E_c is the effective electric field before avalanche breakdown, υ_s is the drift velocity of carriers and X_c is the device impedance level. The above equation holds for any transistor and shows that once the material and the geometry of the device have been determined the available output power is proportional to the reciprocal of the square of the frequency.
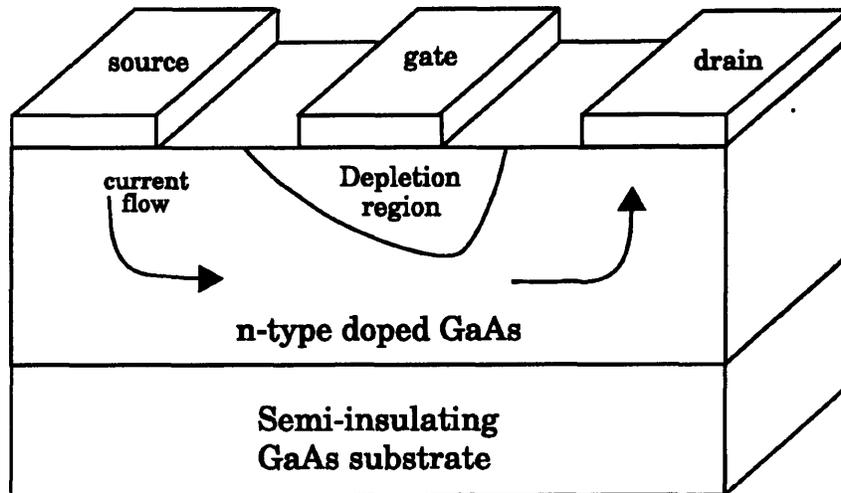
Fig.1.4 Basic GaAs FET structure

In high power FETs there are a number of critical properties including output power, gain, efficiency and linearity for which it is necessary to increase breakdown voltage, decrease thermal resistance, increase drain current and improve gate-drain cross-section structure. Unfortunately, some of the above parameters are interrelated and optimization of FETs for high power generally implies a subtle trade-off between several factors. One of the most important design factors in the microwave FETs is the determination of the gate length because it has the greatest effect on the cut off frequency. It

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determines the time required for the electrons to pass under the gate (given the electron velocity in the GaAS semiconductor) and designers of microwave FETs have constantly striven for shorter gate lengths. Nevertheless, with extremely short gate lengths the gate resistance increases and the output power and gain decreases. Typical values for gate lengths are of the order of few μm[9].

Two fundamental limits for the power capabilities of MESFETs are the drain current and the gate drain breakdown voltage. Higher drain currents can be achieved by increasing the width of the MESFET's gate. As a result, the power capabilities of FETs are often described in terms of power density watt/mm, output power over gate width. However, increasing the gate width, increases, as well, many device parasitics, especially the gate-source capacitance and the gate resistance and as a result reduces the gain of the device[13]. Consequently, power MESFETs usually have relative low gain.

The gate drain breakdown voltage of a power device can be maximized by optimizing the ohmic contact, by using a recessed-gate structure[9] and wide gate drain spacing. Increased gate drain spacing, however, increases the drain series resistance and, as result, it can significantly reduce the output power and the efficiency.

Output power is increased by combing the operation of several individual transistors mounted in a single chip. High power FETs normally use a comb-shaped gate electrode alignment. The gate and drain connections can be made without difficulty but the source electrodes require bridging. This is done by dielectric or air bridges, or by plated via holes connecting each source electrode through the substrate to a common source connection. In general, power FETs are composed by a number of cells and are much wider than small signal chips. The total gate width of the device is the sum of the gate widths of all cell-FETs used. Major problems in the design of the overall chip are the temperature conduction, the difficulty to feed large devices uniformly in phase and amplitude, and the decrease of the output impedance due to the paralleling of the transistors. The low output impedance of power FETs results in serious matching difficulties especially over wide bandwidth. In order to limit matching losses

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manufacturers now, commonly offer packaged devices using one or several internally matched chips. These internally matched power GaAs FETs have 50 Ω bandwidths of the order of 0.5-1 GHz, centred at various communication bands.

A recent development in the design of field effect transistors for microwave frequencies was the development of the HEMT (High Electron Mobility Transistor), sometimes called the heterojunction FET or the MODFET (MOdulation Doped FET). The basic structure of a GaAlAs HEMT is shown in Fig.1.5.
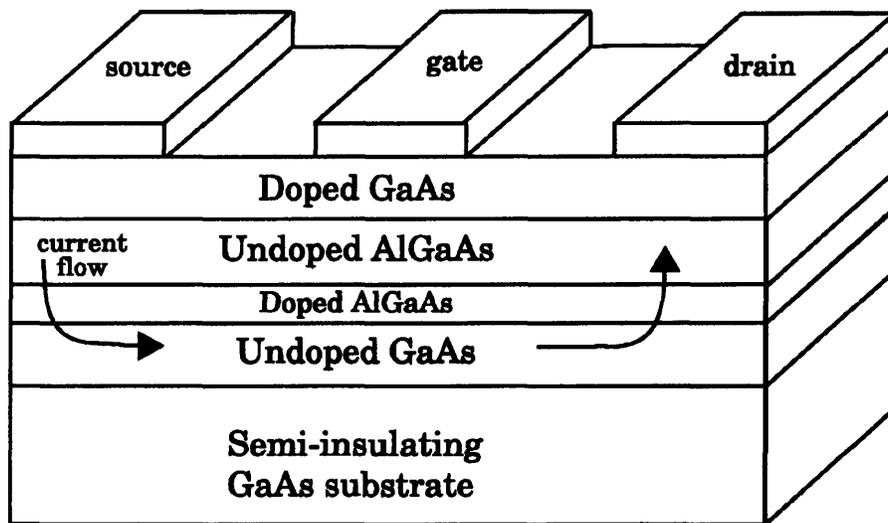
Fig.1.5 Basic HEMT structure

As with the conventional GaAs FET, when a positive voltage is applied between the drain and source electrodes of a HEMT, a current flows due to impurities intentionally added to certain semiconductor layers. This current can be modulated by varying the voltage applied between the gate and the source, as with the GaAs FET. The improved performance offered by the HEMT stems from the difference in the material within drain to source current flows. In the GaAs FET the current flows in the doped GaAs channel between the drain and the source. However, in the HEMTs a two dimensional electron gas resides in the intrinsic GaAs layer, due to AlGaAS/GaAs heterojunction energy gaps, and, hence, current flows due to these electrons. Since the electrons are in the undoped

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GaAs, well away from the ion impurities that act as donors, ionized impurity scattering is greatly reduced when compared to the conventional GaAs FET and the electrons move with higher mobility and velocity. The possibility of high electron mobility in a heterojunction structure was first shown by Dingle et al in 1978 [14] and it soon became clear that devices of this type were potentially superior to GaAs FETs as microwave transistors.

Microwave HEMTs are, today, in widespread use as low noise elements, the first commercial products having started to appear since 1985. However, their high gain affords outstanding characteristics in high frequency applications, and they are being developed for high power applications. Power HEMTs for microwave application were reported in 1987, with 1 W output power at 30 GHz[15]. Today, the double heterojunction pseudomorphic HEMT is a very popular and efficient structure in experimental stages[16]. A MMIC amplifier employing these devices has been reported to produce 7 W at 16 GHz, with 4.5 dB associated gain and 30.8% power added efficiency[17].

The current state of the art for power FETs in terms of maximum output power delivered by a single chip is shown in Fig.1.6 [18]. It can be sheen that this quantity is quickly reduced as the frequency increases, as expected from eq.1.16. Up to 6 GHz few tens of watts can be generated from power FETs having total gate widths of several tens of mm. From 6 GHz to about 20 GHz, output powers between 10 W and 5 W are achieved from devices with gate width of the order of 10 mm. From 20 GHz to 60 GHz, FETs with gate width of about 1 mm produce less than 1 W, while at higher frequencies only tenths of a Watt can be provided with gate widths of few tenths of mm.

A very important advantage of microwave FET transistors is the potential of integration of several devices or MMICs along with their lumped or distributed circuit elements in a single semiconductor chip. Internally matched power FETs are effectively MMIC structures. The use of MMIC technology can involve some compromise because the

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opportunity to adjust the output matching circuit to compensate for device to device variations is not available. However, MMIC technology is increasingly popular,because it has the potential of high volume production and, therefore, low cost products[19].
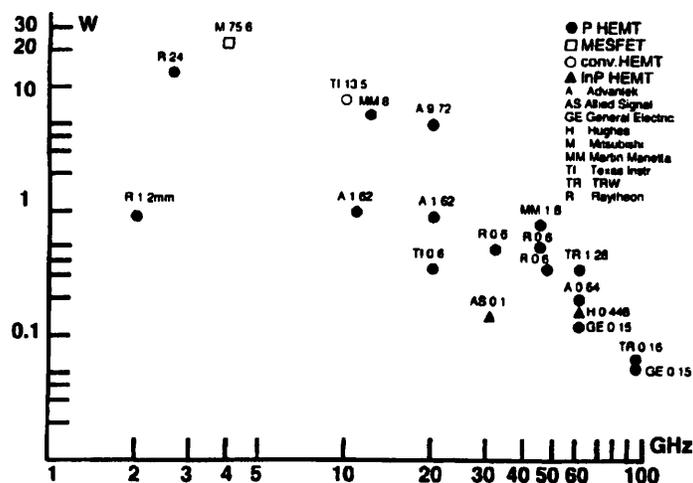
Fig.1.6 State of the art for single FET device output power[18]. Numbers correspond total gate width

Although FETs have so far dominated in microwave power applications, the most promising microwave power transistor today is the HBT (Heterojunction Bipolar Transistor)[20]. The basic structure of this device is shown in Fig.1.7. Silicon bipolar transistors have always been high power devices, but restrained to low frequencies due to the poor performance of the material at frequencies above 4 GHz. The heterojunction structure made it possible to reduce the base resistance and emitter capacitance, thus, enabling the use of GaAs which has superior high frequency properties. Unlike the FET, in which the current flows across the semiconductor surface, the bipolar transistor has a current that flows vertically from the surface to the chip. This gives the device considerable current driving capabilities and makes them especially suitable for power applications. The HBTs have high power density operation, giving smaller chip size, higher breakdown voltage, higher impedance values for a given output power level, very

low leakage current and small knee voltage. The output power performance of the HBT is limited more by thermal considerations than by electrical ones [21]. A recent and impressive demonstration of power MMIC HBT technology has been given by Khatibzadeh et al[22]. They produced a two stage amplifier with output power over 11.5 W, 10.5 dB associated gain and more than 34% power added efficiency over 5% bandwidth around 9.2 GHz. Although HBTs are not yet commercially available, they are currently considered as replacements for FETs in the next generation of solid state power amplifiers.
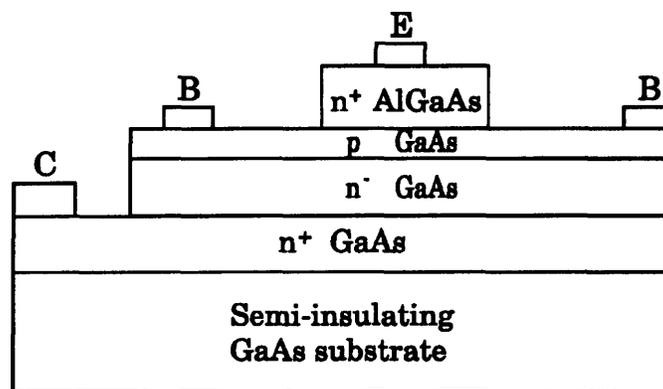
Fig.1.7 Basic HBT structure

1.5 Design Aspects of Microwave Solid State Power Amplifiers

The design of a microwave transistor amplifier involves selecting the appropriate generator and load reflection coefficients and designing the input and output matching networks to present those reflection coefficients to the transistor. The device is treated in the design process as a two port circuit and is described by a set of two port S parameters. Since the S parameters vary with bias conditions, they must be measured at the bias voltages at which the device will be operated. Usually, they are measured in the common source configuration because it provides the most stable arrangement. The selection of the load and source impedances presented to the device depends on the

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desired gain, output power, bandwidth, gain flatness and efficiency. The final design is, usually, a trade off between these parameters. In the next sections, the fundamental considerations and concepts of microwave amplifiers design will be discussed, with particular emphasis on high linearity and output power operation. Methods to determine the optimum design parameters for best power performance are, also, reviewed.

GaAs FET and HEMTs devices can be incorporated into a variety of different circuit structures. Again, as stated earlier, the type of structure chosen for a particular application depends upon the precise requirements of gain, output power, bandwidth, match and linearity. The most common configuration for power amplifiers is reactive matching with optimum loading and its advantages and disadvantages are discussed here in detail. The circuit topology for the balanced amplifier is, also, briefly reviewed, along with basic power combining techniques and design considerations with regard to power amplification.

1.5.1 Fundamental Considerations for Microwave Amplifier Design

The most important consideration in designing a microwave amplifier is stability. The amplifier should be stable not only within the frequency range of operation, but, also, out of band and for terminations deviating from 50 Ω. The conditions sufficient and necessary for unconditional stability with any passive load and source impedance is that the stability factor K is greater than 1 and the magnitude of the determinant of the S parameter matrix, Δ, is less than 1 [1]. If either of these conditions is not met then the device is conditionally stable. The stability factor K is determined by the S parameters of the transistor:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{1.17}$$

and the determinant, Δ, of the S parameter matrix is:

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \qquad (1.18)$$

If the device is unconditionally stable and maximum gain is desired the input and output networks are designed for simultaneous conjugate match. This maximizes the transducer gain defined in eq.1.2. The solution is well defined and equations that describe the required generator and load impedances as a function of the S parameters of the transistor are provided in the literature[1][23].

If the device is only conditionally stable it is necessary to determine the input and output impedances which provide stable operation. Stability circles can be drawn on the Smith chart to determine the areas of load and source impedances which, when presented to the transistor can cause oscillation. The stability circle on the load plane has centre C_L and radius r_L given by[1]:

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \qquad (1.19)$$

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \qquad (1.20)$$

If this circle is plotted on the Smith chart all the values of the load impedances that make the input reflection coefficient $\Gamma_{in}=1$ are determined. The circle represents the boundary. To find whether the inside or outside of the stability circle represents the stable region a known impedance has to be considered. The characteristic impedance Z_o of the S parameter measurement system can be used. For $Z_L=Z_o$ the corresponding input impedance is $Z_{in}=S_{11}$. Usually $Z_o=50\ \Omega$ and, if the normalizing impedance of the Smith chart is also 50 Ω, Z_o should be represented by the centre of the Smith chart. Then, the region that includes the centre of the chart represents the stable region of Γ_L if $|S_{11}| < 1$, or the unstable region if $|S_{11}| > 1$.

Similarly, the stability circle of the source has a centre C_s and radius r_s given by[1]:

$$C_s = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \qquad (1.21)$$

$$r_s = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \qquad (1.22)$$

If a device is conditionally stable then a conjugate match can not be achieved. In this case, a load or source reflection coefficient is chosen and the second matching network is designed to conjugate match the other port of the transistor to the source or the load respectively. There are, also, situations where a conjugate match is not desired because one of the transistor ports is preferred to be terminated by a specific impedance. This is the case in low noise amplifiers where the input matching circuit is designed to provide the minimum noise figure. When high power performance is the aim of the design, the output matching network should present to the device the load impedance for optimum output power. Once the output or input matching network has been selected, the other matching network is usually designed to conjugate match the reflection coefficient at the input or output port of the device respectively.

An amplifier having one conjugate-matched port can be designed by employing the concepts of available and power gain G_a and G_p defined in eq.1.1 and eq.1.3 respectively. If the output impedance is selected first, and the input of the device is conjugated matched, then $G_p = G_t$ where G_t is the transducer gain, i.e. the overall gain of the amplifier. In this case the problem reduces to finding the values of the load reflection coefficients Γ_L that provide the desired G_p and at the same time enable the FET to achieve the optimum output power performance and operate at the stable region. The loci of the Γ_L that give constant power gain are circles on the Smith chart and their centre and radius are given by[13]:

$$C_p = \frac{g_p(S_{22} - \Delta\, S_{11}^*)}{1 + g_p(|S_{22}|^2 - |\Delta|^2)} \qquad (1.23)$$

$$r_p = \frac{(1 - 2Kg_p|S_{12}S_{21}| + g_p^2|S_{12}S_{21}|^2)^{\frac{1}{2}}}{1 + g_p(|S_{22}|^2 - |\Delta|^2)} \qquad (1.24)$$

where K is defined in eq.1.17 and $g_p = G_p / |S_{21}|^2$.

When more than one stage is required to produce the desired gain, the interstage networks are designed to match the input port of the one transistor to the output port of the other. Compromises in designing the interstage networks may be necessary if broadband operation is desired, where a deliberate mismatch can be introduced in order to achieve the desired gain flatness over the required bandwidth.

1.5.2 Biasing Point and Class of Operation Considerations

The biasing voltages for the active device used in a microwave amplifier depend on the requirements of the specific design. Fig.1.8 shows the current and voltage bias points selected for various applications. The highest gain under small signal conditions is obtained at point D, where the drain current I_{ds} is high and V_{ds} is maintained between 3-4 Volts to avoid thermal problems. The best linearity for high power operation is obtained at point A by biasing the transistor at $I_{ds}/2$ and $V_{dsmax}/2$, where V_{dsmax} is the maximum excursion along the drain source voltage axis compatible with safe linear operation. In modern power devices the biasing drain voltage V_{dss} corresponding to $V_{dsmax}/2$ is typically 10 V. An amplifier operating at these bias conditions is called class A amplifier.

In class A operation, the maximum efficiency is, in theory, 50%. This is for an ideal voltage or current gain device that is linear in the first quadrant of the I-V plane with the bias point at $I_{dss}/2$ and $V_{dsmax}/2$ and the dynamic load line, corresponding to a load

resistance R_l, set to $45°$. Under these conditions the peak to peak signal voltage and signal current swings become I_{dss} and V_{dsmax} respectively. The maximum RF to DC efficiency is, then:

$$n_{max} = \frac{P_{omax}}{P_{DC}} = \frac{\dfrac{I_{dss}V_{dsmax}}{4}}{P_{DC}} = \frac{1}{2} = 50\% \tag{1.25}$$

In practice, it is not possible to vary the voltage from zero to $V_{dsmax}/2$ because of the knee at the uppermost I-V curve. Also the current cannot be varied between $I_{dss}/2$ and 0 V because of the leakage current, I_m, limitation. Thus, in practice, the obtainable RF to DC efficiency is less than 50%. Commercially available FETs have efficiencies of about 25% for class A operation and amplifiers with more than one stage will, consequently, achieve efficiencies less than that. Another disadvantage of class A amplifiers is the dissipation of great amount of heat especially when no RF input signal is applied in which case all the DC power is dissipated as heat.
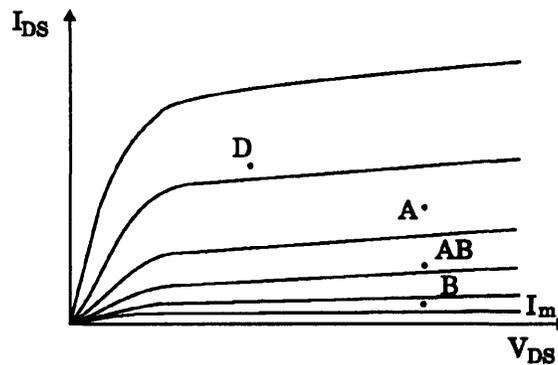
Fig.1.8 I-V characteristics and points of operation

Many of the disadvantages of class A operation can be overcome with class B operation, represented by point B in Fig.1.8. In class B operation the transistor is biased approximately at the cut off point so that the device is on only at one cycle of the signal.

The theoretical efficiency for class B operation with sinusoidal signals is 78.5% [13] and in practice, efficiencies of the order of 70% have been achieved with experimental devices[24]. Class B operation has the disadvantages of inherent low gain and the deterioration of the transistors linearity because the half-wave rectified sinusoid output signal has high harmonic distortion. The low gain and high nonlinearity problems of class B operation can be partially overcome by biasing the device for class AB operation, Fig.1.8, which is effectively a compromise between class A and class B. In class C, where the device is biased beyond pinch-off, even higher efficiencies can be achieved at the expense of even lower gain and increased nonlinearity. Typical values for the power level of the third order intermodulation products in C class amplifiers are 15 dBc[25]. A further disadvantage of any class of operation other than A, is that the small signal S parameters, with which the manufacturers usually characterize their devices, are no longer meaningful so that the appropriate nonlinear FET models have to be used in the design of class B or class C amplifiers.

1.5.3 Reactive Matching with Optimum Loading

In the design of reactively matched power amplifiers the most important consideration is to determine the output reflection coefficient required to achieve the desired output power performance. For class A operation the small signal S parameters are only a rough approximation of the large signal performance and the optimum large signal generator and load impedance must be measured at each frequency of operation. These parameters resemble $S_{11}*$ and $S_{22}*$, but usually the output Γ_{Lopt} is significantly changed from $S_{22}*$[26-27], as seen in Fig.1.9[26]. From measurements, S_{11} is found to be virtually independent of the input power[27]. Therefore, the output power performance of the amplifier will mostly depend on the load reflection coefficient, hence, the output power is load-pulled. The contours of constant output power can be plotted on the Smith chart for the load and generator impedances to determine the effect of non-optimum match.
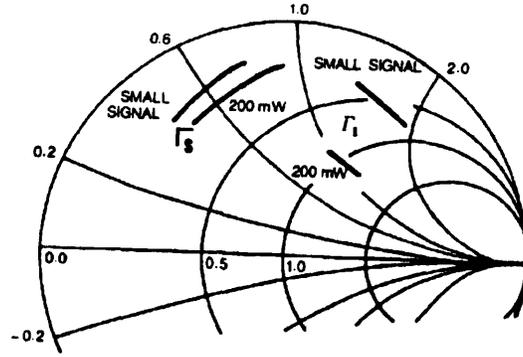
Fig.1.9 Variation of optimum loads Γ_s and Γ_l with signal level[26]

Thus, the problem of designing an amplifier for high power and linearity reduces to developing a matching network which will present the optimum load reflection coefficient to the output of the active device. The small signal gain and stability are considered according to eq.1.17-1.24. For narrow band designs, the matching network can be designed with simple low loss microstrip transmission line circuits, using series line sections and open or short circuited stubs or quarter wavelength impedance transformers. For broader bandwidth designs, it is necessary to design a transforming network which follows Γ_{Lopt} as closely as possible over the required frequency range and remains within the desired power contour. Methods for achieving this using filter synthesis techniques have been discussed extensively in the literature[1][23][26].

The required input matching network can be determined by calculating the input reflection coefficient Γ_{in} of the transistor when its output is terminated by a load with reflection coefficient Γ_{Lopt}, as seen in Fig.1.10, provided that stability is, also, ensured. This reflection coefficient is given by:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_{Lopt}}{1-S_{22}\Gamma_{Lopt}} \qquad (1.26)$$

In a similar manner to the output match design procedure, for a narrow operating band, a simple matching network can be designed to present the conjugate of Γ_{in} to the input port of the transistor, whilst for a broader bandwidth design it is necessary to design the network to present a reflection coefficient as close as possible to the calculated Γ_{in} over the required operating band.
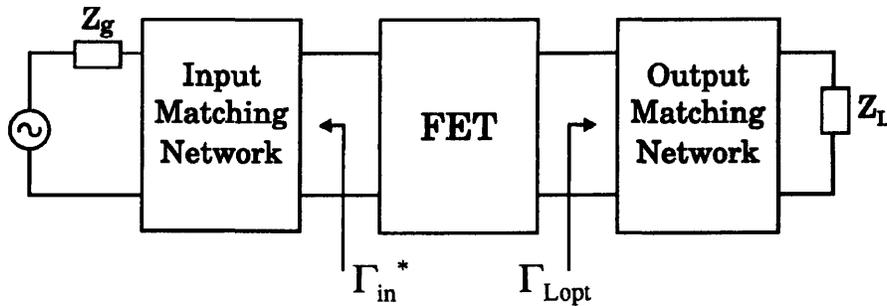
Fig.1.10 Reactive matching with optimum loading

A problem with this design approach is that the resulting small signal output return loss of the finished amplifier will be poor, because the output circuit has been designed for the optimum power load and not for a conjugate match. Since no gain shaping and impedance matching can be accomplished with the output matching network, the input reflection coefficient will also be poor. The above problems may be solved by the use of low loss ferrite isolators or by employing a balanced amplifier configuration. The use of input and output isolators is an attractive solution which has been adopted in many commercial amplifiers. The main disadvantages of this approach, however, are added size, weight and expense involved, and the fact that such elements are not compatible with MMIC technology.

1.5.4 Load-Pull Measurements

Load-pull is the only practical method to measure those terminal impedances which, when applied to an active device, enable it to have particular linear or nonlinear characteristics. The block diagram of a load-pull test set-up for measuring the large

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signal load corresponding to a power FET performance, is shown in Fig.1.11.
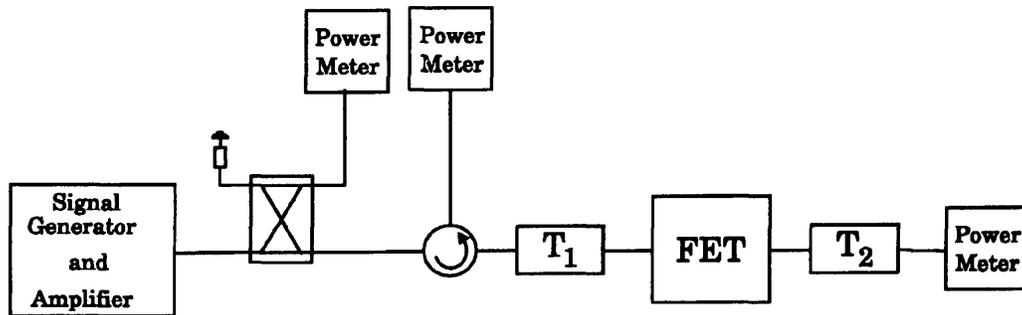
Fig.1.11 Block diagram of load-pull technique

At a fixed frequency and input power level, the input tuner T_1 is adjusted for optimum return loss and the output tuner T_2 is adjusted for the desired output power performance. The output reflection coefficient is then measured, giving the output load that corresponds to the specific power gain performance for the device under test, at a given frequency. Computer controlled tuners can be used to characterize the device for the required range of frequencies and power levels[28].

The load impedance can be either supplied passively with a mechanical tuner, as in Fig.1.11, or actively, by injecting a signal which can vary in amplitude and phase into the output of the device, so that the device is terminated with a virtual load. This signal must be coherent with the drive signal and the active load-pull method is typically implemented by splitting the input signal and feeding it forward to the output port [27][29]. The active load pull method offers the advantage of being able to simulate any load. Due to losses inherent in passive tuners, very high or very low impedances are difficult to be obtained. Hence, the evaluation of very large power FETs which require low impedances, is not practical, with the passive load-pull method.

Intermodulation distortion can, also, be measured as a function of output power load-pull [30][31]. In these measurements two signals are amplified independently to avoid

generating intermodulation products and fed via the input tuner into the FET. A computer driven output tuner is then used to generate the various constant output power and constant C/I contours on the Smith Chart. The output tuner is either pre-characterized or measured. A unique output impedance which allows maximum output power to be obtained for a given C/I requirement can, then, be defined for a given frequency, input power level and bias point.

The main disadvantage of load pull technique is that it requires numerous measurements made at discrete frequencies, power levels and bias conditions. As a result, the method is either tedious if manual or a significant investment if automated. Nevertheless, this technique has the advantage that the FET is operated under conditions simulating actual circuit performance, and when dealing with new and yet unmodelled devices or investigating performance sensitivity to impedance mismatches, it is the most convincing evidence for amplifier impedance related behaviour.

1.5.5 Theoretical Prediction of Power Contours

A simple and elegant derivation of the load pull contours of power FETs was proposed by Cripps [32]. From measurements on medium power transistors, Cripps observed that the output load required for maximum saturation power is very nearly the same as the load required either for optimum 1 dB compression power or maximum linear power. Therefore, the method he developed was based on the primary limitations to output power, namely limitations on the RF voltage and current swing. From the I-V characteristics of a typical device, Fig.1.12, it can be seen that for maximum linear power the load must be resistive and is given by:

$$R_{Lopt} = \frac{V_{DSS}}{\frac{1}{2}I_{DSS}}$$

(1.27)

The above equation is used as a design parameter in low frequency linear amplifiers but, at microwave frequencies, device and package parasitics distort that simple model.

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Cripps experimentally showed that, provided the drain capacitance is de-embedded as a part of the external output load, the optimum load impedance is still resistive and close to the value given by eq.1.27.
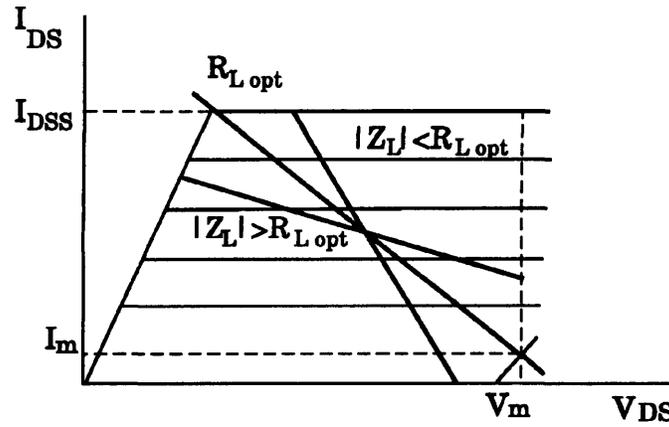
Fig.1.12 Current and voltage limitations for various load lines

Cripps[32] proposed that in order to obtain constant output power contours it is sufficient to consider two cases: $|Z_L| < R_{Lopt}$ when the output power is current limited and $|Z_L| > R_{Lopt}$ when the output power is voltage limited, as shown of Fig.1.12. If $Z_L = R_L + jX_L$ and $|Z_L| < R_{Lopt}$ the maximum value of X_L is given by:

$$|X_L|^2 \leq (R_{Lopt}^2 - R_L^2) \qquad (1.28)$$

If $|Z_L| > R_{Lopt}$ and $1/Z_L = Y_L = G_L + jB_L$, the maximum value of B_L is given by:

$$|B_L|^2 \leq (G_{Lopt}^2 - G_L^2) \qquad (1.29)$$

The ellipsoidal power contours can be obtained by following constant resistance contours on the Smith chart for X_L, (eq.1.28) and constant admittance contours for B_L (eq.1.29) within the bounds fixed for X_L and B_L respectively. Then, the drain capacitance and bond wire inductance parasitics, which are obtained from small signal measurements, are added.

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Cripps produced elliptic curves for the -1 dB and -2 dB power contours for the 1 W GaAs FET F2710, as shown in Fig.1.13[32]. Comparison of the predicted and measured output load-pull contours showed that this theory is in good agreement with experimental measurements.

Fig.1.13 Power contours generated with Cripps' method[32](- -predicted, —measured)

Although the above analysis is only an approximation based on linear circuit concepts, it is a simple and rapid technique and valuable when nonlinear data or load pull measurements are not available. Based on Cripps technique simple mathematical expressions can also be incorporated into CAD programs and allow optimization of microwave amplifier design directly orientated towards the power performance of the device [33].

1.5.6 Power Combining Techniques

When the required output power exceeds device capabilities two or more FETs are combined to achieve the desired power performance. The structure of two power combined FET amplifiers is called balanced amplifier and is shown in Fig.1.14.

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Fig.1.14 Balanced amplifier

In a balanced amplifier, the input signal is fed into one port of a 3 dB coupler. The outputs from the direct and the coupled ports are equal in magnitude and differ in phase by 90°. These signals are fed into identical amplifier stages, and the outputs are recombined in a second 3 dB hybrid coupler. At the output port of the second coupler, the outputs of the two amplifiers add in phase, whereas at the port which is terminated in a resistive load, the outputs interfere destructively. Similarly, reflected power from the inputs of the two amplifiers cancel at the balanced amplifier input port, and add in phase at the load port of the first coupler. Thus, as long as the two transistors and their matching circuits are identical, a good match is achieved over the bandwidth of the couplers.

Practical balanced amplifiers are typically built in microstrip. Two kinds of 3 dB couplers can be fabricated conveniently in this medium, the Lange coupler [34] and the branch line coupler [35]. Lange couplers can be designed to cover bandwidth approaching two octaves. Branch line couplers are simpler to fabricate, because they do not need bond wire interconnections and so fine microstrip lines, but they occupy more circuit area and are narrower in bandwidth. A two branch line coupler has a bandwidth of around 5-10%, three branch couplers cover approximately 20% and some more complicated designs[36] provide up to 50% bandwidth.

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Balanced amplifier stages have been popular as cascadable general purpose gain elements. The good return loss that they offer is ideal in MMIC amplifier technology, where ferrite isolators cannot be used.

When more than two amplifiers are combined, more complicated N-way networks are used, in which power can be fed to and recovered from N number of transistors. These structures must have low transmission loss, good isolation between device ports and, for very high power applications, sufficiently dispersed structure to avoid excessive heat accumulation. Since these networks are reciprocal, the same network can be used either as power combiner or a power divider, and usually identical but reversed structures are used at amplifier input and output ports to produce the identical phase and amplitude transmission for each of the N paths. An advantage of power combined amplifier structures is that failure of one or more amplifier modules does not result in total failure of the combined power amplifier. This property is called graceful degradation. A further advantage of power combining amplifiers is the potential to suppress higher order harmonics introduced by the nonlinearity of the amplifiers, by arranging the phase difference of these harmonics to be $180°$[13] Although this is not easily provided by any kind of combiner/divider structure, implementation of this concept for multi-port amplifiers in multi-carrier systems has been reported to decrease the number of intermodulation products in each channel[37].

A corporate structure for combining power amplifiers is shown in Fig.1.15. The number of devices combined in this structure is binary and the principal elements used to realize such a tree network can be branch line couplers, Lange couplers or Wilkinson combiners/dividers [38]. Compared to Wilkinson structures, quadrature hybrids have the advantage of the excellent matching conditions that are typical of balanced amplifiers.
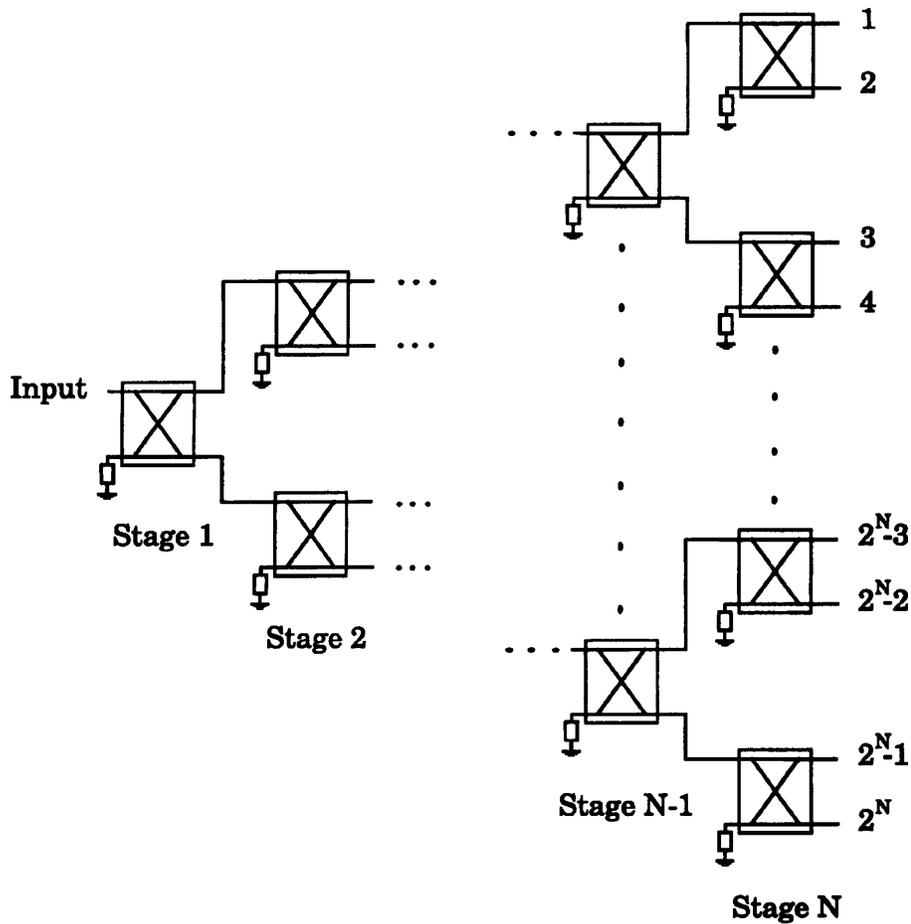
Fig.1.15 Corporate combiner

Fig.1.16 shows a chain or serial combiner. Each successive stage of the N-stage combiner adds 1/N of the power delivered to the output. The advantage of this structure is that the amplifier stages need not be combined in binary units. This form of coupling offers, also, the advantages of good isolation between amplifiers and good return loss but is difficult to obtain the range of fine increase in coupling ratio that is required. They are, therefore, difficult to fabricate in microstrip because some coupling ratios are too weak for branch line hybrids and too strong for directional couplers. In the travelling wave combiner these problems have been solved by the use of a distributed split-tee structure [39].
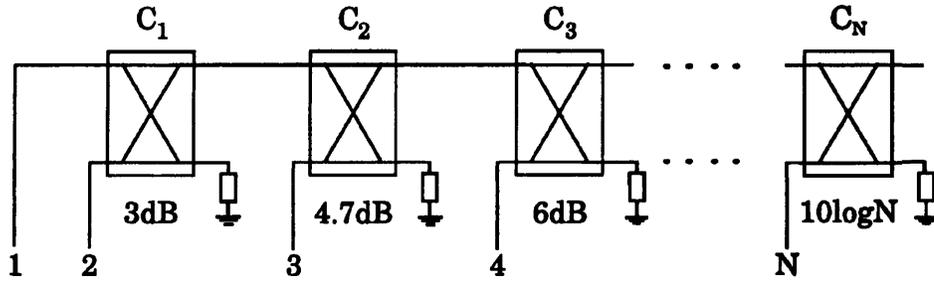
Fig.1.16 Serial combiner

As the number of devices to be combined increases, the transmission loss through a corporate structure increases and lowers its efficiency. The main advantage N-way combiners offer is that they allow large numbers of devices to be connected with minimal loss. Generally, three types of N-way combiners/dividers, the Wilkinson, radial and planar are used to combine large number of amplifier modules. Wilkinson and radial can only implemented in three dimensions for N>2 [38][40] and the planar structure is designed to operate in microstrip achieving good isolation and efficiency of about 78-90% [41-42]. For high output power performance, waveguide power combiners/dividers have, also, been developed[43].

1.6 Applications of Microwave Solid State Power Amplifiers

A power amplifier is used at the output stage of the transmitter in a microwave system in order to produce the required signal power. Traditionally, the tube amplifiers were used for power amplification in microwave frequencies, but the advantages in the power capabilities of modern transistors have led to replacement of TWTAs by SSPAs. In the early 80s[44] the potential of using SSPAs in downlink commercial communications satellites started to be considered because of the advantages SSPAs offer, as mentioned earlier in section 1.3.2.

Ever since several SSPAs have been developed for satellite communication systems for both on board and earth stations[45-47][7-8]. Output powers of the order of 10 W have been produced up to the 12 GHz band with efficiencies of 17% to 26% [45-47] and 5.5 W have been achieved over the 19.7-20.2 GHz band with 17% efficiency[8]. Important design considerations for these amplifiers intended for space use, are temperature stability, high linearity and reliability since these have to be designed for the 10 year operating life of modern satellites. Most of them have gain compensating circuits for temperature changes so that operating temperature ranges of 0-60° are usual[46] and some employ linearizers to improve linearity and efficiency[8][46].

Design criteria are not so strict for earth stations with regard to size and weight, although the low operating voltages, low cost and high reliability of FETs along with the graceful degradation property of SSPAs are advantages that lead to TWTAs replacements. Local gain adjustment along with power supply, temperature and amplifier monitoring and over-temperature shut down protection are usually provided in the SSPAs designs. Efficiency is, also, a very important consideration and for satellite communication systems earth stations that stay idle for significant percentage of their operating time, a burst mode technique has been developed[48]. The amplifier is switched off and on synchronously with the burst carriers in order to improve the efficiency of class A operation. A further advantage of SSPAs is their prominent linearity that allows them to be operated nearer to saturation. This enables SSPAs with lower output power capabilities than TWTAs to be used, like in [7] where 30 W SSPAs have been developed to replace 50 W TWTAs in satellite uplink transmitter applications at 14 GHz.

Another area of application of SSPAs is in terrestrial telecommunications, where large operators are responsible for the provision of national and international links. They apply usually TWTA technology which demands high levels of maintenance. The use of SSPAs allows the increase in smaller unmanned repeater facilities and low cost private links in the business community. In line of sight telephone and television links, 10-25 W

SSPAs subsystems with external gain adjustment and temperature compensation have already been installed to replace TWTAs.

In military mobile communications, SSPAs are used because of their low mass, ruggedness, reliability and high efficiency. Transmission is usually of short duration to avoid detection and conserve power and SSPA instantaneous switch on is of great benefit. With portable systems, efficiency is a major parameter for enhanced battery conservation. One example of the advantages of the use of SSPAs is the man-portable transponder developed for the army Special Operations Forces which uses an X-band solid state transmitter[49]. The unit is compact, capable of 26 W peak output power, with an associated gain of 37 dB, DC to RF efficiency of 15% and is operating from a +/-12 V battery over the temperature range -50° to 50°.

An other area of application for SSPAs is the active phase array antennae, which are commonly used in the Very Small Aperture Terminals (VSAT) and in mobile satellite services. Array transmission elements are typically of small power, 2-3 Watts, and SSPAs with good modular gain and phase tracking, high linearity and efficiency are required[46]. One further advantage of the use of SSPAs in such systems is the potential of integration of GaAs FETs hybrid power modules with attenuators and phase shifters in MMIC form for beam synthesis together with DC control circuits which provides substantial savings in size and mass[47]. Military systems take advantage of the use of SSPAs to produce high capability radars like the Counter Battery Radar system[50], which uses active antennae containing approximately 3000 transmit/receive compact modules, employing MMIC high power amplifiers in the transmitter part.

At low frequencies where FETs are capable of few tens of watts very high output powers can be delivered by SSPAs. These amplifiers are finding increase use in radar systems because of their enhanced reliability. A solid state transmitter already in full scale production for surveillance and air traffic control radar, has been reported to deliver 12 KW output power over the 2.7-2.9 GHz band[5].

Solid state microwave amplifiers have in the last decade made impressive advances and are currently being used in several communication and radar systems. One of their major advantages is their enhanced linearity which allows them to operate at high levels of their output power characteristics resulting in more efficient systems. Nevertheless, SSPAs are often operated several dB away from their saturation, because in modern communication systems a very high degree of linearity is, usually, required. This problem will be addressed in the next chapter together with a detailed review and discussion of the most commonly used linearization techniques today.

CHAPTER 2

Linearization of Microwave Power Amplifiers

2.1 Introduction

Information handling capacity of current communication systems is limited by the nonlinear behaviour of the output power amplifiers. These nonlinearities, as discussed in the previous chapter, have distortion effects such as gain compression, AM to PM conversion and generation of harmonics and intermodulation products. These degrading parameters cause amplitude distortion and phase ambiguities in travelling signals as well as intermodulation noise and can significantly affect the performance of the communication system. In multi-carrier systems, nonlinear behaviour of power amplifiers gives rise to intermodulation between the carriers in different frequency channels. Odd order intermodulation products can have frequencies within the adjacent channels, causing distortion of the wanted signals. In single carrier system configurations, the modulated band-limited carrier, when passed through the power amplifier, can suffer regrowth of the higher order modulation sidebands, which may overlap with adjacent channels and, therefore, cause interference with other transmitters in the same system architecture.

The most common solution for the above problems is to use an amplifier with a very high output power rating and operate it in the linear region, well below saturation. This approach, however, has a number of disadvantages, including increased running costs, poor efficiency, high capital requirements and reduced output power and traffic handling capability. As a result, several alternative configurations have been developed to artificially linearize power amplifiers and some of them have already been successfully

employed in various systems. Nevertheless, the ever growing demand for communication systems is continuously forcing advanced modulation schemes and more carriers to be transmitted simultaneously so that the need for even higher linearity is always in demand.

Linearization techniques have been evolving for the last two decades, with different configurations being developed and old ones adapting to the requirements of modern communication systems. This chapter provides a brief discussion of the systems where linearizers are currently employed or will possibly be in the future, followed by a review of the techniques most commonly used today. These include the RF predistortion, adaptive predistortion, feedback and feedforward linearization. The principle of operation, the advantages and disadvantages and the state of the art performances of these linearization techniques are discussed in detail. Comparison of these techniques highlights the potential advantages of the feedforward method which is further examined and developed in the subsequent chapters of this thesis.

2.2 Linearized Amplifiers in Microwave Communication Systems

The first linearizers were developed for analogue communication systems employing SSB AM modulation. Linearity requirements for such systems demand carrier to third order intermodulation product power ratios (C/I) of at least 50 dB for two tone measurements[51] or even 95 dB for three tone measurements in some cases[52]. The consequent output power back-off required to achieve this highly linear performance was estimated to be 6 - 10 dB below the saturation level[53]. As a result, feedforward, RF predistortion and feedback circuits have been developed to linearize power amplifiers for microwave radio links[52][54] and satellite communication systems[51][53][55] employing SSB AM modulation. Improvements of 8 - 9 dB in the amount of output power back off with the use of a linearizer have been reported[53-54].

The rapid development of communication systems in the last decade has led to new

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forms of modulation and changes in traffic handling, creating, thus, a demand for systems with even greater linearity. Modern communication systems are required to operate in multi-carrier environments carrying a large number of signals. Furthermore, spectrum being a scarce resource, there is considerable interest in using high level digital modulation schemes such as multilevel quadrature modulation formats. In these systems the information is contained in both the amplitude and the phase of the carrier which makes these modulation methods very efficient but, also, highly sensitive to the nonlinearities of the output power amplifier.

An area where obtaining more bits per hertz has become a major concern is digital microwave radio systems. Multilevel modulation schemes such as 16 QAM digital radio transmission systems have, already, been implemented[56] and higher schemes such as 64 QAM and 256 have, also, been investigated[57-58]. These systems require extremely linear transmitters and operation of the power amplifier in the linear region implies such large amounts of output power back off that it, often, makes this approach impractical. For the experimental systems described in [58] the required output power back off for the desired system performance was 6, 10, 13 and 15 dB for single carrier 16, 64, 256 and 1024 QAM systems respectively. Furthermore, a dramatic increase in the required output power back off was predicted for larger number of carriers[58]. Consequently, several linearizers, mainly predistortion, have been developed for high capacity digital radio link systems over the last 10 years[57][59-61].

Another area where linearization of power amplifiers could be advantageous is satellite communication systems. In the past, the bulk of satellite transmission have been single carrier TV or telephone signals[62]. Digital compression now allows several TV signals to be transmitted in the frequency space previously occupied by a single signal. Multiple signal services such as VSATs or mobile communication systems for both military and commercial applications are altering traditional satellite loading. These changes have created a necessity for satellite transponders and earth stations that can carry multi-carrier traffic and multi-level modulated signals more efficiently. Operating the power amplifier in low output signal levels is a severe penalty especially in satellite

transponders and artificial linearization has been a popular approach for satellite communication systems[62-69]. Today, several solid state power amplifiers intended for on board satellite communication applications include linearizers[8][46]. Without linearization, the RF power efficiency and the thermal design considerations of the satellite become complex with significant drawbacks in terms of mass, volume and fuel. Electrical power produced by the solar generators is limited and, as a consequent, the complete satellite concept is largely determined by the output power and efficiency of the power amplifier. Earth stations requirements for weight and power consumption are not so strict. Nevertheless, power efficiency, small volume and low cost are always significant design considerations.

The output power levels of modern active devices encourages the development of communication satellite transponders using active array antennae, where a large number of amplifiers is necessary. These modules must have low mass and volume, while maintaining the required efficiency and linearity over their whole dynamic range. In particular, gain and phase characteristics of these amplifiers should track over the signal dynamic range in order to preserve antenna radiation pattern. Linearized microwave amplifiers have, recently, been developed for active array antennae applications, employing both RF predistortion and feedforward techniques[46][70].

The development of mobile communications such as cellular systems has, over the last few years, created a demand for highly linear transmitters. Some of these systems employ multi-level modulation schemes like the north America cellular telephony service which uses $\pi/4$ DQPSK[71]. Continuing pressure for efficient use of the limited available spectrum is forcing the development of such modulating schemes and, also, imposes the need for little spacing between adjacent channels. In such systems the out-of-band transmission should be 60 - 70 dB below the carrier level[71-74] to prevent channel interference. In order to meet these strict requirements the adaptive predistortion technique[71-72][75-78] and the feedback cartesian loop method[79-81] have, recently, been developed to linearize the transmitters of such systems. Although these

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linearization techniques are restricted to single channel narrow band systems, they are particularly suitable for the current generation of cellular systems which rely on single channel amplification and multiple input power combination to achieve the required number of channels from the base station[73-74]. Nevertheless, this approach has the disadvantages of excessive overall size and significant power loss in the output combiner. The use of a broadband linearized amplifier would allow a large number of channels to be amplified simultaneously. Broadband linearization techniques such as feedforward are, therefore, possible candidates for personal mobile communication systems in the future[82-85].

2.3 Review of Linearization Techniques

2.3.1 RF Predistortion

Predistortion linearizers compensate for the distortion of power amplifiers by generating the inverse amplitude transfer function and the opposite sign phase shift of the amplifier to be linearized. An ideal linearizer's expansion transfer function and negative phase shift are shown in Fig.2.1, along with amplitude and phase transfer functions for a power amplifier. The resulting transfer function of the series connected devices will be an amplitude linear function and the resulting phase shift will be zero for the whole dynamic range of the linearized amplifier.
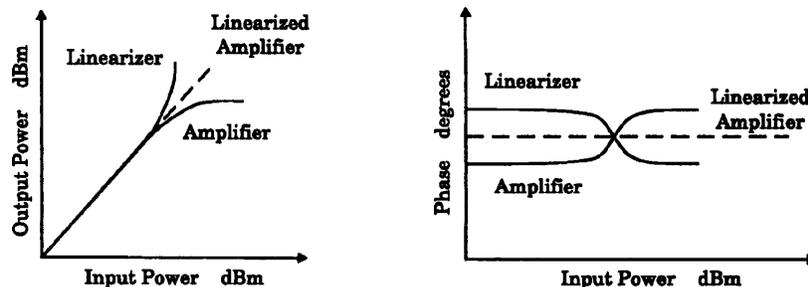
Fig.2.1 Principle of operation of a predistortion linearizer

A general block diagram of a transmission type predistortion linearizer circuit is shown in Fig.2.2, where the input signal is divided into two paths: one is the linear route and the other is the distortion route. The operation of the predistortion linearizer is based on the vectorial addition of the outputs of each path, the resulting output voltage V_{out} , of the linearizer being:

$$V_{out} = V_1 + V_2 \tag{2.1}$$

The voltages V_1 and V_2 are the outputs of nonlinear devices and, therefore, depend on the input power level. By properly adjusting the loss of the attenuators and the phase shift in each arm, as well as the bias of the nonlinear devices, the output voltage can show the desired amplitude expansion and phase lead with respect to input voltage.
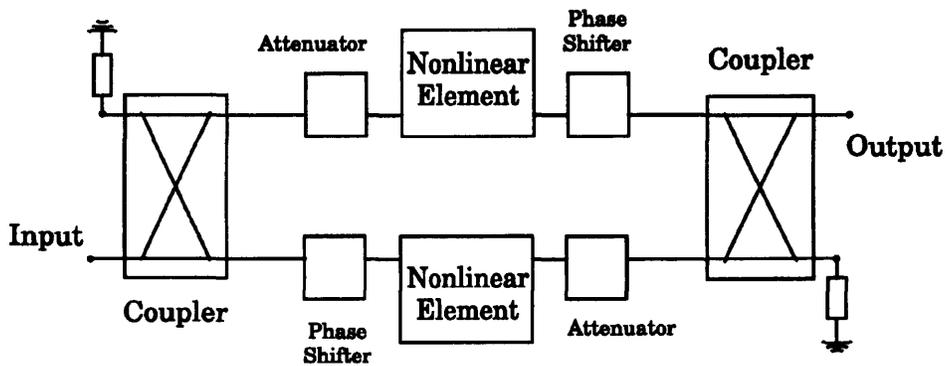
Fig.2.2 Block diagram of transmission type predistortion linearizer

Fig.2.3 shows the vectorial addition of the voltages in the linear and the distorted path. For small signal level, the gain of the linear and the distorted path are constant and no predistortion is generated. When the input power increases to a higher level, the gain of the distortion route is compressed and the output voltage becomes V_{out}', where the amplitude expansion and phase shift has been generated.

A wide range of different types of nonlinear behaviour can be generated from this circuit by selecting the phase shift and/or the attenuation in each arm, using active devices in one or both arms and the appropriate choice of devices, the circuit configuration and the

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bias of the active devices. A variety of the above combinations has been reported in the literature[57][64-66][86].Another configuration is a reflection type predistorter in which only one coupler is used with the isolated port being the output. One of the reflection paths includes a distortion generator which, when the input signal level increases, changes the amplitude and/or phase of the reflected signal[67].
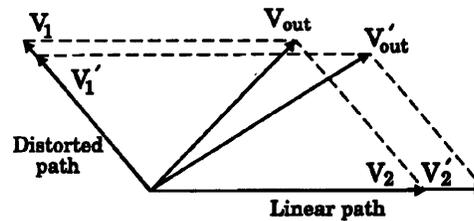
Fig.2.3 Vector diagram of linearizer

Schottky barrier diodes are very popular active devices as distortion generators for predistortion linearizers[57][64-67][86] because of their fast response and low power consumption. Usually two diodes are used in only the distortion path, in an antiparallel arrangement connected in shunt and operating as gain compressors or expanders by increasing the signal that they reflect.

Distortion generators have also been implemented using single[8][46][52][60-61][67] or dual[68] gate FETs in transmission configuration linearizers. Single stage GaAs FET amplifiers [46][60] and an antiparallel connected transistor pair[52] have been used as distortion generators in only one path of the linearizer. Dual gate FETs have also been used in both arms of the predistortion linearizer exploiting the gain expansion properties of the devices when biased near pinch off[68]. Single gate FETs act as again expanders as well, when biased near pinch off, and have been used in conjunction with phase shifters to compensate for amplitude and phase distortion in power amplifiers[8][61]. Recently, a MMIC predistorter has been reported employing a single gate FET in the common gate configuration[63].

Predistortion has been a popular linearization method throughout the 80s and early 90s and it has been implemented to linearize both SSPAs[8][46][59-61] and TWTAs[52][63-68][86]. Predistortion linearization improves the amplitude and phase nonlinearity of the power amplifier and as a result the intermodulation products are

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suppressed as well. The amount of intermodulation suppression depends on the desired bandwidth of linearization and it is improved with increased output power back-off from saturation. Improvements in the 3rd order intermodulation distortion ranging from 7 dB to 18 dB have been reported for bandwidths of 200 - 500 GHz and output power back-off of 4 - 12 dB [57][60][66][68]. The above performances are maintained over 3 - 12 dB input power dynamic range of the amplifier. An impressive demonstration of wide band operation is the MMIC predistortion linearizer described in [63] which achieved nearly 10 dB improvement over 10.7 - 12.7 GHz and dynamic range 2 - 8 dB back off from saturation.

Predistortion linearizers are installed at the input of power amplifiers and, since they are adjusted for a specific condition of amplifier operation, they do not compensate for any changes in the characteristics of either the amplifier or the components included in the linearizer. Such variations can occur due to changes in time, temperature or operating level. The usual approach to ensure good performance over a wide temperature range is to characterize and, then, temperature compensate the amplifier and the linearizer by using a temperature sensor to adjust the control voltages of the phase shifters and attenuators included in the linearized amplifier. Operating temperature ranges of 30° to 50° are achieved this way[52][59][64-66][46]. More complicated configurations employing feedback control have, also, been suggested. In these, the output signal is sampled in a coupler and diode detectors are employed to measure intermodulation distortion either by switching the predistorter for re-calibration mode[52] or by detecting the spectrum spreading[57][[60] and then apply some computational method to optimize the phase shifters and attenuators in the linearizer so that the optimum distortion cancellation is obtained.

2.3.2 Adaptive Predistortion

Recently, special interest has been shown for predistortion schemes where digital signal processing predistorts the baseband modulating signal so that the effects of power

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amplifier nonlinearities are negated. A second digital signal processing is used to adaptively optimize this predistortion. Hence, the method is called adaptive predistortion. The block diagram of an adaptive predistortion linearizer is shown in Fig.2.4.

The predistorter modifies the modulation envelope to correct for the nonlinearities introduced by the power amplifier and its characteristics are, effectively, such that its nonlinearity is complimentary to that of the power amplifier. The nonlinear transfer characteristics of the predistorter can be implemented using either a look up table[71-72][75-76] or polynomial functions[77-78]. Since the characteristics of the amplifier change with temperature, time and operating level, the table elements or the coefficients of the polynomial functions change adaptively.
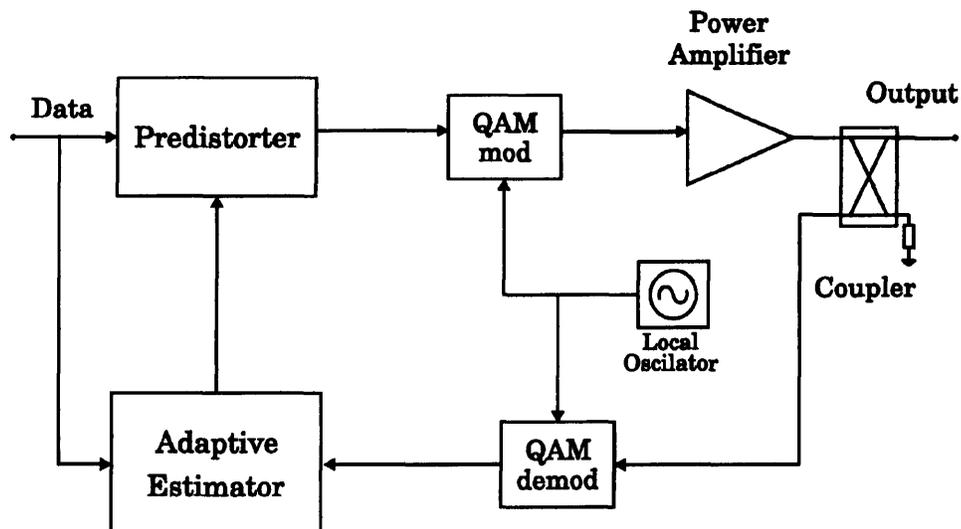
Fig.2.4 Adaptive predistortion

This is achieved by sampling the analogue signal in the output coupler and employing the demodulated signal in the feedback path. The adaptive estimator compares the desired modulation envelope with the measured modulation envelope from the output of the power amplifier to produce a loop error vector and then estimates the required predistortion. The characteristic function of the predistorter is changed so that for all

values of output voltage the loop error vector is minimum. An algorithm has to be implemented at this stage and several have been proposed[71-72][75][78], trying to improve convergence and the required convergence time. Practical implementation difficulties of the method also include accurate estimation of the delay through the feedback loop, local oscillator feedthrough and imperfections of the modulator and demodulator[71][76].

The adaptive baseband predistortion has been developed mainly with 16 QAM modulated signals for communication systems where spread spectrum should be kept very low, such as in cellular systems. Simulation work has been presented[72][75][78] predicting reduction in out-of-band distortion of excess of 25 dB and practical results have achieved 20 dB reduction of out of spectrum distortion for 8 kHz channels at 857 MHz[71] and 30 dB reduction over 30 kHz channels at 221 MHz[76].

2.3.3 Feedback Method

The feedback technique has been investigated as means of linearizing high frequency power amplifiers as early as 1964[55] and the schematic diagram of the feedback linearizer is shown in Fig.2.5. The response of the closed loop system is[55]:

$$G = \frac{AC}{1 + ABC} \qquad (2.2)$$

where G is the gain of the feedback system, A is the gain of the power amplifier, B the response of the feedback path and C the response of the narrow bandpass filter connected to the input of the amplifier to prevent spurious signal oscillations. The product ABC is the loop gain. The denominator of eq.2.2 describes the feedback loop capability to correct for distortion. Errors such as intermodulation distortion will be suppressed by a factor 1/(1+ABC) while the gain of the power amplifier is reduced by a factor C/(1+ABC) due to the feedback. Hence, the amount of distortion suppression depends on the loop gain and the system performance will improve with increased loop

gain provided that it is not increased to a point where stability is threatened.

The above linearization method has been applied to a 10 W TWTA operating at 3 GHz and achieved a reduction of the 3rd order intermodulation products of 13 dB over 0.3 MHz bandwidth with similar loss in the gain of the power amplifier[55]. Since then, alternative configurations have been investigated such as active, low frequency and IF feedback.
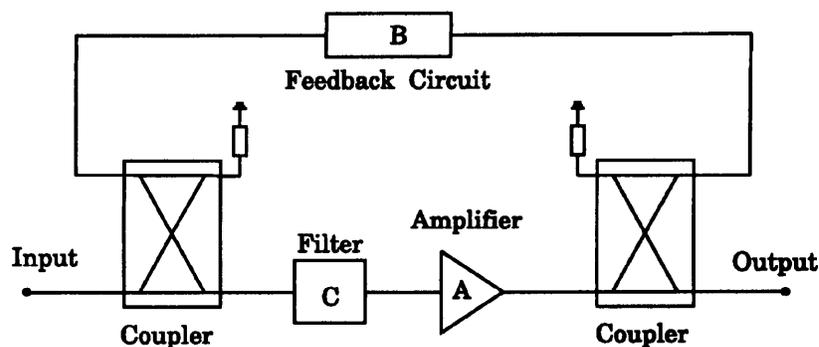
Fig.2.5 Feedback linearizer

Active feedback uses an auxiliary RF amplifier at the feedback loop so that the loss in the gain of the power amplifier can be kept low. Active feedback linearization was first applied to a one stage 27 dBm amplifier and obtained an improvement of 3.2 dB in the required amount of output power back-off of the power amplifier over 130 MHz centred at 1 GHz[87]. The technique has, recently, been implemented using MMIC technology[88]. This linearizer was directly connected across its active device terminals, in order to increase the bandwidth of operation. The linearized amplifier delivered 3 dBm at 1.6 GHz and the feedback linearizer achieved a 15 dB improvement in C/I ratio over 12% bandwidth.

The IF feedback method employs frequency conversions so that the loop filter and the auxiliary amplifier can be implemented at the IF frequency where, in general, amplifiers and filters of a given bandwidth are easier and less expensive to implement. This also

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allows the use of more complex filters which can give better control over the loop gain and lead to improved performance. The technique was applied to a 450 MHz amplifier and achieved 12 dB reduction of the 3rd order intermodulation distortion over 1 MHz bandwidth at 5 dB output power backed of from 1dB compression point[89].

Another method investigated in [90] is low frequency feedback, in which the difference frequency between two carriers is fed back from the output to the input of an amplifier stage. By choosing the appropriate transfer function for the feedback path, the re-injection of the difference frequency to the input port causes the generation of third order intermodulation products equal in magnitude but opposite in phase to those generated by the open loop amplifier, and thus a cancellation of the third order intermodulation products occurs. The implementation of a low frequency feedback system operating at 10 GHz achieved nearly 10 dB improvement of the third order intermodulation products for the carrier spacing being 10 MHz[90].

A form of feedback linearization termed Cartesian Loop has, recently, become popular due to its particular application in systems employing quadrature modulation schemes[79-81]. Cartesian Loop linearization is essentially an envelope feedback system, in which the feedback process is represented in quadrature components, with both amplitude and phase distortion to be corrected at the baseband. The method is limited by the continuous analogue feedback architecture and practical systems have been reported to achieve 45 dB reduction of intermodulation products over a 5 kHz channel at 900 MHz[79].

2.3.4 Feedforward Linearization

Feedforward linearization was first implemented at microwave frequencies by Siedel[54] who linearized a 4 GHz TWTA achieving 38 dB suppression of the third order intermodulation distortion over a 20 MHz channel. Since then, little work had been reported[51][53][69][91] until the start of this decade[70][82-85][91-101]. Today,

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feedforward linearization is considered a promising technique for microwave power amplifiers competing with the well established predistortion method.

The principle of operation of a feedforward linearizer is illustrated in Fig.2.6.
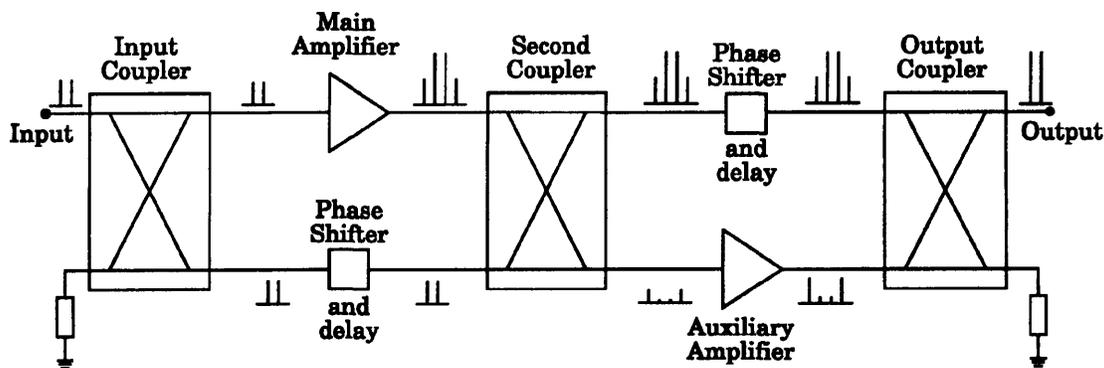
Fig.2.6 Feedforward linearizer

The input signal is sampled at the input coupler so that part of it passes through a linear path to be used as a reference. The rest of the input signal is fed to the main microwave power amplifier where, as well as amplified, is also distorted due to the nonlinear characteristics of the amplifier. At the second coupler a portion of the distorted and amplified signal is compared to the reference signal by adding the two signals 180° out of phase. The difference between them is an error signal proportional to the distortion introduced by the power amplifier. This error signal is then amplified to the appropriate power level by the auxiliary linear amplifier and is subtracted from the amplified signal at the output coupler. Thus, an error free signal is produced at the output of the linearizer.

The main advantages feedforward linearization offers are: i) inherent stability, since no feedback loops are present like in feedback linearization and ii) the fact that the error correction signal is directly extracted from the distorted signal and does not need to be independently generated like in predistortion circuits. As a result, feedforward linearizers

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are able to operate close to saturation level and over frequency ranges that cover the whole operating bandwidth of the amplifier to be linearized. That was verified by simulation and practical results for the linearizers later presented in chapters 3 and 8 of this thesis.

In theory, the feedforward technique can suppress any type of distortion the power amplifier produces over wide bandwidths. The practical limitations of the method are, however, the strict requirements for the phase and amplitude balance of the signals being cancelled in each feedforward loop. Bennett and Clements[91] were the first to address these problems. They produced theoretical curves to predict the level of distortion cancellation in the second feedforward loop for a given phase and amplitude imbalance. Since then, other researchers have published similar results[69][70][92], which reported that, for example, 25 dB distortion suppression requires a phase balance of +/-1° and a gain balance of +/-0.5 dB. As a result, there is a trade off between the operating bandwidth, which is, effectively, the frequency range over which the required balance can be obtained, and the distortion cancellation. To achieve the optimum performance of a feedforward system, a simple method of optimizing the distortion cancellation over the required bandwidth has been developed[93-94] and is further discussed in the designs of the linearizers included in this thesis.

The use of an additional amplifier has always been considered the disadvantage of the feedforward technique. It directly reduces the efficiency of the system and leads to increased circuit complexity, size and weight. That was the main reason that feedforward was more often employed at large systems such as cable television systems[95-96], where the overheads associated with feedforward circuitry are a small proportion of the total system. However, the developments in microwave transistors has made it possible to produce much cheaper and reduced size microwave amplifiers and MMIC technology will, in the near future, allow to fully exploit the advantages feedforward linearization offers. At the same time, alternative solutions to the classic feedforward configuration, which employs two equal power rating amplifiers, are investigated in order to improve

efficiency. One interesting approach is to use class C amplifiers taking, thus, advantage of their high efficiency and linearize them to obtain performances that class A amplifiers achieve with regard to linearity. Although this had been suggested since 1974[53], recently the idea has been further developed giving promising results[97]. The use of reduced delay in the feedforward loops has also been suggested, in order to reduce the losses at the high power output path and, hence, improve system efficiency, but this arrangement leads to very narrow bandwidths[97-98]. Another approach is to use an auxiliary amplifier with power handling capacity lower than that of the main amplifier leading to improved system efficiency[99-100]. This configuration allows significant improvement in the overall efficiency but care should be taken to keep the phase and amplitude balance within the required limits, because first loop imbalances can seriously effect the system performance[100]. The viability of such an approach is further discussed in chapter 4 where the CAD assessment of lower power auxiliary amplifier configurations is presented.

Feedforward linearizers have been developed since 1980 for cable television systems at frequencies in the range 100 - 300 MHz[95-96]. Increased interest in feedforward linearization has, also, been observed over the last few years due to the rapid development of the personal mobile communication systems around 900 MHz[82-85]. The use of feedforward linearization has been studied and practical implementation of the technique showed that up to 20 dB reduction of the third order intermodulation systems can be achieved for bandwidths of the order of 5% [83]. The possibility of employing MMIC technology at these systems makes the feedforward linearization a 𝀕 very attractive approach and commercially available MMIC feedforward amplifiers have already been reported for frequencies up to 1 GHz by Mini circuits[101].

In microwave frequencies feedforward linearization is not yet fully investigated due to increased matching problems and the difficulty to implement control circuits such as variable phase shifters and attenuators. A solid state microwave feedforward linearizer was reported by Dixon in 1986[69]. He implemented a 6 GHz feedforward system using

SSPAs. A reduction of 25 dB could be obtained in intermodulation distortion over a 500 MHz bandwidth but the linearizer had to be tuned for every 30 MHz channel.

Another feedforward microwave linearizer was reported in 1990 by Steel et al[70]. This linearizer employed MMIC technology amplifiers and was designed to operate over the 6 - 18 GHz bandwidth. An improvement of 20 dB and 7 dB in the second order and third order intercept points, respectively, was achieved. The authors have also suggested that the noise figure of the main amplifier could be improved as any other kind of distortion, provided that the auxiliary amplifier is appropriately designed. Unfortunately, no further results have since been reported to support this idea.

An experimental 6 GHz feedforward linearizer has, also, been developed and is further described in this thesis. The linearizer operates over the full 5.9 - 6.4 GHz band of the main amplifier and achieves 20 dB reduction in the third order intermodulation distortion. The promising results of this work indicate that feedforward linearization can be successfully employed at microwave frequencies to reduce significantly the distortion introduced by power amplifiers.

2.4 A Comparative Study of Linearization Techniques

2.4.1 Predistortion

The main advantages of this technique are simplicity of circuit, small size and weight and low power consumption. The active devices employed in predistortion linearizers are either diodes which do not require high bias voltages or transistors biased near pinch off. However, these circuit arrangements introduce high transmission loss. Predistortion linearizers exhibit a loss ranging between 8 dB [64] and 35 dB [68], making the use of a linear post-amplifier necessary.

Predistortion results in small size, compact and independent circuits. These circuits can be adjusted to linearize different amplifiers but, although independent RF predistorters have been commercially available in the past, generally, predistortion linearizers are built for a specific microwave amplifier. This allows the circuit configuration to be optimized for the particular application.

The main disadvantage of predistortion linearization lies in the way the distortion correction is generated i.e. independent of the nonlinear characteristics of the power amplifier. For perfect cancellation of the distortion the exact inverse nonlinear characteristics of the amplifier have to be obtained and, as expected, this is extremely difficult, if not impossible, to achieve over the whole operating bandwidth and dynamic range of the microwave power amplifier. Most practical predistortion linearizers are designed and analyzed as cubic distortion generators to compensate for the most troublesome third order intermodulation products[52][57][60-61][68]. However, the IM_3 products follow the 3:1 slope only when the amplifier exhibits mild nonlinearities and, in practice, they show a dependence not only on the input drive level but, also, on the number of carriers and the frequency separation between them. While the TWTAs present a dominant third order distortion, the SSPAs have also considerable fifth order products and predistortion linearizers generally do not compensate for these[59]. All the above restrict the cancellation of distortion that can be achieved to the reported levels of about 10 dB at several dB output power backed off from saturation and usually the full bandwidth of the power amplifier is not covered[63-64][68]. Some predistortion linearizers are adjusted for different channel operation [66] and/or are also adjusted for the number of carriers transmitted in multi-carrier communication systems[64].

One further disadvantage of predistortion linearization is that it cannot compensate for changes either in the components characteristics or in the amplifiers characteristics, because the circuit is effectively an open loop configuration. Although this ensures stability, it does not allow the linearizer to compensate for temperature changes and component aging effects. If the amplifier and the linearizer components are fully

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characterized, temperature changes can be taken into account by using a temperature sensor to control the bias voltages of the active devices employed in the linearizing circuit[46][52][59][64-66]. Furthermore, control feedback systems have to be added to take into account variations of the predistorted amplifier with time[52][57][60].

2.4.2 Adaptive Predistortion

The above problems encountered in RF predistortion are solved with adaptive predistortion systems. The main advantage this method offers is the ability to redefine the nonlinear characteristics of the power amplifier and change the predistortion accordingly, to compensate for input power level changes and time or temperature effects. The penalty, however, is extra digital signal processing with considerable circuit complexity and significant computation time and memory requirements.

The method is still based on the predistortion correction concept and has the same limitations of reproducing the exact nonlinear characteristic required to compensate for the power amplifier distortion. Although the loss due to the predistortion system should be minimum, since only a small fraction of the output is required for the feedback loop, the complexity of the system is significantly increased and such a linearizer has to be built around the transmitter. Considerable computing and memory is, also, required. As a result, an adaptation period of about 70 s has been reported for experimental systems[76] which is expected to be increased for more realistic signals encountered in practical systems. This could be a serious limitation for TDMA systems where the input power level and, hence, temperature varies significant between different time slots[73]. Further work should, also, be carried out to improve the immunity of the linearization to non-ideal component performance. However, the method is relatively new and still being developed and, because it is limited to single channel systems, appears to be well suited for low frequency communication systems such as cellular telephones.

2.4.3 Feedback

Analogue feedback is another technique which has been investigated as a means of linearizing power amplifiers. The advantage of this method is that the correction signal is generated from the distorted output signal and it is, at every instant, adapted to the output of the system. Therefore, this method is not restricted to third order distortion cancellation only. It is, however, the loop stability that imposes the main limitation on the performance of the linearizer and the bandwidth of the signals that can be handled. The reduction of intermodulation distortion with this method is between 10 dB[90] and 15 dB[88] and some times the amplifier has to backed off in order to achieve this performance even to as low as 10 dB from saturation[88].

The main disadvantage of the method is its narrow bandwidths. Although an impressive 200 MHz frequency range has been recently demonstrated with active feedback at 1.8 GHz[88], the feedback loop was required to be applied to the terminals of the active device in order to reduce the loop delay. For this purpose a single stage amplifier was employed. At higher frequencies, however, power devices produce considerably reduced gain and limited output power and the expected 2 - 3 dB losses[87] through the feedback system would make this approach unacceptable for single stage amplifiers. Further disadvantages of the feedback technique are the increased complexity of the circuit which, also, has to be built around the specific power amplifier and the deterioration of the loop performance due to temperature and time effects on the feedback components characteristics. Although temperature or time stability data are not usually provided for the reported feedback linearizers, the problem has been addressed at [87] where it was concluded that a means of controlling the variations of the linearizer's components is necessary.

In overall, feedback linearization is a relative complex approach from a circuit point of view, restricted to narrow bandwidths and prone to instabilities. Hence, it has not been developed very much, with the exception of the Cartesian loop configuration. Nevertheless, the use of this linearization technique could be a reasonable approach, for single channel linearization in systems where size, weight and power consumption are

not prohibiting factors. Up to date, the most successful implementation of feedback linearization is the Cartesian loop technique which has been employed in commercial transceivers for cellular systems[76][81].

2.4.4 Feedforward

Feedforward is another linearization technique for microwave power amplifiers which has, recently, received a lot of attention. Feedforward linearization provides a means of error correction that leads to bandwidths that can cover the whole of the operating frequency range of the amplifier to be linearized. Unlike feedback, this method of linearization is unconditionally stable. The inherent stability of a feedforward system results from the lack of an intrinsic feedback path. A basic feedforward system, therefore, cannot monitor its own performance and correct for any changes due to temperature or aging effects. Although such practical difficulties have, yet, to be overcome, feedforward linearization offers several advantages over the other methods which make it a very attractive and promising linearization technique.

The main advantage of the method is that the correction signal is directly generated from the nonlinearity of the amplifier so that any distortion could be suppressed irrespectively of the type of amplifier distortion characteristics. The feedforward circuit could even reduce the noise of the power amplifier[70]. This is an advantage over any predistortion technique in which the response of the power amplifier has to be tailored by another circuit with the consequent restrictions on distortion cancellation that have been mentioned earlier.

The need for an auxiliary amplifier and the consequent added cost and circuitry complexity has always been considered the main disadvantage of this technique and it often discourages its use. Nevertheless, the feedforward network is no more complex than an active feedback linearizer and it can achieve better distortion cancellation over wider bandwidths and wider dynamic ranges than both predistortion and feedback. This allows feedforward amplifiers to operate at much higher power levels and the savings

in output power and efficiency can overweight the cost and power consumption of the extra amplifier. Furthermore, the use of lower power rating auxiliary amplifier would significantly improve the efficiency of the linearizer[90][100]. A further advantage of feedforward linearization is that it has the potential to provide a failsafe mode, whereby failure of the linearization circuitry results only in reduced operational performance. This is particularly important in military applications where reliable operation is essential in vital systems and components.

The potential of employing MMIC technology in the design of feedforward linearizers has already been demonstrated in [85] and [101] and is going to further encourage the use of this technique. In the case of feedforward linearizers, the use of MMIC techniques is not only a matter of reduced size and adaptation to the new technology. Feedforward linearizers can directly benefit from the inherent wide band properties of MMIC designs because their performance is basically limited by the bandwidths of their components.

The advantages and disadvantages of the linearization techniques described above are summarised in Table I. Reported performances and areas of application for these linearizers are, also, included.

2.5 Conclusions

Linearization of power amplifiers is an attractive approach for reducing the problems arising from the nonlinear behaviour of power amplifiers in a variety of communication systems. Several linearization techniques have been developed and the ones most commonly used have been discussed in this chapter along with their potential areas of application. For single channel narrow band systems the most popular techniques today are Cartesian loop and adaptive predistortion which have been developed for cellular systems employing quadrature modulation schemes. Feedforward has not yet gained widespread recognition in narrow band systems because of its increased size and the

requirement for an auxiliary amplifier. However, it offers a number of significant advantages such as excellent improvement in linearity, inherent stability and better noise performance and the benefits arising from the use of feedforward linearization in the above narrow band systems are currently being investigated[98].

For wide band applications feedforward and RF predistortion are the only linearization techniques that could be used effectively. Multi-carrier systems such as mobile communications base stations and satellite transponders and earth stations require the simultaneous transmission of a number of channels of information, each of which may carry any kind of information. The most flexible and power efficient method for achieving the channel combination is to use a broadband low level combiner followed by the transmitter power amplifier. Feedforward linearization and RF predistortion are the only techniques that could enable just one linearized power amplifier to cover the whole operating band of communication systems rather than linearizing amplifiers for separate channels. Compared to predistortion, feedforward linearization offers the advantages of much better distortion cancellation over wider dynamic ranges and bandwidths and the potential to provide a failsafe mode of operation. However, this technique has not yet been fully developed due to its increased circuit complexity.

In the remainder of this thesis the feedforward linearization technique is further analyzed and developed. Computer aided design techniques are first employed to assess the method and study the particular problems of circuit sensitivity to phase or amplitude imbalance and the reduced efficiency due to the need for an auxiliary amplifier. Finally, low power rating auxiliary amplifier configurations are evaluated. Furthermore, an experimental feedforward linearizer is developed employing MIC technology. This linearizer achieves 20 dB reduction of the intermodulation products covering the dynamic range of the main amplifier over the whole commercial satellite band 5.9-6.4 GHz. The performance of this linearizer demonstrates that feedforward linearization can be successfully employed to microwave amplifiers achieving improvements in the linearity of the amplifier that overweight the increased complexity of the method.

TABLE I

	RF Predistortion	Adaptive Predistortion	Feedback	Feedforward
Distortion cancellation	10 dB [63] 15 dB [66] 18 dB [60]	20 dB [71] 30 dB [76]	12 dB [89] 15 dB [88] 45 dB [79]	20 dB [83] 25 dB [69] 20 dB(IP_2) & 7 dB(IP_3) [70] 20 dB [Thesis]
Frequency Range	2 GHz at 11 GHz [63] 250 MHz at 11 GHz [66] 200 MHz at 5 GHz [16]	8 kHz at 857 MHz [71] 30 kHz at 221 MHz [76]	1 MHz at 450 MHz [89] 12% at 1.6 GHz [88] 5 kHz at 900 MHz [79]	5% at 900 MHz [83] 30 MHz at 6 GHz [69] 6 - 8 GHz [70] 500 MHz at 6 GHz [Thesis]
Advantages	• wide bandwidth • stability • low power consumption • simple circuits • small size and weight	• adapts to variations with time/ temperature/drive level • employs low frequency techniques	• corrects every variation in amplifier's output • allows IF frequency or baseband implementation	• excellent distortion reduction • wide bandwidths • corrects any type of distortion including noise • stability • failesafe mode
Disadvantages	• needs to tailor amplifier's responce • no temperature/time/power level compensation • high loss	• circuit complexity • increased computation • large memory requiremets • long adaptation time	• narrow bandwidth • instability • circuit comlexity • active configureation requires auxiliary amplifier	• circuit complexity • requires auxiliary amplifier • no temperature/time compensation
Applications	• single & multi carrier systems • satellite communications[13-21] • digital µwave links[7][9-11] • mobile communications • active array antennae[21]	• single carrier systems • cellular phones[23][28]	• narrow band systems • satellite earth stations[5] • mobile communicatios base stations • cellular phones[23][28]	• single & multi-carrier systems • satellite communications[19] • mobile communications • active array antennae[22] • personal communications[34-37]

CHAPTER 3

Design and Performance Evaluation of a Simulated Microwave Feedforward Linearizer

3.1 Introduction

Most Microwave Integrated Circuits (MICs) designed today are tested using Computer Aided Design (CAD) software before final fabrication. These design tools are now well established and have been proven to be a cost effective technique for complex design where prototyping is expensive[102]. The design software Eesof Academy[103] has been employed to design and evaluate a solid state feedforward linearizer for operation in the satellite communication band 5.9 to 6.4 GHz. The software employs the harmonic balance technique[104] to predict higher order harmonics and intermodulation products and the active devices are modeled using nonlinear lumped element models like the Curtice and Ettemberg GaAs FET model[105].

The simulated linearizer was designed for the highest linear performance and was optimized to operate at 2 dB below saturation level. A systematic method based on single tone simulation was developed for the optimization of feedforward linearizers over the required operating bandwidth[93]. The optimized linearizer exhibits an improvement in the intermodulation distortion of the main power amplifier, of at least 20 dB over the full bandwidth for various carrier combinations[106].

In this chapter the design criteria of the overall linearizer, as well as the description of the individual components incorporated, are presented. A schematic of the linearizer design is, also, included with the optimised component parameters.

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3.2 Feedforward Linearizer Design Aspects

3.2.1 Design Equations

The principle of operation of feedforward linearization is illustrated in the block diagram of Fig.3.1. The input signal, consisting of two carriers, is amplified by the main power amplifier which, also, produces intermodulation distortion. Part of the input signal is also sampled in the first coupler to be used as a reference signal through the linear arm A of the first loop. The first loop is set up so that the reference signal and the coupled amplified signal are equal in amplitude and 180° out of phase at the output of the second coupler. Thus, at the arm B of the second coupler the two carriers are cancelled leaving an error signal analogous to the distortion introduced by the main amplifier. The following equation must hold in order to achieve the required amplitude balance:

$$C_1 \ L_1 \ T_2 = T_1 \ G_1 \ C_2 \tag{3.1}$$

where G_1 is the linear gain of the main amplifier, C_1 the coupling ratio of the input coupler and T_1 the associated transmission loss, C_2 and T_2 the coupling factor and the transmission loss of the second coupler and L_1 the loss through the delay element.
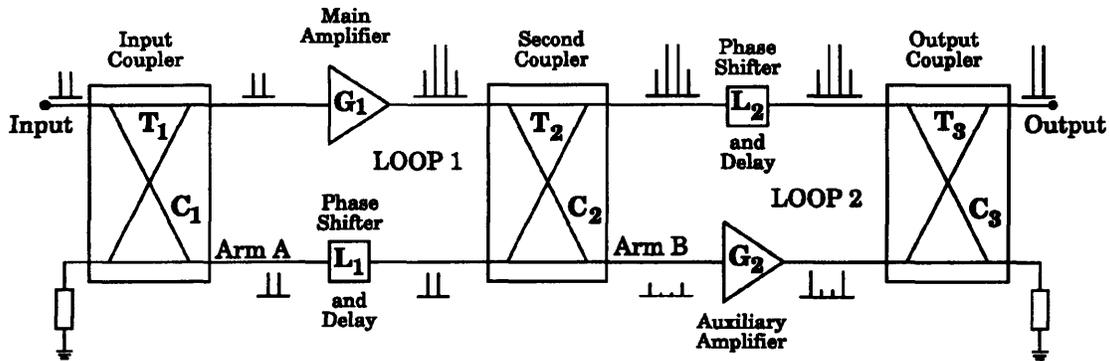
Fig.3.1 Feedforward linearizer

In the second loop the error signal is linearly amplified by the auxiliary amplifier and then subtracted from the main amplifier's output to cancel the distortion. Therefore, the second loop is set up so that the error signal and the distortion in the main signal are

equal in amplitude and 180° out of phase at the output of the third coupler. The amplitude balance is achieved when:

$$T_2 \, L_2 \, T_3 = C_2 \, G_2 \, C_3 \qquad (3.2)$$

where G_2 is the linear gain of the auxiliary amplifier, C_3 the coupling ratio of the output coupler, T_3 the associated transmission loss and L_2 the loss through the delay element.

Equations 3.1 and 3.2 summarize the conditions for amplitude balance in each of the feedforward loops so that the signals to be compared are properly cancelled. Based on these equations the design criteria for each component incorporated in the linearizer are discussed next, considering the requirements for optimum system efficiency and some practical implementation issues.

3.2.2 Component Design Considerations

The most important component in the feedforward linearizer design is the auxiliary amplifier. The power consumption of this amplifier governs the efficiency of the feedforward system and its performance determines the distortion cancellation achievable by the linearizer. The gain of the auxiliary amplifier as a function of the input and output couplers' coupling ratios and the gain of the main amplifier can be determined by combiningeq.3.1 and 3.2:

$$G_2 = \frac{L_2}{L_1} \, \frac{T_1 \, T_2}{C_1 \, C_2} \, G_1 \qquad (3.3)$$

From the above equation it is apparent that loose coupling at the input and output couplers requires that the gain of the auxiliary amplifiers is much higher than the gain of the main amplifier. Therefore, the auxiliary amplifier will require several stages to produce the desired gain which directly results in reduced power added efficiency. Longer delay elements are, also, introduced in the second loop and the associated delay loss L_2 reduces the output power of the linearizer. Low coupling ratios in the output coupler, also, imply increased output power of the auxiliary amplifier. Since the coupled

error signal and the distortion in the main signal must have the same amplitude at the output, the auxiliary amplifier must provide sufficient power to account for the coupling loss through the output coupler.

Hence, it is desirable to keep the coupling ratio of the output and the input couplers as high as possible in order to relax the requirements for the power rating and gain of the amplifier and reduce the high power path delay loss. Nevertheless, tight coupling means loss of the main signal. In particular, any losses through the output coupler directly reduce the output power and, thus, the efficiency of the system. There is, therefore, a trade off between the loss in the output coupler and the requirement for low power and low gain auxiliary amplifier. The usual choice is loose coupling for the output coupler to preserve the output power and high coupling ratio for the input coupler to keep the gain of the auxiliary amplifier low. The loss in the input coupler is not as critical because it only concerns low power gain. Typical values for the output coupler are in the range of 10 - 20 dB. A coupling lower than 20 dB makes the gain of the auxiliary amplifier prohibitively high, while coupling tighter than 10 dB results in unacceptable level of transmission loss and it is, also, difficult to fabricate in microstrip. The feedforward linearizer presented in this chapter employs a directional coupler[107] at the output. The input coupler, however, was chosen to be a 3 dB hybrid which is easily realized in microstrip by a branch line coupler[35] or a Wilkinson divider[38]. With a 3 dB coupling at the input, $T_1 = C_1$ in eq.3.1 and the second coupler must be:

$$C_2 = \frac{L_1 \, T_2}{G_1} \tag{3.4}$$

The above equation implies low coupling ratios for the second coupler as well, determined by the gain of the main amplifier. This coupler is placed at the output of the main amplifier and its transmission loss should, also, be kept minimum. The gain of the auxiliary amplifier for a 3 dB input coupler becomes:

$$G_2 = \frac{L_2}{L_1} \frac{T_3}{C_3} G_1 \qquad (3.5)$$

If, for simplicity the transmission losses through the couplers and the delay lines are considered negligible and omitted in the above equation the gain of the auxiliary amplifier reduces to:

$$G_2 \approx \frac{G_1}{C_3} \approx G_1 - C_3 \quad dB \qquad (3.6)$$

where $C_3 < 1$ and in dB it is a negative value. Thus, the gain of the auxiliary amplifier in dB is approximately equal to the gain of the main amplifier plus the coupling ratio of the output coupler.

Having decided that one 3 dB hybrid and two directional couplers should be employed in the linearizer, a minimum of 4 dB reduction in the gain of the main amplifier should be expected due to the linearizer circuit. In order to overcome this limitation feedforward linearized SSPAs must consist of two or more stages of amplification.

The main amplifier of the linearizer was designed for highly linear output power in order for the linearized amplifier to achieve the best possible linear performance. The auxiliary amplifier, however, need not have as high output power as the main one, because it only handles the distortion products and any residual carriers which are at much lower power levels than the output signal. Further considerations on the design criteria of the auxiliary amplifier will be presented in chapter 4 based on the CAD analysis of the feedforward linearizer.

3.3 Computer Aided Design of the Main and the Auxiliary Amplifier

The nonlinear CAD software employed to design and simulate the amplifiers includes data for the nonlinear model of [105] for several microwave transistors[108]. Of these the Avantek GaAs FET AT8151 was chosen because it produces the higher output

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power at the frequency of interest. It is a 1 watt device with a gain of 6.5 dB at 8 GHz and the relevant specifications are included in Appendix 1.

Since the nonlinear model library of the software includes only chip devices, it was decided to use the same transistors for all the stages for both the main and the auxiliary amplifier in order to ease the ordering procedure and the fabrication of the amplifiers. However, different bias conditions were chosen since the main amplifier was designed for high linear output power, while the auxiliary amplifier was designed for high transducer gain.

The S parameters of the transistor depend on the bias conditions and were obtained with simulation of its nonlinear model. This enabled the generation of S parameter data which were, then, used for the small signal design of the two amplifiers.The chosen bias conditions were:

High gain: Vds = 4 V   Ids = 512 mA

High power: Vds = 9 V   Ids = 313 mA

In Fig.3.2 the simulated I - V characteristics of the Avantek GaAs FET AT8151 are shown together with the chosen biasing points. The simulated low power S parameters are provided in Appendix 2.

3.3.1 Main Amplifier

The main amplifier is a two stage, class A amplifier designed for high output power. An optimization method, similar to the load pull technique, was employed, using the nonlinear simulator of the software. The load pull technique is, as explained in section 1.5.3, a practical method of measuring those terminal impedances which, when applied to a device, enable it to have particular linear or nonlinear characteristics. A similar procedure was followed, the only difference being that instead of actually

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measuring the output power of the device the corresponding model was used to simulate its nonlinear characteristics.
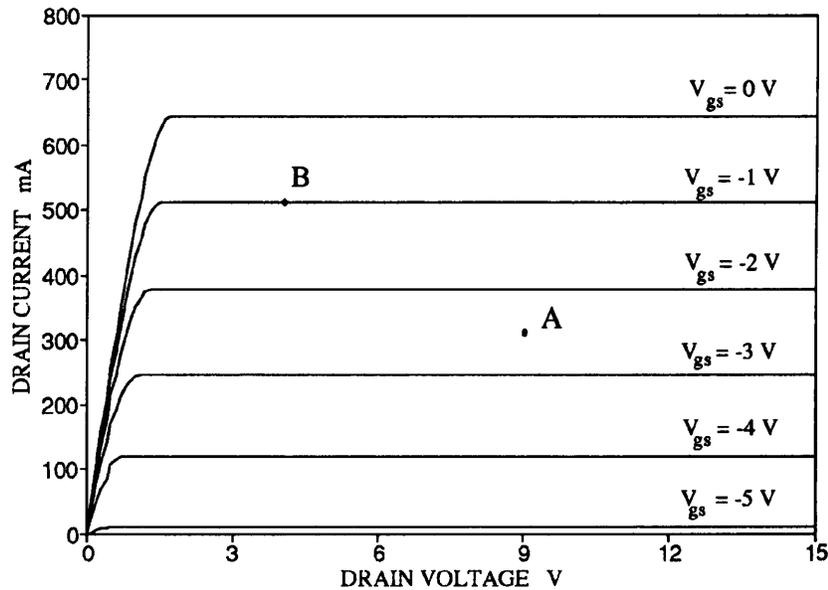
Fig.3.2 Simulated I - V characteristics of the Avantek GaAs FET AT8151

A network was designed to match the input of the device to 50 Ω, while the parameters of the output matching network were allowed to vary in order to obtain the optimum load condition. The single stub matching technique with open circuit stubs was the technique employed for all the matching networks. The length of the stub and the length of the 50 Ω line were optimized for high output power at large signal conditions for the frequency range 5.9 - 6.4 GHz and provided the optimum matching circuit for high linear output power for this device. The interstage and input matching networks were, then, synthesized and optimized using the low power S parameters shown in Appendix 2 and the initial values for these networks were determined following the procedure for reactive matching described in section 1.5.3. CAD optimization for high and flat linear gain and good return loss concluded the design. A compromise had to be made between flat gain and input matching since amplitude balance is very important in the operation of the feedforward linearizer. It was, therefore, decided to include a mismatch at the

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input network in order to achieve the required gain flatness over the full bandwidth. To ensure an overall good match an isolator was placed at the input port. The isolator was represented in the design as an S parameter file with the characteristics that manufacturers typically quote for microstrip isolators: 20 dB isolation, 20 dB return loss and 0.5 dB insertion loss. The S parameters of the simulated isolator are included in Appendix 2.

The AT8151 is conditionally unstable at 6 GHz since $K < 1$ and $\Delta < 1$, where K and Δ are defined in eq.1.17 and eq.1.18 respectively. Care was taken to ensure stable operation within and outside the band. At frequencies higher than 6 GHz, the gain of the device is dramatically reduced so that stable operation is easily achieved. At low frequencies, however, the transistor has considerable gain and it was proved impossible to keep the input reflection coefficient less than one for frequencies below 1 GHz. This is a problem often encountered in transistor amplifier designs and is usually solved when the bias networks are included in the design. The DC bias networks are designed to be transparent over the bandwidth of the amplifier but, at frequencies away from the operating band they introduce high loss and, thus, improve stability. Once the biasing networks were included in the design the input reflection coefficient remained less than one indicating stable operation.

The schematic diagram of the main amplifier is shown in Fig.3.3. The amplifier and all the remaining components of the linearizer were designed to be built on microstrip employing the 0.030" Rogers RT/Duroid material, type 5880. The DC blocking capacitors and the bias network required for the nonlinear simulator are also included. The final amplifier has a gain of 14 dB and return loss better than 17 dB. Both simulated gain and matching characteristics are shown in Fig.3.4. Nonlinear simulation verified that the optimised amplifier is very linear with an output power at 1 dB compression point of 30 dBm, same as the saturation power. The amplitude and phase response at large signal operation are given in Fig.3.5.

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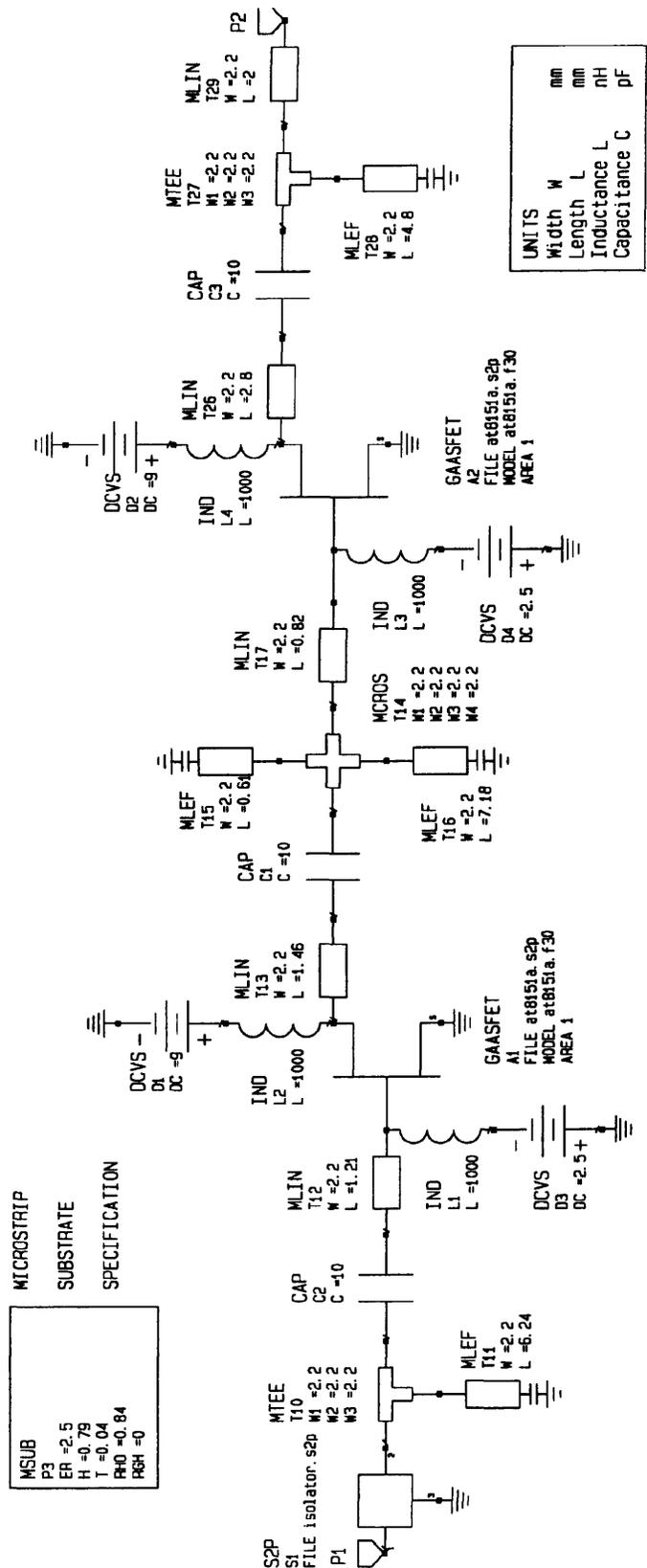
Fig.3.3 Academy schematic diagram of the main amplifier
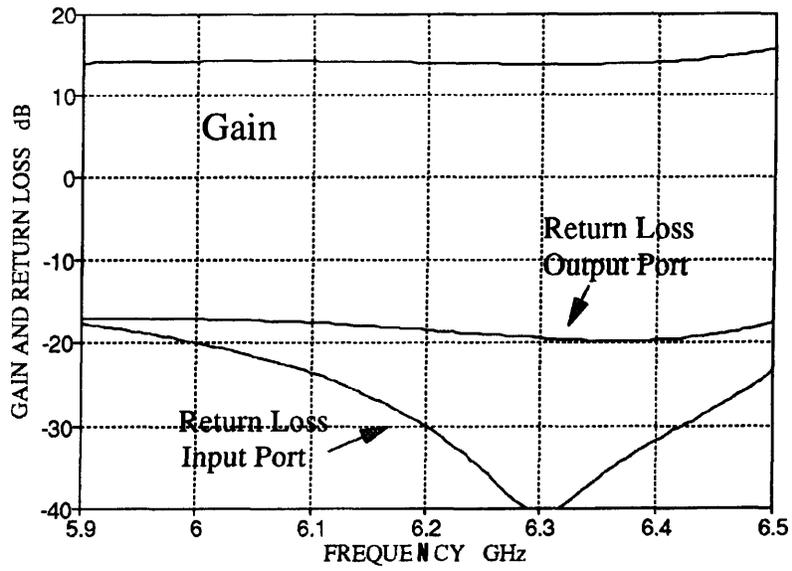
Fig.3.4 Gain and return loss of the main amplifier
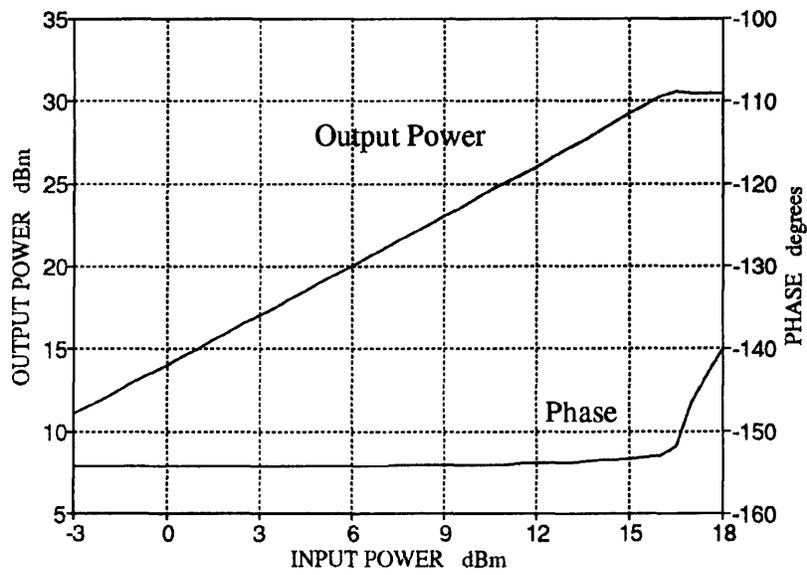
Fig.3.5 Large signal characteristics of the main amplifier

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3.3.2 Auxiliary Amplifier

The gain of the auxiliary amplifier in dB is defined by eq.3.6 to be approximately equal to the 14 dB gain of the main amplifier plus the coupling factor of the output coupler, which is between 10 - 20 dB. Thus, three gain stages were, at least, required. Since this amplifier does not need to have output power as high as 30 dBm, it was designed for high gain employing the small signal S parameters of Appendix 2. Because the device is conditionally unstable at 6 GHz a conjugate match cannot be achieved and the design procedure explained in section 1.5.1 was followed, with the output matching network designed first to provide about 9 dB gain and stable operation. Stability outside the band was checked with the biasing networks included. Single stub matching with open circuited stubs was employed in the design of the matching networks. The circuit was then optimised for high and flat gain with good return loss over the frequency range 5.9 to 6.4 GHz. To achieve gain flatness over the full bandwidth the input matching was again sacrificed and an isolator as described in the previous section 3.3.1, was placed at the input of the amplifier.

The schematic diagram of the auxiliary amplifier, including DC blocking capacitors and bias networks, is given in Fig.3.6. The optimized amplifier has a gain of 26 dB and return loss better than 16 dB. The simulated gain and return loss are shown in Fig.3.7. The amplifier was, also, nonlinearly simulated and the amplitude and phase characteristics for increasing input power levels are presented in Fig.3.8. It can be seen that the auxiliary amplifier has a saturation power 7 dB lower than the main amplifier.

Fig.3.6 Academy schematic diagram of the auxiliary amplifier

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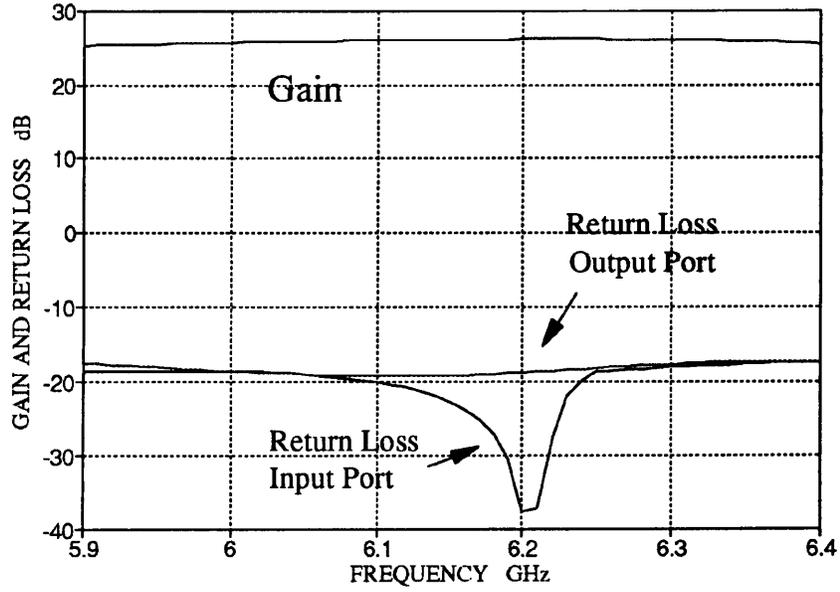
Fig.3.7 Gain and return loss of the auxiliary amplifier
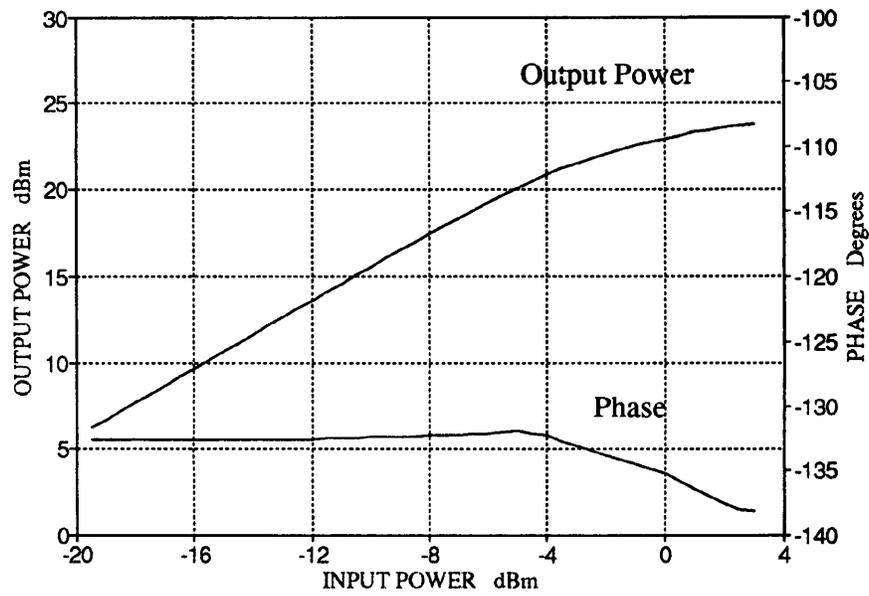
Fig.3.8 Large signal characteristics of the auxiliary amplifier

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3.4 Design of the Individual Components

This section provides further details on the design of the other components incorporated in the simulated linearizer. The configuration of the couplers is first discussed followed by a brief analysis of the Schiffman phase shifters[109] which are employed to achieve the required phase difference of 180° between the two paths in the feedforward loops. Finally, the need for a bandpass filter employed at the input of the auxiliary amplifier is discussed.

3.4.1 Couplers

The 3 dB input hybrid was realised with a branch line coupler[35] having its isolated port terminated by a 50 Ω resistor. Directional couplers[107] were employed for the second and output couplers. The microstrip layout of a directional coupler is shown in Fig.3.9, where the length L of the coupled lines is 90° at the centre frequency while the width W and the space S determine the coupling ratio[107].
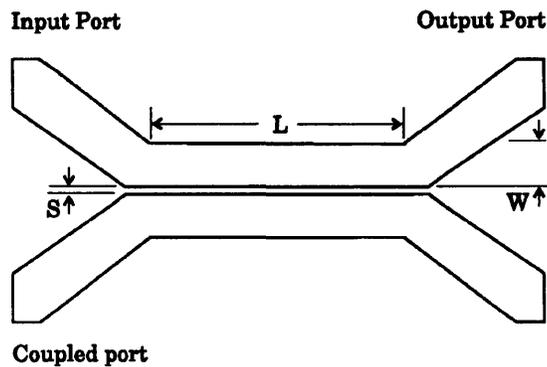
Fig.3.9 Directional coupler

The coupling factor of the second coupler is defined by eq.3.4. If, for simplicity the loss through the coupler and the delay element are considered negligible and omitted in the above equation, then, the coupling ratio C_2 becomes approximately equal to the gain of the main amplifier:

$$C_2 \approx \frac{1}{G_2} \approx - G_2 \quad dB \qquad (3.7)$$

A directional coupler with coupling ratio 14 dB was, therefore, used as the second coupler. The coupling factor of the output coupler is defined by Eq.3.6 to be the

difference between the gain of the auxiliary amplifier and the gain of the main amplifier. The output coupler was, therefore, realized with 12 dB directional coupler.

The through loss in the couplers T_2 and T_3 and the delay elements L_1 and L_2 included in eq.3.1 and eq.3.2 were not taken into account in the initial design of the couplers. Any small adjustments in the coupling ratios, required for optimum balance in the feedforward loops, were performed when the overall linearizer was optimized, as will be described in section 3.6.

3.4.2 Schiffman Phase Shifters

In the Schiffman phase shifters[109] the desired phase shift is obtained by subtracting the phase response of a C-section from the phase response of a delay line of suitably chosen length. The C-section is a pair of coupled lines with adjacent ports interconnected as shown in Fig.3.10.
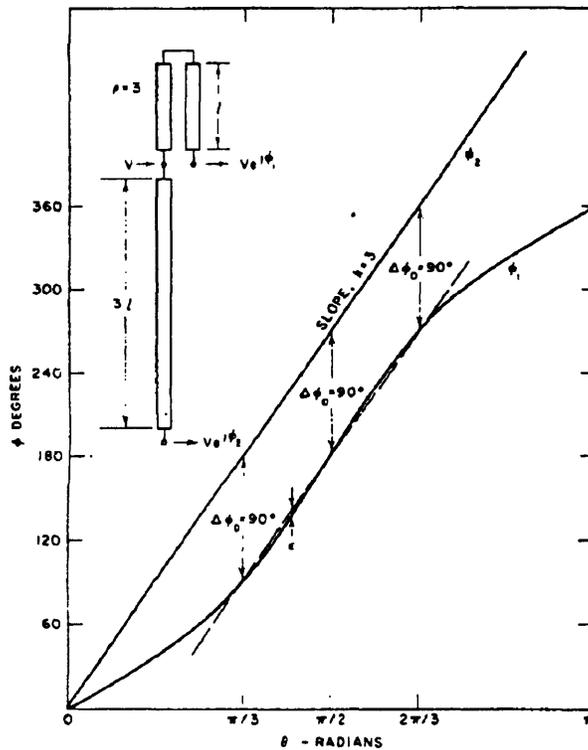
Fig.3.10 A 90° Schiffman phase shifter[109]

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The phase response of this structure is given by the equation[109]:

$$\phi_2 = \cos^{-1}\left(\frac{\rho - \tan^2\theta}{\rho + \tan^2\theta}\right) \tag{3.8}$$

where θ is the electrical length of the coupled section and ρ is its impedance ratio defined as:

$$\rho = \frac{Z_{0e}}{Z_{0o}} \tag{3.9}$$

where Z_{0e} and Z_{0o} are the even and odd mode impedances of the coupled line section. The impedance ratio and the coupling ratio are related by :

$$C = -20 \log \frac{\rho - 1}{\rho + 1} \tag{3.10}$$

If the delay line has an electrical length of $\phi_1 = K\theta$ then the phase difference between the two structures is:

$$\Delta\phi = \phi_1 - \phi_2 = K\theta - \cos^{-1}\left(\frac{\rho - \tan^2\theta}{\rho - \tan^2\theta}\right) \tag{3.11}$$

The coupled line can be designed so that the phase difference $\Delta\phi$ stays the same over the required frequency range as shown in Fig.3.10. In order to get the desired phase performance, the constants K, ρ and θ must be chosen properly. A direct method for designing Schiffman phase shifters has been developed by J.L.Ramos Quirarte et al[110] which produced design equations that allow to design the phase shifter for a specific bandwidth or a specific phase deviation.

The schematic diagram of a C-section and the corresponding layout are shown in Fig.3.11 and Fig.3.12 respectively. Due to the limitations of the software, part of the coupled lines was simulated with the coupled line element[111] and part of it with a microstrip gap element[111], in order to produce the right layout. The practical evaluation of this model will be discussed in section 5.2 of chapter 5.

Schiffman phase shifters were used in the design of the linearizer in order to achieve the 180° phase difference between the two paths of the feedforward loops and to match the phase characteristics of the amplifiers in each loop. Since the amplifiers' phase response is a nonlinear function of frequency, a linear delay line alone cannot be used to compensate for the phase shift in the amplifiers. Thus, a combination of a microstrip line and a Schiffman phase shifter with the characteristics of Fig.3.10 were used to tailor the amplifiers' phase response and provide at the same time 180° phase difference between the two paths.
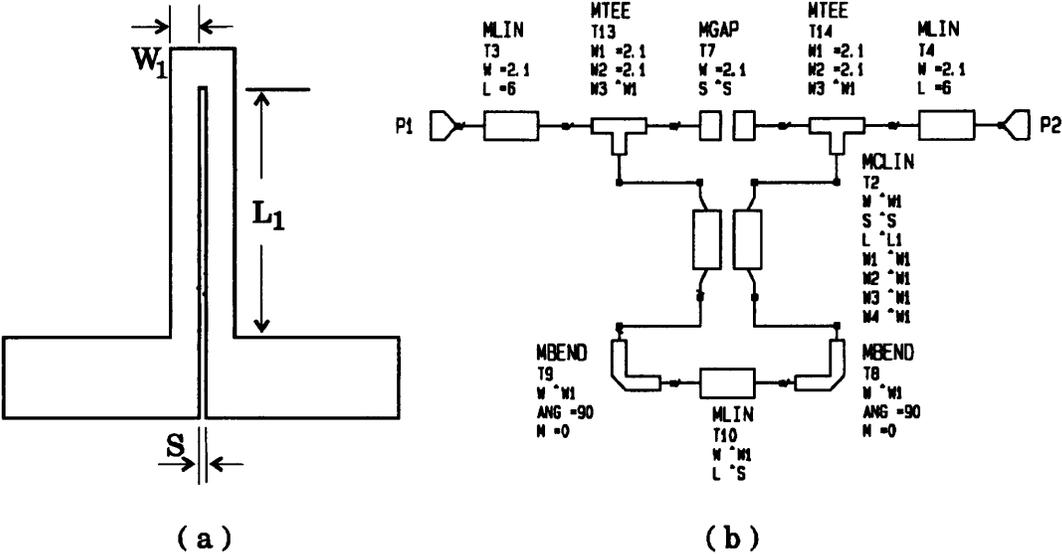
Fig.3.11 Designed Schiffman phase shifter (a) layout (b) Academy schematic

The initial values for W_1, S and L_1 were calculated using the equations in [110] for the smallest possible phase variation across the band. The phase shifters were, then, simulated employing the model of Fig.3.11(b) and further optimised for a flat phase response over the band.

3.4.3 Band Pass Filter

Feedforward linearizers are primarily designed to remove in-band third order intermodulation distortion at frequencies $2F_1-F_2$ and $2F_2-F_1$, where F_1 and F_2 are the frequencies of any two carriers requiring amplification. Out-of-band intermodulation products and higher harmonics are, usually, of little interest since they can be filtered out at the output of the linearized amplifier. Nevertheless, out-of-band distortion produced by the main amplifier can affect the performance of the overall feedforward system especially at large signal conditions. This arises from the nonlinearity of the auxiliary amplifier.

Ideal operation of the feedforward linearizer assumes perfect cancellation of the carriers in the first loop, so that only the distortion signals are fed to the auxiliary amplifier. In practice, however, only a finite cancellation will be achieved in the first loop, resulting in residual carriers entering the auxiliary amplifier. On the other hand, as the main amplifier is driven into nonlinear operation second order intermodulation products at frequencies F_1-F_2 and F_1+F_2 rise rapidly. Depending on the out of band performance of the second coupler part of these products will be fed to the auxiliary amplifier. Consequent second order interaction within the auxiliary amplifier, between second order mixing products at frequencies the F_1-F_2 and F_1+F_2 and residual carriers at the frequencies F_1 and F_2, leads to generation of further third order intermodulation products which could upset the balance of the second loop. The second order intermodulation products at frequencies F_1+F_2 are of little concern because the gain of any practical microwave amplifier at frequencies twice the operating frequency is very low. Nevertheless, the low frequency gain can be significantly high. To avoid any further third order intermodulation products generated within the auxiliary amplifier the above frequencies have to be filtered out.

In order to do this, a band pass filter was employed at the input of the auxiliary amplifier. It was a quarter wave coupled line filter [107] realized in microstrip. Its layout is shown in Fig.3.13. The filter was simulated using the Eesof model for

microstrip coupled lines filters[111] and it was optimized for low loss within the band and high insertion loss at low
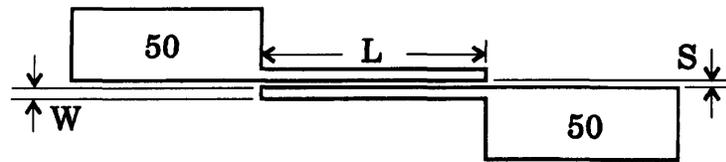
Fig.3.12 Coupled lines microstrip filter

frequencies. The final values for the width W, the spacing S and the length L of the filter were : W=0.36 mm, S=0.20 mm and L=8.67 mm. The simulated response of the filter is shown in Fig.3.13, where it can be seen that the intermodulation signals at frequencies F_1-F_2 for any carriers within the 5.9-6.4 GHz band will be effectively suppressed. Thus, any nonlinear behaviour of the auxiliary amplifier due to the out-of-band distortion products will be avoided.
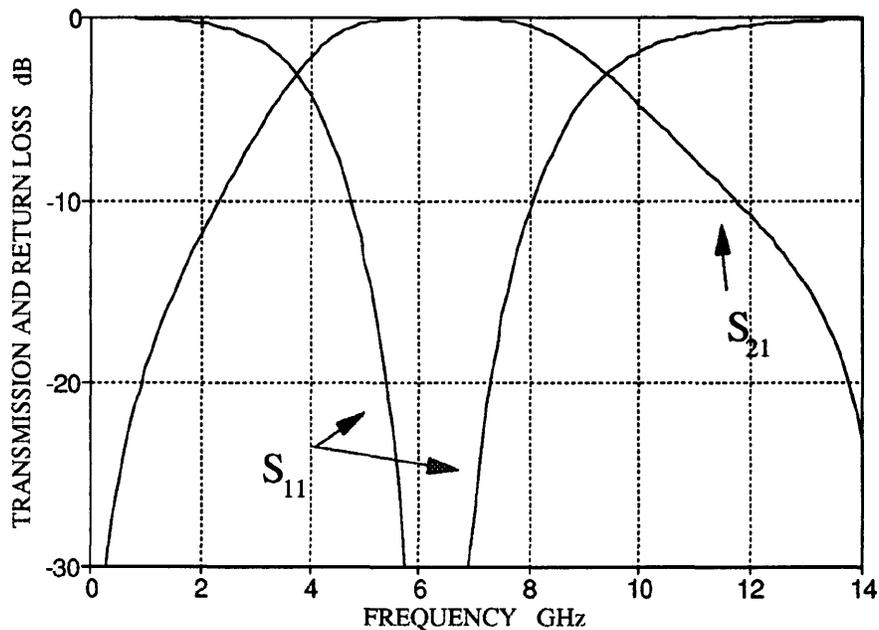
Fig.3.13 Transmission and return loss of the coupled lines filter

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3.5 Design of the Feedforward Linearizer Circuit

The schematic diagram of the designed feedforward linearizer is given in Fig.3.14. The first loop consists of the input branch line coupler, the main amplifier, a 14.5 dB directional coupler, one Schiffman phase shifter and a microstrip delay line. The branch line coupler and the directional coupler produce, each of them, a 90° phase shift between the two paths in the first loop. Therefore, the phase difference between the two signals compared in the second coupler is 180° due to the phase characteristics of the couplers alone. Hence, if the delay in the arm A of the first loop (Fig.3.1) is equal to the delay of the amplifier, no further phase shift is required in this loop. Nevertheless, the phase response of the amplifier is nonlinear and it cannot be balanced with a delay line alone. To determine the required value for the Schiffman phase shifter, an ideal delay element[111] and an ideal phase shift element[111] were employed to model the phase response of the main amplifier. These elements were optimized to match the phase characteristics of the amplifier and it was found that the response of the amplifier can be represented by a delay of 551 ps and a 6° phase shift. Hence, a 551 ps long microstrip line and a 6° Schiffman phase shifter were introduced at the reference path to balance the phase characteristics of the main amplifier.

The second loop consists of the middle 14.5 dB coupler, the auxiliary amplifier, one Schiffman phase shifter, a delay line, the output 12 dB coupler and the band pass filter at the input of the amplifier. Following the same procedure as for the design of the first loop, a 118° Schiffman phase shifter and a 933 ps microstrip delay line were used to provide the 180° phase difference between the two signals and a delay equal to that of the amplifier over the band. The initial design of the feedforward linearizer was based on the requirements for amplitude and phase balance in each loop. Nevertheless, over the frequency range 5.9 - 6.4 GHz the gain and phase response of the various components deviates from the centre frequency value and fine adjustments of the phase shifters, delay lines and the couplers were required to obtain the optimum performance across the band. The method developed to optimize the performance of the linearizer over the full operating bandwidth is described next.

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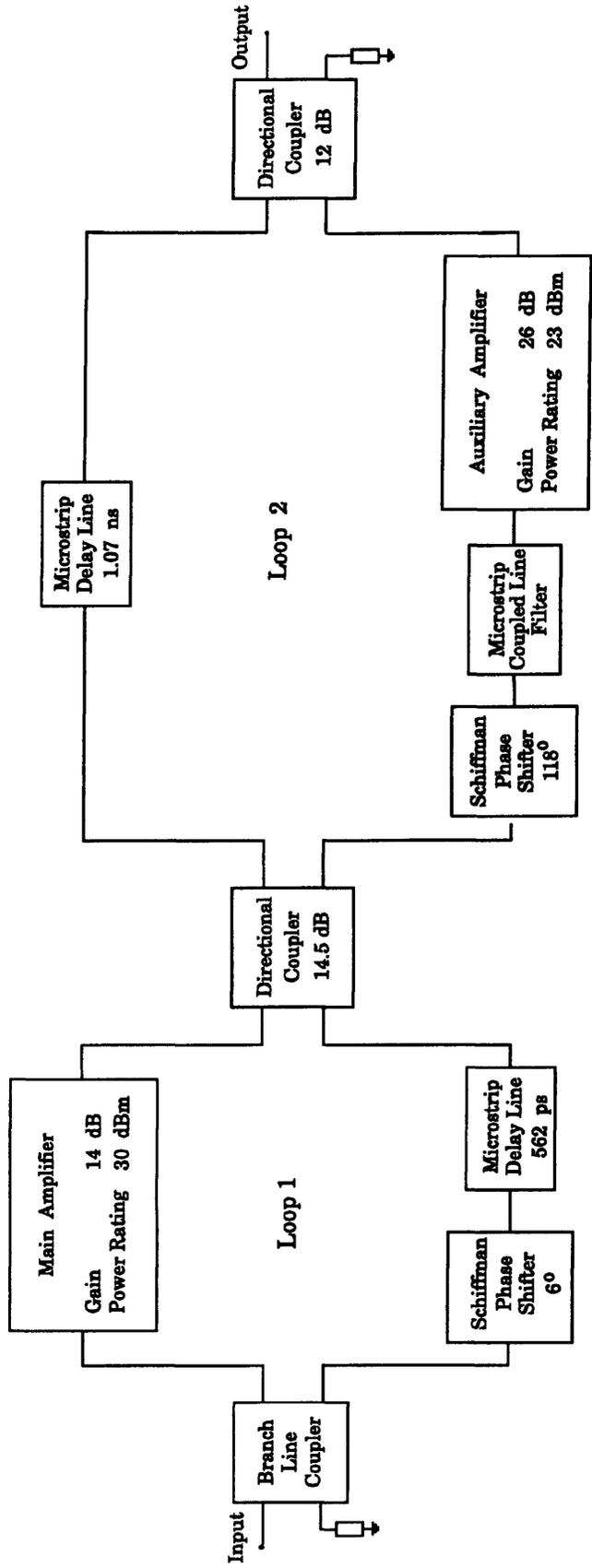
Fig.3.14 Block diagram of the 6 GHz feedforward linearizer

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3.6 Optimization Method for Feedforward Linearizers

The feedforward linearization technique is, in theory, capable of operating over very broad bandwidths and provide perfect distortion cancellation[54]. In practice, however, precise balance of the phase, delay and amplitude over the full operating bandwidth is difficult to achieve, due to the amplifiers' and couplers' nonlinear amplitude and phase response. A systematic and efficient method has, thus, been developed [93] to optimize the performance of feedforward linearizers over the desired frequency range. The method is based on the concept that each feedforward loop may be optimized independently of the other, provided that the auxiliary amplifier does not create any further intermodulation distortion.

Ideal operation of the feedforward linearizer assumes that the auxiliary amplifier will operate linearly. However, any practical amplifier will also distort the error signal that it is required to amplify and will, thus, produce a finite level of intermodulation distortion. Nevertheless, if the first loop operates correctly, the residual carriers that enter the second loop are so low that the intermodulation products of the auxiliary amplifier should be negligible compared to the distortion of the main amplifier. Filtering the out of band second order harmonics as well, ensures that no significant distortion is introduced by the auxiliary amplifier. In the case where the auxiliary amplifier produces significant intermodulation products, this distortion is added directly into the output signal and presents, as a consequence, a fundamental limit on the performance. When this is the case, the operation of the first loop should be re-examined or an auxiliary amplifier with a higher output power should be considered.

Having established that the two loops can be considered independently, CAD techniques can be implemented to optimize each of them individually. As will be explained in the next sections a single frequency can be implemented in the optimization process. This, along with the fact that smaller circuits are optimized, reduces dramatically the required simulation time. Furthermore, the method allows fine adjustments of the optimized

parameters so that, in each loop, one path tailors the response of the other to achieve the optimum balance over the whole bandwidth.

3.6.1 First Loop Optimization

In the first loop, shown in Fig 3.15 the input signal is suppressed at the arm B of the second coupler, in order to extract the distortion introduced by the main amplifier. Any signal input to the system should, thus, be cancelled as shown in Fig.3.16 for two carriers. A single frequency can, therefore, be used to analyze the circuit with the first loop optimized for minimum output power at the arm B. If the frequency is swept over the 5.9 - 6.4 GHz the linearizer is optimized over the whole band.
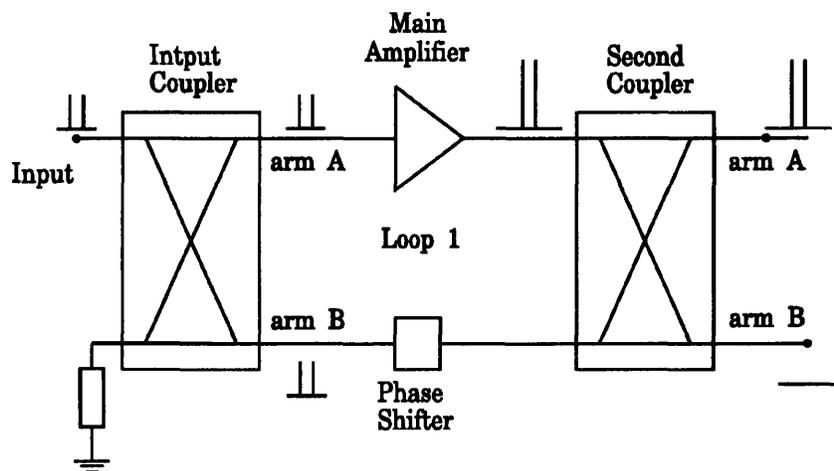
Fig.3.15 First loop of feedforward linearizer

The small signal characteristics of the main amplifier change under large signal operation and, therefore, the phase and amplitude response of the reference path required for loop balance will be different for low and high input power levels. The feedforward linearizer was optimized for large signal conditions to increase the system efficiency. Harmonic balance simulation was, thus, employed in the optimization, to take into account phase distortion and compression phenomena in the main amplifier. The length of the delay line, the phase of the Schiffman phase shifter and the coupling ratio of the second coupler were allowed to vary in the optimization with the restriction that the

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return loss of the optimized components should remain less than 20 dB, to ensure good matching. The predicted cancellation of the first loop is better than 27 dB, shown in Fig.3.16, for output power level 2 dB backed off from saturation.
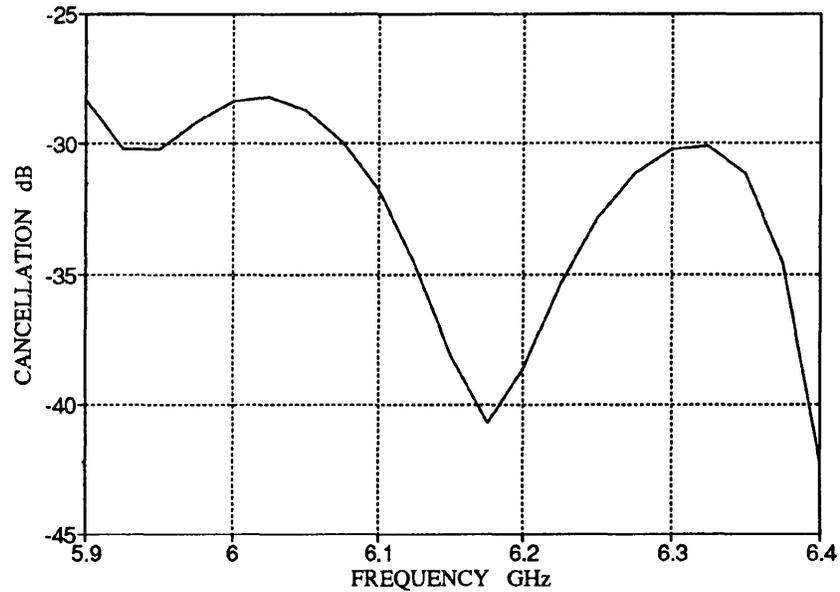
Fig.3.16 First loop cancellation

Parameter values for the optimized elements of the first loop are listed below.

<u>Directional coupler 14.5 dB</u> (parameters referring to Fig.3.9):
W = 2.08   mm
S = 0.43   mm
L = 8.24   mm

<u>Schiffman phase shifter 6°</u> (parameters referring to Fig.3.11):
W = 1.86   mm
S = 7.8   mm
L = 8.24   mm

<u>Microstrip delay line 562 ps</u>:
L = 113.66   mm

3.6.2 Second Loop Optimization

In the second loop the distortion caused by the main amplifier is cancelled by subtracting the error signal from the distorted signal. If the second loop is considered independently, as shown in Fig.3.17, and the phase and amplitude in that loop are properly balanced, any signal input to the circuit should be suppressed at the output. Thus, harmonic balance optimization for a single tone was again performed to take into account any nonlinear phase and gain characteristics of the auxiliary amplifier. The optimized elements were the delay line, the Schiffman phase shifter and the output coupler. The target of the optimization was minimum output power over the full operating bandwidth, with the restriction of a 20 dB return loss for the optimized components. The input power was chosen to present an input signal to the auxiliary amplifier at the same power level as the intermodulation products which would arise in the main amplifier at an output power 2 dB backed off from saturation. The predicted cancellation for the second loop is better than 20 dB as shown in Fig.3.18.
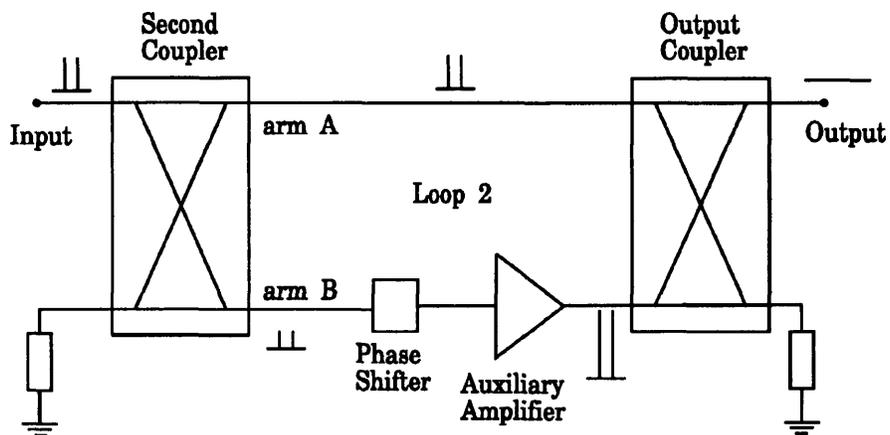
Fig.3.17 Second loop of feedforward linearizer

Parameter values for the optimized elements of the first loop are listed below.

Directional coupler 12 dB (parameters referring to Fig.3.9):
W = 1.86   mm
S = 0.28   mm
L = 8.41   mm

Schiffman phase shifter 118° (parameters referring to Fig.3.11):
W = 2.10   mm
S = 2.19   mm
L = 7.15   mm

Microstrip delay line 1.07 ns:
L = 216.37   mm
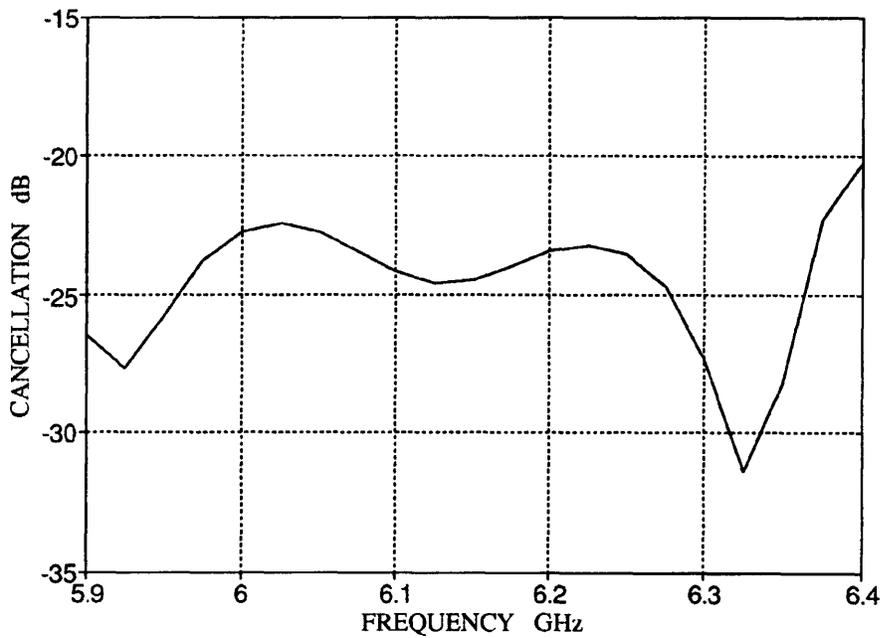
Fig.3.18 Second loop cancellation

3.7 Performance Evaluation of the Optimized Linearizer

After the optimization of the feedforward loops, two tone tests were performed, with and without linearization, to evaluate the improvement in the linearity of the power amplifier. Simulation results, considering up to third order terms, for 4 dB total output power backed off from saturation are shown in Fig.3.19. A range of carrier combinations are used to cover the full 5.9 to 6.4 GHz communication band. At least 20 dB reduction in the intermodulation product level is achieved.

Three tone tests were also carried out. Again an improvement of 20 dB in the level of the third order intermodulation products was apparent. Simulation results at 2 dB output power back off are presented in Fig.3.20. No further adjustments, other than the optimization described in section 3.6, were made to the phase and gain of the feedforward loops to achieve these results.

The effect of the band pass filter on the performance of the linearizer was also investigated. In order to do that the filter was replaced with a network which had the same response as the coupled line filter in band, so that the balance in second loop was not disturbed, but, also, allowed all the frequencies out of band to pass through. This network was simulated with an S parameter file included in Appendix 2. Three tone tests were simulated for various input power levels, with and without filtering the out-of-band harmonics. The carrier to intermodulation ratio (C/I) for both cases is shown in Fig.3.21, along with the C/I ratio for the unlinearized amplifier. At large signal conditions, where both amplifiers start behaving nonlinearly, the use of the filter leads to a further 5 dB improvement of the C/I ratio.

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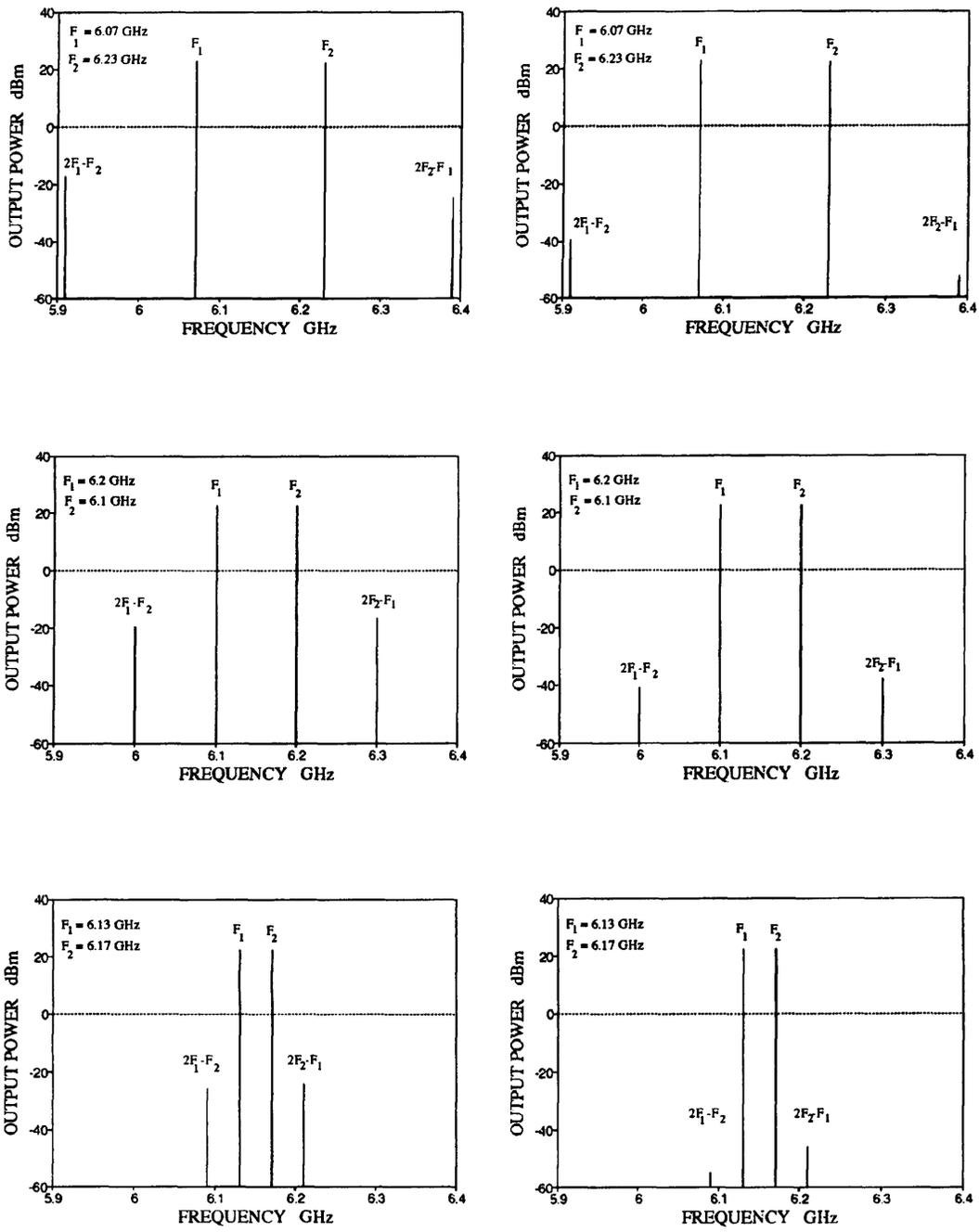
Unlinearized Output Power Spectra   Linearized Output Power Spectra

Fig.3.19 Output power spectra with and without linearization
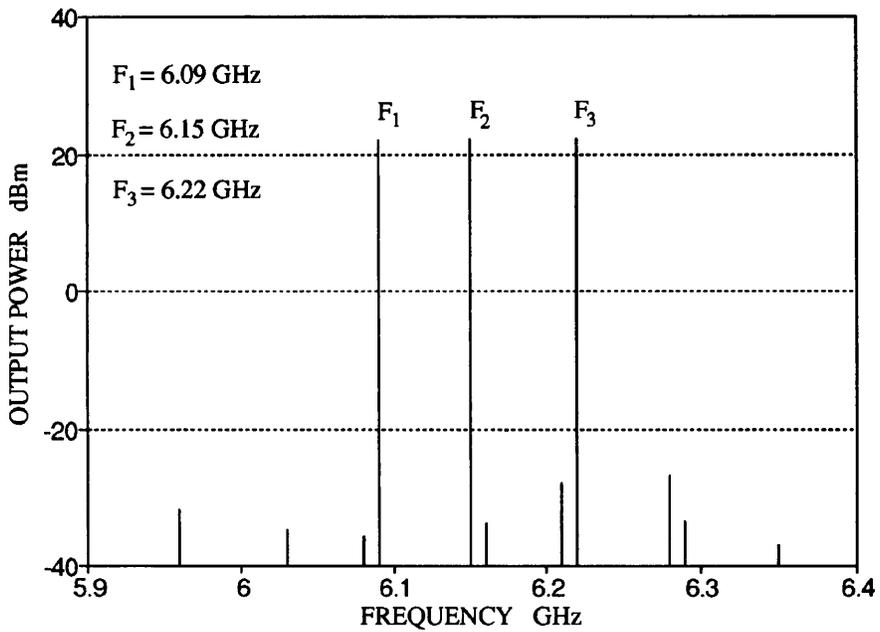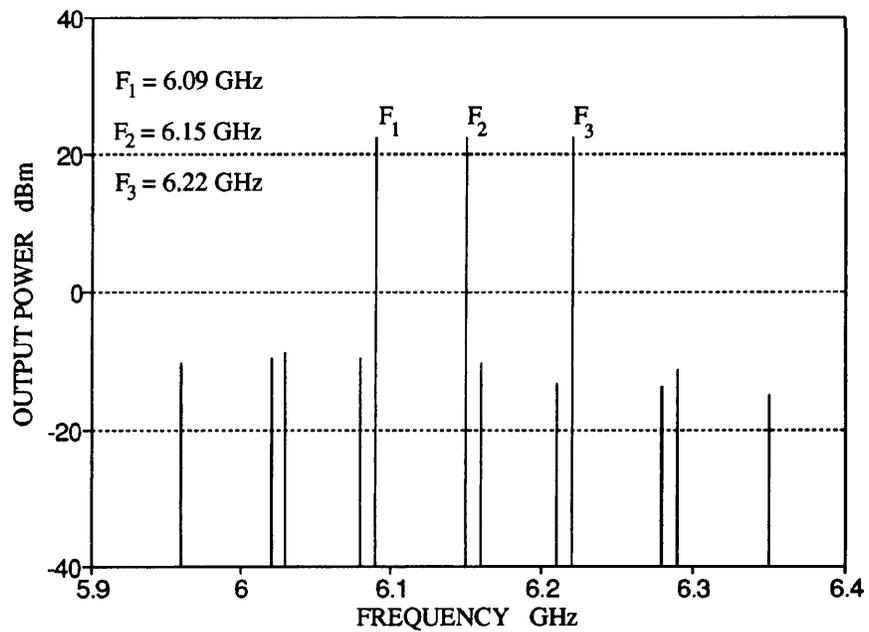
Fig.3.20 Output power spectra before and after linearization
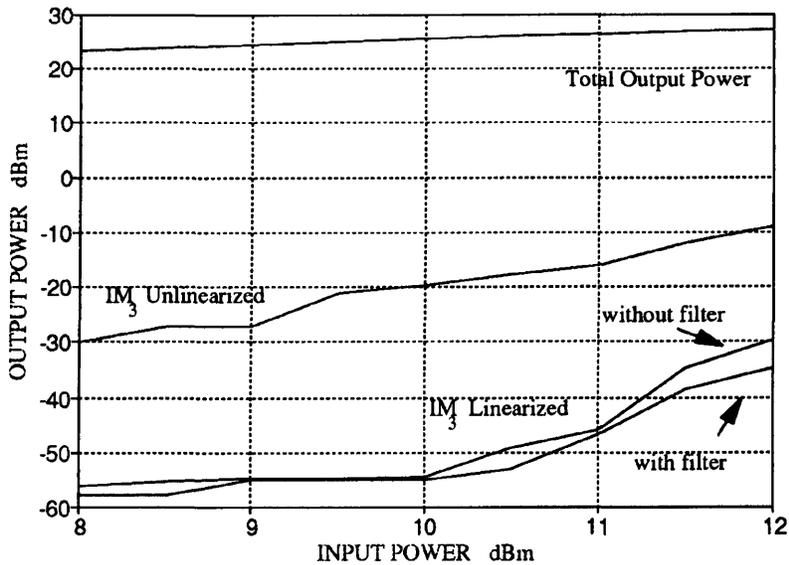
Fig.3.21 Output power as a function of input power

3.8 Conclusions

The design of a 6 GHz solid state feedforward linearizer has been presented in this chapter. With the optimization method employed, an improvement in the third order intermodulation products of at least 20 dB was possible over the 5.9 to 6.4 GHz frequency range. A range of carrier combinations were employed to test the performance of the linearizer showing that the intermodulation cancellation covered the full band and was independent of the carrier separation and position in the band.

It was, also, found that the out-of-band second order harmonics can deteriorate the performance of the linearizer especially at high output power levels. The microstrip filter employed at the input of the auxiliary amplifier effectively suppressed any nonlinear behaviour of this amplifier due to second order harmonics, allowing, thus, a further 5 dB improvement of the C/I ratio.

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Although the linearizer presented here was intended to be fabricated, difficulties in obtaining the chip devices did not allow the practical implementation of the design. Nevertheless, this design is used in the next chapter to investigate further the potentials of the feedforward linearization technique and evaluate the viability of linearizer configurations employing auxiliary amplifiers with different power ratings.

CHAPTER 4

CAD Assessment of the Feedforward Linearization Technique

4.1 Introduction

The 6 GHz feedforward linearizer described in the previous chapter achieved significant improvement in the performance of the power amplifier, indicating that the feedforward method is a very promising linearization technique. The method is further assessed in this chapter. In particular, the effect of amplitude and phase imbalance in the feedforward loops is examined in detail accounting, also, for the effect of auxiliary amplifier power rating.

It is generally appreciated that the auxiliary amplifier need not have as high power rating as the amplifier to be linearized because it only handles signals at lower power levels compared to the main amplifier[92]. However, an auxiliary amplifier with too low power handling capability will significantly distort the error signal and produce intermodulation products of its own. The feedforward system does not provide compensation for this additional distortion and the limit for the cancellation that can be achieved is governed by this additional distortion introduced due to the lower power handling capability of the auxiliary amplifier. The power rating of the auxiliary amplifier should, therefore, be carefully selected in order to obtain the highest efficiency and minimize cost without sacrificing the performance of the overall system. The effect of the auxiliary amplifier power rating on the performance of the linearizer was initially investigated employing CAD techniques[99]. The results are presented in section 4.2 for some feedforward linearizer configurations.

The operation of the feedforward linearizer is based on the vector subtraction of two signals at the output of each loop, as explained in section 3.6.2. Consequently, amplitude and phase imbalance in the feedforward loops leads to the deterioration of the system performance. This effect was evaluated employing analytical and CAD techniques. The analytical approach serves to develop an understanding of the relative importance of the different kinds of imbalances and the effect of the auxiliary amplifier power rating. A worst case theoretical analysis of the first loop effect is developed to produce equations which allow the design of feedforward linearizers for a specified circuit performance. CAD analysis of the feedforward linearizer's sensitivity to imbalances for various power ratings is, also, presented providing detailed predictions for some specific cases of interest[94].

The effect of the output coupling factor on the feedforward linearizer efficiency is, also, considered based on the analysis reported in [25]. The assumptions made in [25] are further discussed and a more realistic approach for the case of class A amplifiers is developed.

In overall, this chapter presents the investigation for developing a design strategy and provides the necessary design parameters that need to be incorporated in the initial design of a feedforward linearizer.

Finally, the advantages of feedforward linearization are assessed employing the computer aided designs of a linearizer, a balanced amplifier and an unlinearized amplifier[99]. Comparison of these configurations demonstrates that the feedforward linearization is the most efficient solution for systems where high linearity is essential.

4.2 Effect of the Auxiliary Amplifier Power Rating on the Linearizer Performance

The effect of the auxiliary amplifier power rating on the performance of the feedforward linearizer was investigated[99] employing the nonlinear CAD package Academy for the

feedforward linearizer presented in chapter 3. This was achieved by including two ideal gain elements[111], one at the input and the other at the output of the auxiliary amplifier. Variation of the gain, or loss, of these two elements allowed the saturation level of the amplifier to be varied whilst still maintaining the same gain and phase delay as the original amplifier and, therefore, the same amplitude and phase balance in the second loop. The results are presented in Fig.4.1, where it can be seen that for an auxiliary amplifier with a saturation level greater than 10 dBm, there is little difference in the performance of the linearizer up to approximately 22 dBm output power.
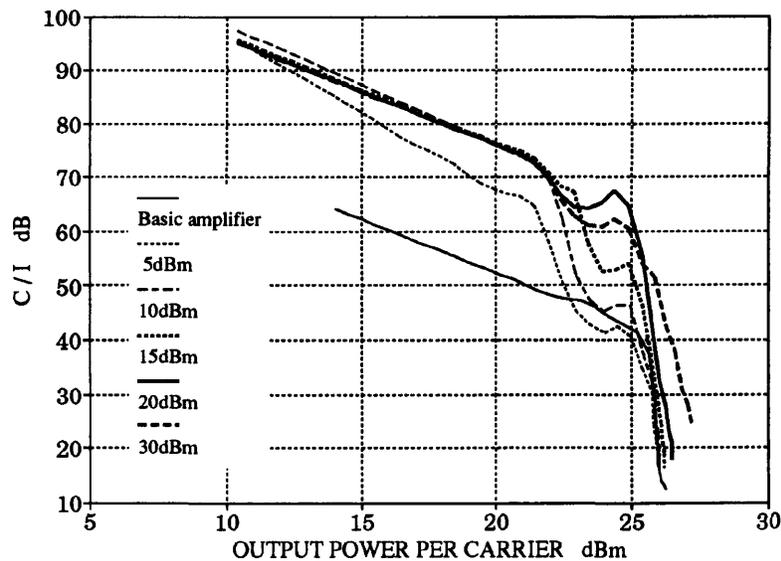
Fig.4.1 Effect of auxiliary amplifier power rating

The graph corresponding to a 5 dBm auxiliary amplifier in Fig.4.1 indicates that below 10 dBm level, the nonlinearity of the auxiliary amplifier significantly degrades the linearizer's performance. Furthermore, for linearized output power above 22 dBm, the error signal is sufficient to drive a 10 dBm auxiliary amplifier into nonlinear operation, leading to a rapid deterioration of the linearizer performance. As the auxiliary amplifier saturation level is increased from 10 dBm to 20 dBm, the output power level at which this rapid deterioration begins, gradually increases. Finally, no significant improvement

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is achieved by using the an auxiliary amplifier with a saturation level higher than 20 dBm.

The minimum value required for the auxiliary amplifier power rating depends upon the specified value for the carrier to intermodulation ratio. For example, a C/I ratio of 70 dB can be achieved at an output power of 22 dBm using an auxiliary amplifier with a saturation power level of only 10 dBm i.e. 20 dB lower than the saturation power level of the main amplifier. No further improvement is achieved by increasing the power rating further. In order to achieve that level of linearity the unlinearized amplifier must be backed off to 12 dBm per carrier. Therefore, in this case, an increase of approximately 1% in DC power consumption would lead to 10 dB increase in output power.

4.3 Analysis of the Sensitivity of Feedforward Linearizers to Phase and Amplitude Imbalance

The results described above demonstrate that, when optimal balance of amplitude and phase is achieved in the cancellation loops, the feedforward linearizer circuit succeeds in drastically reducing the intermodulation products in the main amplifier output. In particular, optimum balance of the first loop results in an error signal of sufficiently low power, permitting, thus, an auxiliary amplifier with a low power rating to be used without significantly affecting the performance of the feedforward system. In a practical system, however, the phase and amplitude balance may deviate from their optimum values due to changes in operating level, temperature or aging of the components used. Such changes in the operating conditions will affect the overall performance of the linearizer. Therefore, detailed analysis of the performance dependence on the phase and amplitude imbalance is necessary to fully evaluate the potentials of feedforward linearization.

A theoretical analysis is presented in the next sections to determine the distortion cancellation achievable by the feedforward linearizer as a function of the imbalances in each feedforward loop. Precise calculation of the distortion suppression is not possible unless the exact transfer characteristics of the main and the auxiliary amplifier are known for all the fundamental signals and their harmonics in the system. This, clearly, leads to a computer aided design approach. Nevertheless, a worst case theoretical analysis is attempted here. From a design point of view, the resulting equations and graphs set the safety margin for the auxiliary amplifier power rating, given a specific level of amplitude and phase imbalance in the first loop. Nonlinear simulation, employing harmonic balance, was also used to investigate the effect of imbalance on specific designs and evaluate the viability of lower power auxiliary amplifier configurations.

4.3.1 Theoretical Prediction of Cancellation in Independent Feedforward Loops

A feedforward linearizer circuit consists of two cancellation loops and its operation is based on the suppression, by anti-phase cancellation, of the signals of two paths at the output of each loop. The vector representation of the loop cancellation is shown in Fig.4.2, where the two cancelling signals have different amplitude levels A_1 and A_2 and the phase difference between them is $(180 - \theta)°$. The resultant vector ε is related to the phase error θ and the amplitude imbalance $\alpha = A_2/A_1$ by the equation:

$$|\varepsilon| = \sqrt{A_1^2 + A_2^2 - 2A_1A_2\cos\theta} = |A_1| \sqrt{1 + \alpha^2 - 2\alpha\cos\theta} \qquad 4.1$$

Therefore, the cancellation in dB achieved in each loop individually is:

$$\text{Cancellation} = 10 \log \frac{|\varepsilon|^2}{|A_1|^2} = 10 \log (1 + \alpha^2 - 2\alpha\cos\theta) \qquad 4.2$$

The relationship between the cancellation and the phase and amplitude error is shown in Fig.4.3. The characteristics shown in this figure are plotted using eq.4.2, with the

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amplitude imbalance α in dB as a parameter. Results similar to Fig.4.3 have been reported by other researchers in the past[69][91-92].

The plots show the level of cancellation that can be obtained for a given amplitude and phase balance within each of the feedforward loops. The frequency range over which this balance can be achieved is the bandwidth of the overall system. It is evident that the higher the desired cancellation and wider the bandwidth, the more difficult it is to meet the strict phase and amplitude requirements. Both the main and auxiliary amplifier should be designed for the required gain and phase flatness over the band of operation. In the case where the limits of amplifier design have been exhausted, alternative solutions may be sought to match the response of the two cancelling paths. In cable TV systems, were feedforward linearization has long been employed, gain and phase equalizers have been applied to achieve the required amplitude and phase balance [95-96]. At microwave frequencies though, matching is a critical
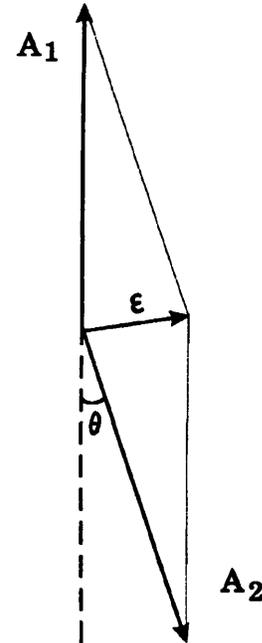
Fig.4.2 Vector cancellation

factor and control circuits are difficult to operate over wide bandwidths. In [70] in order to cover the 6 - 18 GHz frequency range   four finger Lange couplers were employed to tailor the phase characteristics of the amplifiers in the two loops resulting in 7 dB improvement of the third order intercept point of the main amplifier. In the 6 GHz linearizer design of chapter 3, Schiffman phase shifters[109] were used for the same reason maintaining over the 500 MHz bandwidth +/- 0.5 dB and +/- 2° balance in the first loop and +/-0.75 dB and +/-4° balance in the second loop. For these levels of imbalance the suppression of the cancelling signals is predicted from eq.4.2 to be 25 dB and 20 dB for the first and second loop respectively. The same order of cancellation was estimated after the optimization of the two loops in section 3.6 and was verified by two and three tone tests presented in section 3.7.
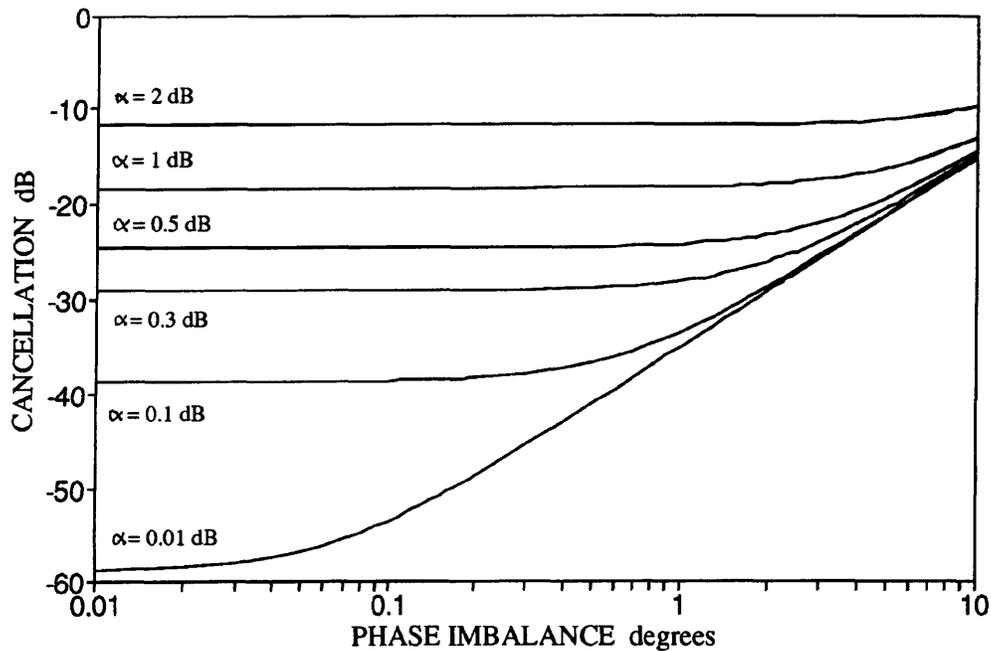
Fig.4.3 Cancellation as a function of phase and amplitude imbalance

4.3.2 Evaluation of the Effect of First Loop Imbalance

Imbalance in the first loop results in incomplete cancellation of the fundamental signals at the input of the auxiliary amplifier. This allows part of the input signal to be amplified by the auxiliary amplifier leading to further intermodulation products being produced by this amplifier. The level of the auxiliary amplifier intermodulation distortion will depend on the level of the suppressed carriers entering this amplifier and the linearity of the auxiliary amplifier. A theoretical analysis is developed in this section in order to determine the effect of first loop imbalance on the performance of the auxiliary amplifier. The analysis is based on the feedforward linearizer block diagram of Fig.4.4. For the distortion cancellation calculations, it is assumed that the main and the auxiliary amplifier exhibit only mild nonlinearities and, therefore, only the 3rd order

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intermodulation products are considered. The power is expressed in watts and the gain of the amplifiers, the coupling factors and transmission losses through the couplers and the losses in the delay lines are expressed as linear power ratios.
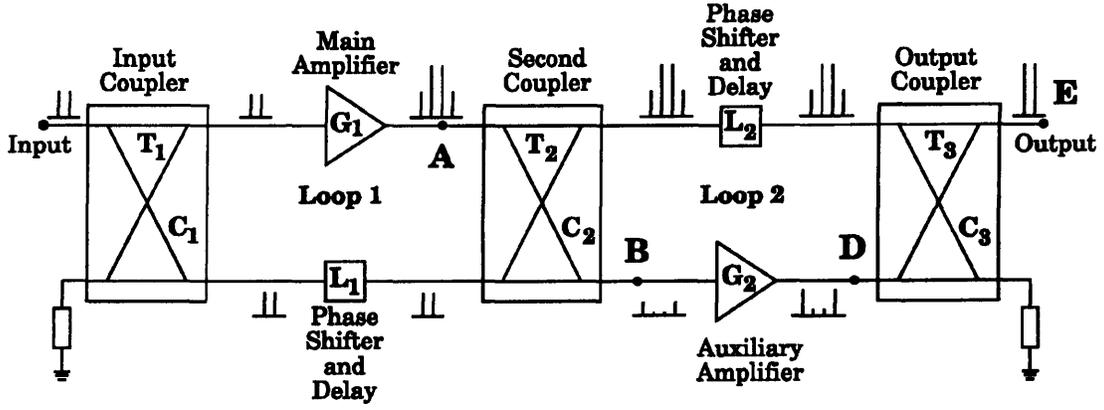
Fig.4.4 Feedforward linearizer block diagram

At the output of the main amplifier, at point A, the power $P_{A,carrier}$ per carrier and the power level $P_{A,IM1}$ of a 3rd order intermodulation product are:

$$P_{A, carrier} = P_{in} \, T_1 \, G_1 \qquad (4.3)$$

$$P_{A, IM_1} = P_{A, carrier} \left(\frac{I}{C} \right)_{1, A} \qquad (4.4)$$

where T_1 is the transmission loss of the input coupler, G_1 is the gain of the main amplifier, P_{in} is the input power per carrier and $(C/I)_{1, A}$ is the carrier to third order intermodulation ratio of the main amplifier for the specific output power level.

At point B, the carriers are suppressed and the level of the fundamental signals entering the auxiliary amplifier is:

$$P_{B, carrier} = P_{A, carrier} \, C_2 \, CANC_1 \qquad (4.5)$$

where C_2 is the coupling ratio of the second coupler and $CANC_1$ is the cancellation achieved in the first loop, defined, according to eq.4.2, as the power ratio of the

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suppressed signal over the signal corresponding to the open loop configuration.

At the output of the auxiliary amplifier, point D, both the intermodulation products and the residual carriers are amplified to:

$$P_{D, \text{ carrier}} = P_{B, \text{ carrier}} \; G_2 = P_{B, \text{ carrier}} \; CANC_1 \; C_2 \; G_2 \qquad (4.6)$$

$$P_{D, \text{ IM}_1} = P_{A, \text{ IM}_1} \; C_2 \; G_2 \qquad (4.7)$$

where G_2 is the gain of the auxiliary amplifier.

The residual carriers of eq.4.6 produce further third order intermodulation products IM_2 at the output of the auxiliary amplifier:

$$P_{D, \text{ IM}_2} = P_{D, \text{ carrier}} \left(\frac{I}{C} \right)_{2, D} \qquad (4.8)$$

where $(C/I)_{2, D}$ is the carrier to intermodulation ratio of the auxiliary amplifier for the specific output power level.

For mild nonlinearities, the power level of the third order intermodulation product of an amplifier P_{IM} is related to the output power per carrier P_{carrier} and the third order intercept point PI by eq.1.14[1]:

$$P_{IM} = 3 \; P_{\text{carrier}} - 2 \; PI \qquad dB \qquad (4.9)$$

Therefore, the carrier to intermodulation ratio (C/I) can be expressed in terms of output power and intercept point in linear form by:

$$\frac{C}{I} = \frac{P_{\text{carrier}}}{P_{IM}} = \left(\frac{PI}{P_{\text{carrier}}} \right)^2 \qquad (4.10)$$

Combining eqs 4.6, 4.7, 4.8 and 4.10 the intermodulation products introduced by the auxiliary amplifier are:

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$$P_{D, IM_2} = P_{D, IM_1} \left(\frac{PI_1}{PI_2} \right)^2 C_2^{\,2} \, G_2^{\,2} \, CANC_1^{\,3} \qquad (4.11)$$

where PI_1 and PI_2 are the intercept points of the main and the auxiliary amplifier respectively.

The level of the auxiliary amplifier intermodulation products depends on the linearity and the gain of the auxiliary amplifier, the coupling ratio of the second coupler and the level of cancellation achieved in the first loop. Increased phase and amplitude imbalance in this loop results in an increase of the $CANC_1$ term and a threefold increase of the auxiliary amplifier third order intermodulation products. This arises from the 3:1 slope of the third order intermodulation products, as explained in section 1.2.3.

The overall cancellation of the distortion at the output of the linearizer depends on the phase and amplitude balance that can be achieved in the second loop as expressed in eq.4.2 and the level of the intermodulation products of the auxiliary amplifier. In order to calculate precisely the deterioration of the second loop cancellation due to auxiliary amplifier nonlinearity the phase of the suppressed distortion signals and the phase of the auxiliary amplifier intermodulation products is required. This requires the exact transfer function of the two amplifiers to be known for the fundamental and the higher harmonics. A worst case analysis, however, is presented in the next section.

4.3.3 Design Equations and Graphs

The intermodulation products of the main and auxiliary amplifier can be considered independent for any practical system. Thus, the auxiliary amplifier distortion will be added to the output distortion with arbitrary phase. The worst case situation is when the intermodulation products introduced by the auxiliary amplifier are added in phase to the suppressed distortion signals at the output of the linearizer. Then, the level of the

intermodulation products at the output of the linearizer (point E in Fig.4.4) will be:

$$P_{E, IM} = \left(\sqrt{P_{E, IM_1}} + \sqrt{P_{E, IM_2}} \right)^2 = \left(\sqrt{P_{E, IM_1}} + \sqrt{P_{D, IM_2} \, C_3} \right)^2 \quad (4.12)$$

where C_3 is the coupling ratio of the output coupler and $P_{E, IM1}$ is the power level of the intermodulation products of the main amplifier which are suppressed at the output due to the second loop feedforward correction. Their power level will depend on the cancellation that can be achieved in the second loop. According to eq.4.2 the cancellation that can be achieved in the second loop alone is defined as the power ratio of the suppressed signal over the power of the same signal for the open loop configuration:

$$CANC_2 = \frac{P_{E, IM_1}}{P_{A, IM_1} \, T_2 \, L_2 \, T_3} \quad (4.13)$$

where T_2 and T_3 are the transmission loss of the second and output coupler respectively and L_2 is the loss of the delay line of the second loop.

Similarly, the effective cancellation of the overall feedforward linearizer is the power ratio of the level of the intermodulation products at the output of the linearizer over the power level of the intermodulation products for the open loop configuration:

$$CANC_{eff} = \frac{\left(\sqrt{P_{E, IM_1}} + \sqrt{P_{E IM_2}} \right)^2}{P_{A IM_1} \, T_2 \, L_2 \, T_3} \quad (4.14)$$

The amplitude imbalance α_2 in the second loop, defined as the power ratio of the two paths gain, is:

$$\alpha_2 = \frac{T_2 \, L_2 \, T_3}{C_2 \, G_2 \, C_3} \quad (4.15)$$

Substituting eq.4.7, eq.4.11 eq.4.13 and eq.3.15 in eq.3.14 the cancellation of the intermodulation products at the output of the linearizer is given by:

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$$CANC_{eff} = \left(\sqrt{CANC_2} + \sqrt{CANC_1^{\ 3} \left(\frac{PI_1}{PI_2} \right)^2 \frac{1}{C_3^2} \frac{T_2^{\ 2} L_2^{\ 2} T_3^{\ 2}}{\alpha_2^{\ 3}}} \right)^2 \Rightarrow \qquad (4.16)$$

$$CANC_{eff} = 20 \ \log \left(\sqrt{CANC_2} + \sqrt{CANC_1^{\ 3} \left(\frac{PI_1}{PI_2} \right)^2 \frac{1}{C_3^2} \frac{T_2^{\ 2} L_2^{\ 2} T_3^{\ 2}}{\alpha_2^{\ 3}}} \right) \ dB$$

The terms $CANC_2$ and $CANC_1$ depend on the amplitude and phase balance that can be achieved in each feedforward loop independently and they can be calculated from eq.4.2:

$$CANC_1 = 10 \ \log \ (\ 1 + \alpha_1^{\ 2} - 2\alpha_1 \cos\theta_1 \ ) \qquad (4.17)$$

$$CANC_2 = 10 \ \log \ (\ 1 + \alpha_2^{\ 2} - 2\alpha_2 \cos\theta_2 \ ) \qquad (4.18)$$

where α_1, θ_1 and α_2, θ_2 are the amplitude and phase imbalance in the first and second loop respectively.

Equations 4.16 - 4.18 govern the cancellation that can be achieved with the feedforward correction as a function of phase and amplitude imbalance in both loops. The first term of eq.4.16 depends on the balance that can be achieved in the second loop and is further quantified by eq.4.18. The second term of eq.4.16, however, does not only depend on the balance that can be achieved in the first loop as expressed in eq.4.17 but, also, on other parameters of the linearizer circuit. In particular, it depends on the linearity of the auxiliary amplifier compared to the linearity of the main amplifier, the loss ($T_2 \ L_2 \ T_3$) through the output power path and the coupling ratio C_3 of the output coupler. An auxiliary amplifier with low linearity or too loose coupling at the output coupler increases the effect of the amplitude and phase imbalance in the first loop. Furthermore, eq.4.16 shows that phase and amplitude imbalances in the first loop which are expressed by the term $CANC_1^{\ 3}$ result in a threefold reduction of the overall cancellation, as opposed to the phase and amplitude imbalances in the first loop which directly affect the cancellation through the $CANC_2$ term. Therefore, for high values of phase and

amplitude imbalance the cancellation achievable with the feedforward linearizer is determined by the cancellation $CANC_1$ obtained in the first loop. This dependence will be more critical if the auxiliary amplifier linearity and the coupling ratio of the output coupler are low. The particular importance of the auxiliary amplifier linearity and the output coupler will be further discussed in sections 4.4 and 4.5 of this chapter.

The above equations 4.16 - 4.18 permit the calculation of the distortion suppression by the feedforward linearizer circuit for a given amplitude and phase imbalance in both loops and for specific auxiliary amplifier linearity and output coupling ratio. Graphs for various levels of imbalance and specific circuit parameters can be obtained using these equations in order to allow the design of feedforward linearizers for the desired performance.

The suppression of the third order intermodulation products achieved at the output of the linearizer as a function of phase and amplitude imbalance in both the feedforward loops is shown in Fig.4.5 - Fig.4.9 for some cases of interest. The plots in these figures show the effective cancellation as a function of the first loop phase imbalance with the first loop amplitude imbalance and the second loop amplitude and phase imbalance as parameters. The cancellation achieved in the second loop alone is, also, provided to indicate the level of the overall cancellation in the case where the first loop had been perfectly balanced. The second and output couplers were assumed to have coupling ratios of at least 10 dB and, therefore, the loss $(T_2 \ L_2 \ T_3)$ through the output power path was estimated to be 1.5 dB. The output coupler was assumed to have coupling ratio $C_3 = 10$ dB which is the lower value for directional couplers that can be easily fabricated on microstrip. The effective cancellation at the output of the linearizer was calculated for one auxiliary amplifier with the same third order intercept point as the main amplifier and one auxiliary amplifier with 10 dB lower intercept point. In order to evaluate the significance of the auxiliary amplifier linearity, the cancellation achieved by both auxiliary amplifiers is shown in the same graph.

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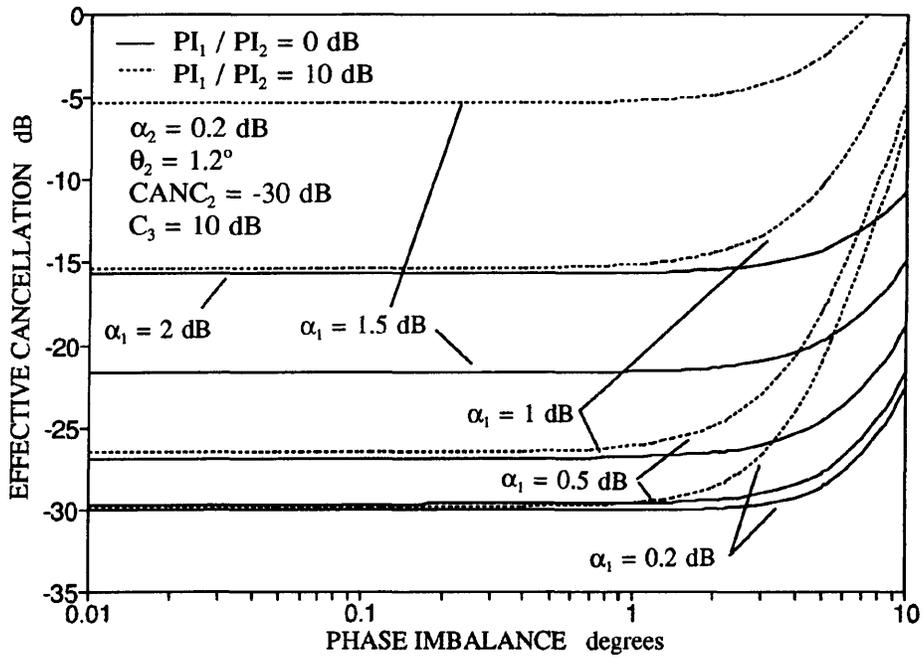
Fig.4.5 Effective cancellation for 30 dB cancellation in the second loop

PI$_1$ / PI$_2$ = 0 dB
PI$_1$ / PI$_2$ = 10 dB

α_2 = 0.2 dB
θ_2 = 1.2°
CANC$_2$ = -30 dB
C$_3$ = 10 dB

α_1 = 2 dB
α_1 = 1.5 dB
α_1 = 1 dB
α_1 = 0.5 dB
α_1 = 0.2 dB

EFFECTIVE CANCELLATION   dB

PHASE IMBALANCE   degrees
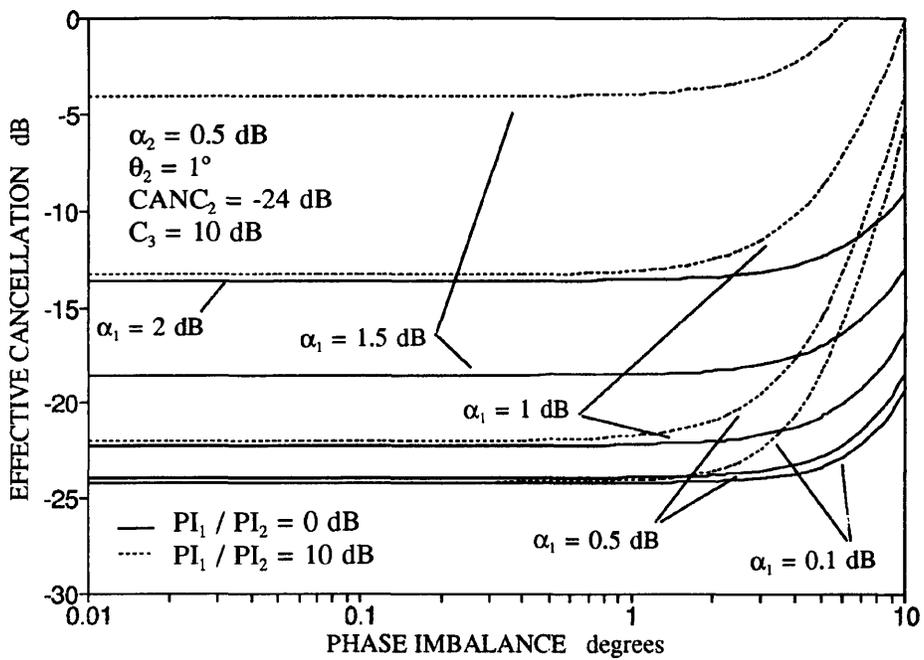
Fig.4.6 Effective cancellation for 24 dB cancellation in the second loop

α_2 = 0.5 dB
θ_2 = 1°
CANC$_2$ = -24 dB
C$_3$ = 10 dB

α_1 = 2 dB
α_1 = 1.5 dB
α_1 = 1 dB
α_1 = 0.5 dB
α_1 = 0.1 dB

PI$_1$ / PI$_2$ = 0 dB
PI$_1$ / PI$_2$ = 10 dB

EFFECTIVE CANCELLATION   dB

PHASE IMBALANCE   degrees

108
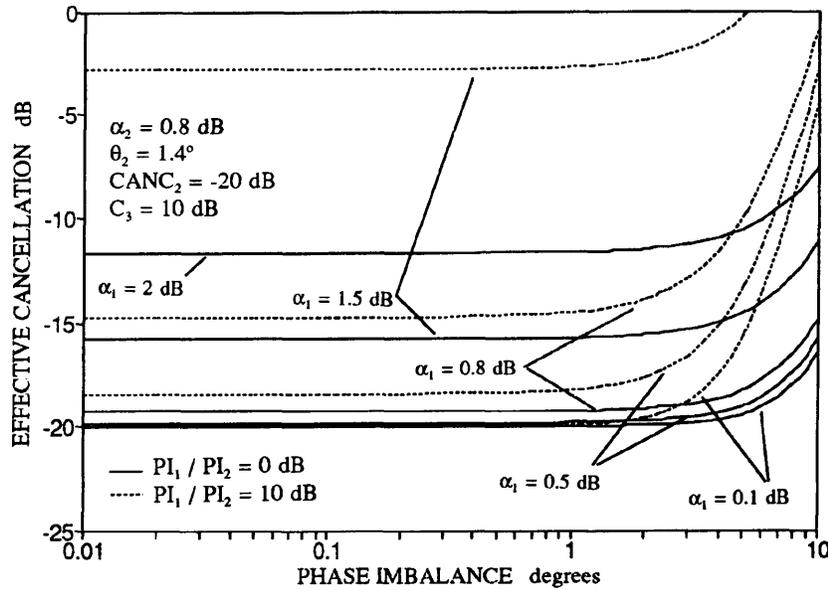
Fig.4.7 Effective cancellation for 20 dB cancellation in the second loop

The effective cancellation for a 30 dB, 24 dB and 20 dB cancellation in the second loop is shown in Fig.4.5, Fig.4.6 and Fig.4.7. Compared to Fig.4.3, the slope of the cancellation curves as a function of first loop phase imbalance is much steeper than the curves of Fig.4.3. and the deterioration of the cancellation with amplitude imbalance is more severe for the first loop imbalance. This is the result of the first loop cancellation term being raised to the third power in eq.4.16. This effect is more severe when the auxiliary amplifier with intercept point 10 dB lower than the main amplifier is used. In this case, for significantly high amplitude and/or phase imbalance the effective cancellation is less than 0 dB implying that the intermodulation products introduced by the auxiliary amplifier are higher than the main amplifier distortion signals.

If the auxiliary amplifier has the same intercept point as the main amplifier and the same level of imbalance is considered in both loops, the effective cancellation is practically equal to the second loop cancellation. For the 30 dB cancellation, Fig.4.5, first loop imbalance of $\alpha_1 = 0.2$ dB and $\theta_1 = 1.2°$ leads to 29.9 dB effective cancellation. For the 24 dB second loop cancellation, Fig.4.6, the effective cancellation becomes

23.8 dB with first loop imbalance α_1 = 0.5 dB and θ_1 = 1°. In the case of 20 dB cancellation in the second loop, Fig.4.7, the same imbalance of α_1 = 0.8 dB and θ_1 = 1.4° in the first loop allows the effective cancellation to be 19.2 dB. However, when the auxiliary amplifier with 10 dB lower intercept point than the main amplifier is employed, the effective cancellation significantly deviates from the second loop cancellation value. For the same level of imbalance as before, the 30 dB second loop cancellation leads to an effective cancellation of 29.4 dB, for the 24 dB case the cancellation is reduced to 21.7 dB and for the 20 dB case the effective cancellation drops to 14.3 dB.
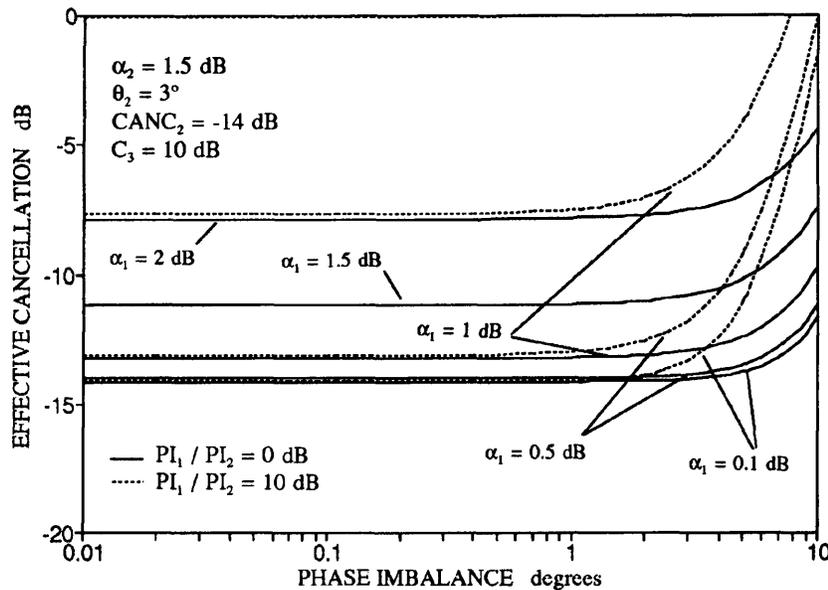
Fig.4.8 Effective cancellation for 14 dB cancellation in the second loop

The effective cancellation of the linearizer for 15 dB and 11 dB second loop cancellation is shown in Fig.4.8 - 4.9. For these levels of phase and amplitude imbalance the sensitivity of the linearizer to high first loop imbalance is more clear. For the same level of amplitude and phase imbalance in both loops the overall cancellation is mostly determined by the first loop imbalance. For the second loop cancellation of 14 dB the phase and amplitude imbalance is α_2 = 1.5 dB and θ_2 = 3°. The same imbalance in the

first loop results in an effective cancellation of only 10.8 dB. Similarly for 11 dB second loop cancellation the effective cancellation is reduced to 5.4 dB for $\alpha_1 = 2$ dB and $\theta_1 = 5.4°$ imbalance. With the "10 dB" auxiliary amplifier the cancellation level is above 0 dB for the same level of imbalance, implying that no reduction of the intermodulation distortion has been achieved.
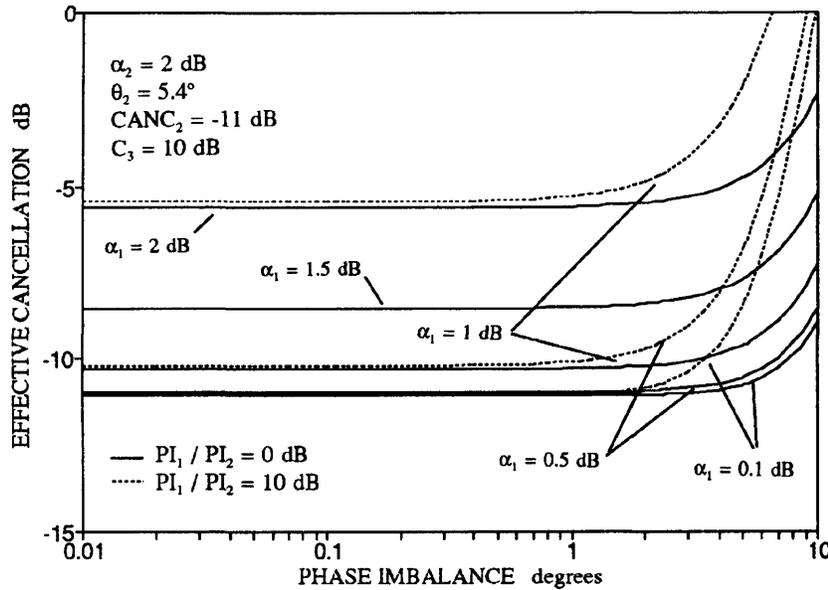
Fig.4.9 Effective cancellation for 11 dB cancellation in the second loop

4.3.4 CAD Study of High Efficiency Configurations

If the first loop is not properly balanced the residual carriers that enter the second loop can drive the auxiliary amplifier into nonlinear operation. Generation of further intermodulation products within this amplifier deteriorates the performance of the linearizer, as expressed in eq.4.16. The level of the intermodulation products generated by the auxiliary amplifier depends on the level of the residual carriers, i.e. the level of cancellation in the first loop, and the linearity of this amplifier. Thus, the higher the power rating of the auxiliary amplifier the higher the imbalance in the first loop that can be tolerated. However, an auxiliary amplifier with high power rating compared to the main amplifier leads to reduced efficiency linearizers. In section 4.2 the effect of the

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auxiliary amplifier rating was investigated for optimum balance in the feedforward loops. In this section the performance of feedforward linearizers employing auxiliary amplifiers with various power ratings is investigated for cases were the phase and amplitude balance deviates from the optimum values. Extra phase and amplitude imbalance was, therefore, introduced in each loop to simulate changes in the operating conditions and evaluate the viability of high efficiency linearizer configurations[94].

The effect of the phase and amplitude imbalance on the performance of high efficiency feedforward linearizer configurations has been investigated using the simulated linearizer design described in chapter 3. Phase or gain imbalance has been introduced in one arm of the feedforward loops using ideal phase and gain elements included in the software element library[111]. The auxiliary amplifiers with different power levels were obtained the same way as in section 4.2. At the output of the linearizer, the C/I ratio was calculated for two carriers at frequencies F = 6.1 GHz and F = 6.2 GHz. The results presented here are calculated for the third order intermodulation product at frequency F = 6 GHz. It should be noted that the main amplifier of the 6 GHz feedforward amplifier was designed for highly linear power and its intercept point and saturation level are 46 dBm and 30 dBm respectively. The auxiliary amplifier, however, is not as linear and its intercept point is only 33 dBm , 10 dB higher than its saturation level. Thus, although the power rating of the auxiliary amplifier is only 7 dB lower than the main amplifier its intercept point is 13 dB lower. Consequently, the deterioration of the effective cancellation due to first loop imbalance should be even more severe than predicted in Fig.4.5 - 4.9 for the low linearity amplifier.

Sensitivity to First Loop Imbalance

The effects of phase and amplitude imbalance in the first loop upon the performance of the simulated linearizer with various auxiliary amplifier power ratings are shown in Figs.4.10-4.15. To provide an indication of the magnitude of the deterioration, plots of the performance characteristics of the optimally balanced linearizer with the 23 dBm auxiliary amplifier, and of the amplifier without linearization have been included.

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Fig.4.10 shows the effect of increased amplitude imbalance upon the linearizer design when the auxiliary amplifier has a saturation power level of 20 dBm. For an imbalance of 0.5 dB, the performance of the linearizer is degraded but it is still better than that of the unlinearized amplifier at low output power. Above 22 dBm the performance deteriorates rapidly due to the auxiliary amplifier being driven into saturation. When the imbalance is increased to 1 dB the performance is dramatically degraded as expected.
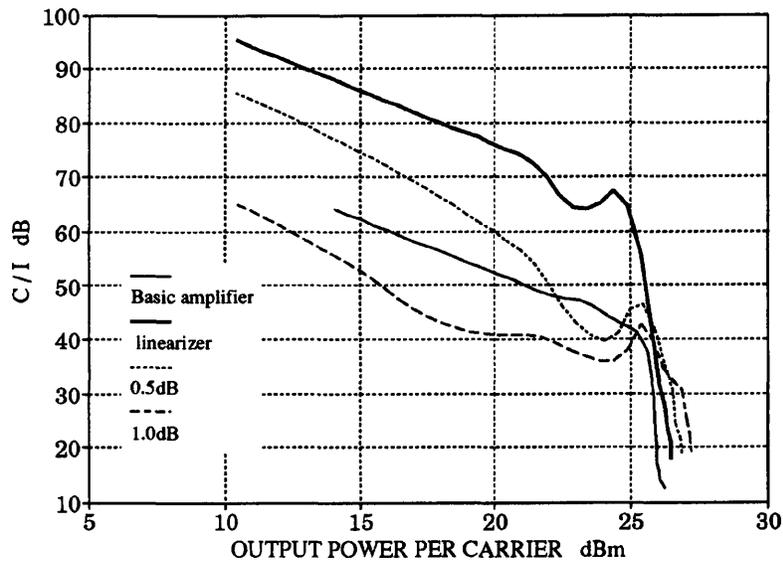
Fig.4.10 Effect of amplitude imbalance for a 20 dBm auxiliary amplifier

Fig.4.11 shows the effect of a 1 dB imbalance in the first loop for various auxiliary amplifier saturation levels. As expected the higher the amplifier saturation power level, the less sensitive the circuit is to the effects of the imbalance. A sharp improvement in the linearizer performance occurs at an output power of 25.5 dBm. At this power level, compression of the main amplifier gain compensates for the introduced imbalance, resulting in reduction in the power of the error signal and the corresponding improvement in the linearizer performance. There are two possible cases which result in an amplitude imbalance of the same magnitude. The first occurs when the transmission coefficient of the first loop cancellation path containing the amplifier is

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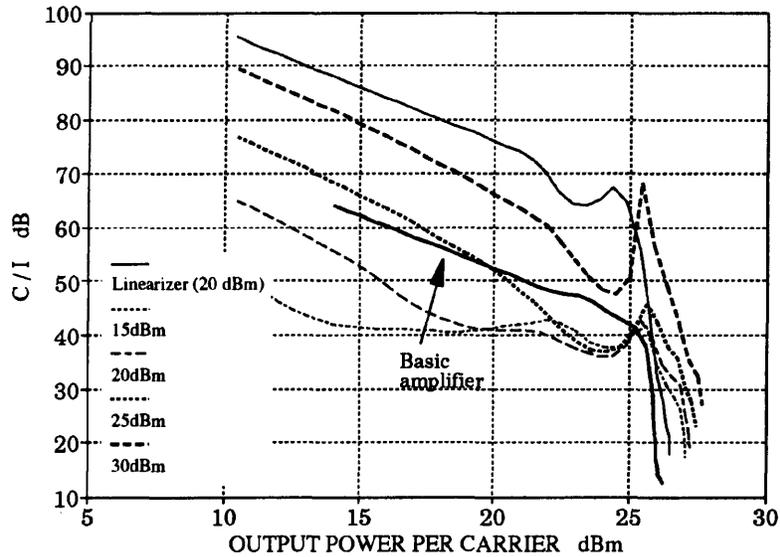
Fig.4.11 Effect of 1 dB imbalance in the first loop

greater than that of the input reference path. This was the imbalance used to generate the plots in Fig.4.11. The second case is obtained from the opposite condition, i.e. when the transmission coefficient of the amplifier path is the lower of the two. The effects of both cases on the performance of the linearizer, with a 30 dBm auxiliary amplifier, are shown in Fig.4.12. The improvement at 25.5 dBm, as would expected, occurs only when the main amplifier path has the higher coefficient. It can also be seen that at output power greater than 15 dBm, the plots diverge. This difference in the predicted performance results from the comparatively lower intermodulation products present in the error signal when the transmission coefficient of the path containing the main amplifier is reduced.

The effect of phase imbalance upon the performance of the linearizer is shown in Fig.4.13 - Fig.4.15. Fig.4.13 shows the sensitivity of the performance of the linearizer to the variation in the phase imbalance when the auxiliary amplifier has a saturation power level of 20 dBm. It can be seen that while a phase imbalance of 2.5° degrades the performance of the linearizer at low power levels, for output power greater than 25 dBm

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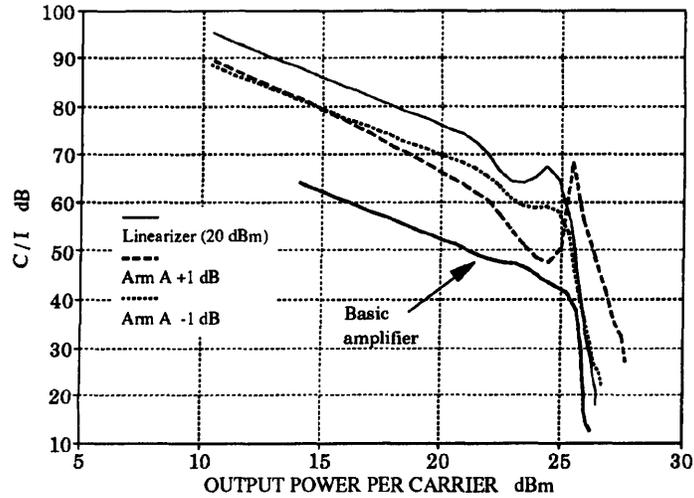
Fig.4.12 Effect of +/- 1 dB amplitude imbalance in the first loop

the performance improves slightly. This improvement is due to the imbalance compensating for phase distortion introduced by the two amplifiers as they operate near to saturation. The plots show that for phase imbalance greater than approximately 5° the performance of the linearizer deteriorates below that of the unlinearized amplifier.
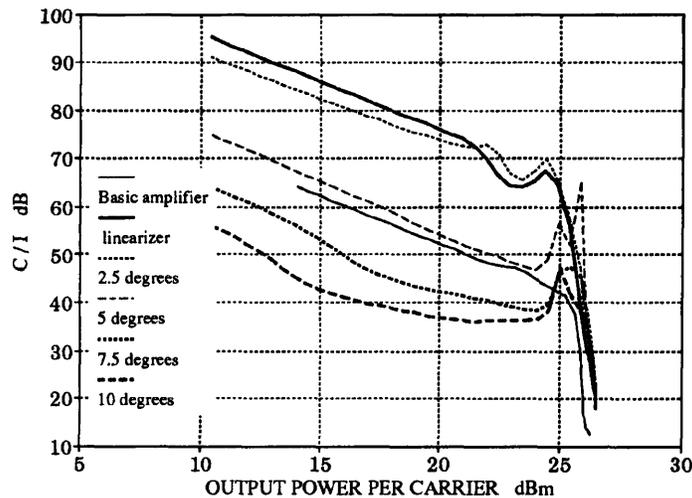
Fig.4.13 Effect of phase imbalance for a 20 dBm auxiliary amplifier

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Fig.4.14 shows the sensitivity to phase imbalance when the saturation power rating of the auxiliary amplifier is increased to 30 dBm. As predicted from the theoretical analysis of the previous section, the effect of the imbalance is not as dramatic as in the case of the lower power amplifier considered above.
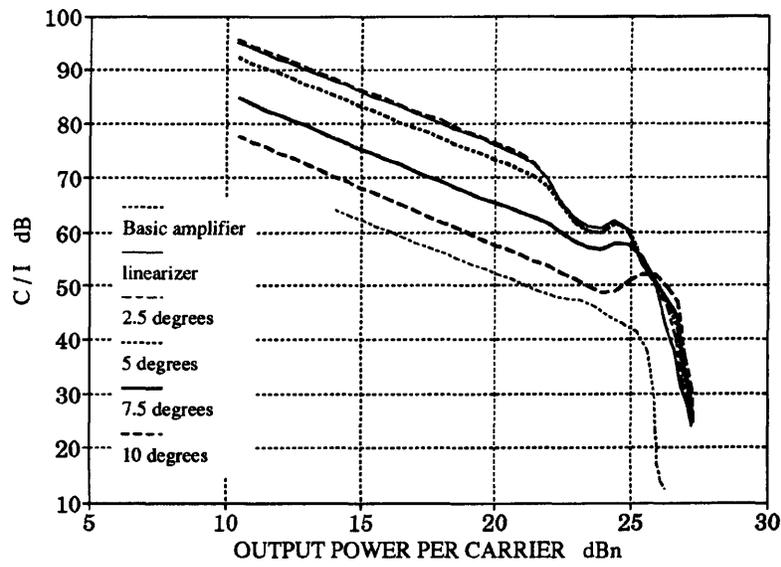
Fig.4.14 Effect of phase imbalance for a 30 dBm auxiliary amplifier

The effect of $5°$ imbalance upon the performance of the linearizer with different auxiliary amplifier power ratings is shown in Fig.4.15. As expected the lower the power rating of the amplifier, the more sensitive the linearizer is to the imbalance. For the 30 dBm case the imbalance has little effect. When a 15 dBm amplifier is considered the performance of the main amplifier is degraded by the linearizer circuit as a result of the auxiliary amplifier driven into highly nonlinear operation at very low level of linearizer output power.

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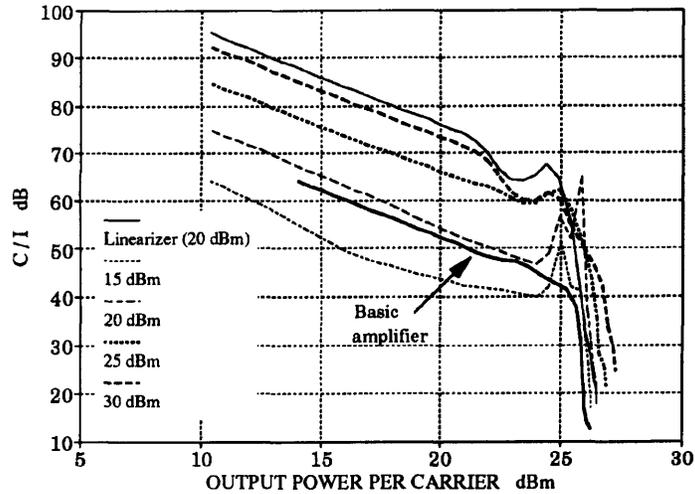
Fig.4.15 Effect of 5° imbalance in the first loop

Sensitivity to Second Loop Imbalance

Phase or amplitude imbalance in the second loop results directly in imperfect cancellation of the main amplifier distortion, irrespective of the linearity of the auxiliary amplifier. The following graphs (Figs 4.16 to 4.17) show the effect of phase and amplitude imbalance in the carrier to intermodulation levels achieved by the simulated linearizer. Again, an indication of the magnitude of the deterioration is provided by the inclusion of the results for the optimally balanced linearizer with the 23 dBm auxiliary amplifier, and for the basic unlinearized amplifier in both plots.

Fig.4.16 shows the effect of a 10° phase imbalance introduced into the arm of the second loop containing the auxiliary amplifier. The results show the effect this imbalance has on the linearizer performance when the amplifier has saturation power levels of 20 dBm and 30 dBm. It can be seen that the degradation in the performance that results from the phase imbalance is independent of the auxiliary amplifier power rating. Comparison of these plots with the results for 5° imbalance in the first loop, Fig.4.15, clearly demonstrate that the linearizer performance is less sensitive to phase imbalance in the second loop.

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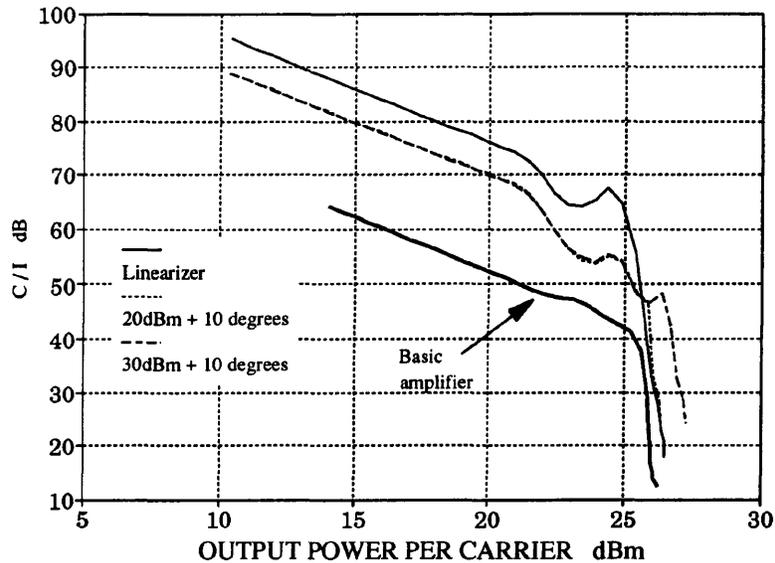
Fig.4.16 Effect of 10° imbalance in the second loop

The effect of 1 dB amplitude imbalance in the second loop using two different auxiliary amplifier power ratings is shown in Fig.4.17. As with phase imbalance in this loop, the deterioration in the linearizer performance caused by the amplitude imbalance is independent of the auxiliary amplifier power rating. Again, comparison of the results with those of the same imbalance in the first loop, shown in Fig.4.11, demonstrates that the linearizer is less sensitive to imbalance in the second loop.

The results obtained from the above CAD analysis confirm the theoretical predictions of sections 4.3.1 - 4.3.3 and demonstrate that an auxiliary amplifier with lower power rating than the main amplifier can be employed in a practical feedforward circuit provided that phase and amplitude imbalances in the first loop are kept below certain levels. The design aspects of the auxiliary amplifier are further discussed in the next section based on the outcome of the above CAD and theoretical analysis.

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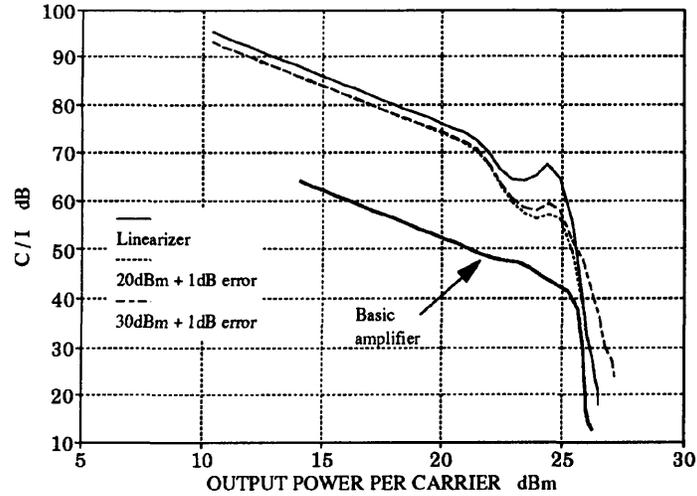
Fig.4.17 Effect of 1 dB imbalance in the second loop

4.4 Further Considerations on the Design Criteria of the Auxiliary Amplifier

The auxiliary amplifier is a critical component for the performance of the feedforward linearizer. Its phase and gain flatness over the frequency range of interest dominate the amplitude and phase imbalance across the band determining, thus, the distortion cancellation that can be achieved in the second loop of the feedforward linearizer as described in section 4.3.1. Furthermore, the power rating of this amplifier directly affects the efficiency of the linearizer system determining at the same time the degree of imbalance in the first loop that can be tolerated without significantly deteriorating the overall system performance. The power rating of the auxiliary amplifier should, therefore, be carefully selected in order to achieve the highest efficiency and minimize cost without sacrificing the performance of the overall feedforward system.

The effect of the auxiliary amplifier nonlinearity upon the performance of the linearizer is described by eq.4.16. Fig.4.18 to Fig.4.22 show the effective cancellation achieved by

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the feedforward linearizer for various cancellation levels achieved in each feedforward loop. The ratio of the main amplifier and the auxiliary amplifier intercept points in dB is used as the parameter characterizing each curve. The output coupler is again assumed to be 10 dB and the loss $(T_2 \; L_2 \; T_3)$ through the output power path was estimated to be 1.5 dB. The same amplitude imbalance α_2 as in Fig.4.5 - 4.9 was used for the second loop cancellation calculation.

The graphs of Fig.4.18 - Fig.4.22 determine the level of cancellation that is required for each feedforward loop in order to achieve the desired performance when a specific auxiliary amplifier is employed in the linearizer circuit. Each loop should be designed to maintain this cancellation over the frequency range of interest.

Fig.4.18 - Fig.4.22 show that, in order to achieve a specific performance, the required level of cancellation is not the same for both loops. As expected from eq.4.16 this is more clearly demonstrated for high levels of imbalances. From Fig.4.22, 11 dB cancellation in both loops results in less than 5 dB effective cancellation even if an auxiliary amplifier with the same linearity as the main amplifier is employed. Generally, the effective cancellation remains close to the second loop cancellation value if an auxiliary amplifier with the same linearity as the main amplifier is employed and the first loop cancellation is better than 20 dB. Such high cancellation levels in the first loop ensure that the auxiliary amplifier does not produce significant distortion. However, if lower linearity auxiliary amplifiers are employed the requirements for the first loop cancellation become more strict. For example, for a 20 dB effective cancellation using the "10 dB" auxiliary amplifier, with the second loop cancellation being 20 dB, the first loop must achieve a 30 dB cancellation, as shown in Fig.4.20. Alternatively, the same order of effective cancellation can be achieved with a 30 dB cancellation in the second loop and 21 dB cancellation in the first loop. Several combinations of the parameters in Fig.4.18 - Fig.4.22 can be selected to obtain the desired performance. In practice, however, it is easier to obtain higher levels of cancellation in the first loop than in the second loop. This arises from the high gain of the auxiliary amplifier. As discussed in

section 3.2, the gain of the auxiliary amplifier is approximately equal to the gain of the main amplifier plus the coupling ratio of the output coupler. Therefore, the auxiliary amplifier will require more gain stages than the main amplifier resulting in longer delay elements in the second loop. Consequently, the phase balance achieved in the first loop will be better, especially if wide bandwidths are required. In the linearizer presented in chapter 3, for example, the cancellation achieved in the first loop was 25 dB whilst the second loop alone achieved only 20 dB cancellation.

At large signal condition the auxiliary amplifier does not only produce further intermodulation products but its phase and amplitude characteristics change nonlinearly with input power level. Theses changes in amplitude and phase response will, consequently, upset the balance in the second loop. However, this kind of distortion can be compensated for, if the gain and phase of one path in the second loop is rearranged for large signal operation. The linearizer described in chapter 3 was optimised for operation at 2 dB from saturation power as explained in the relevant section 3.6. From Fig.4.1. it can be seen that the C/I ratio peaks at 25 dB output power per carrier implying that the linearizer was optimized for optimum amplitude and phase balance at this power level.
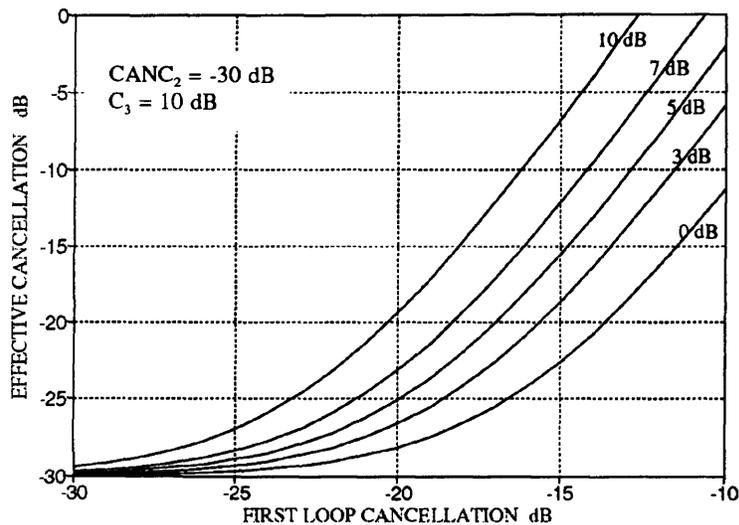
Fig.4.18 Effective cancellation for 30 dB second loop cancellation
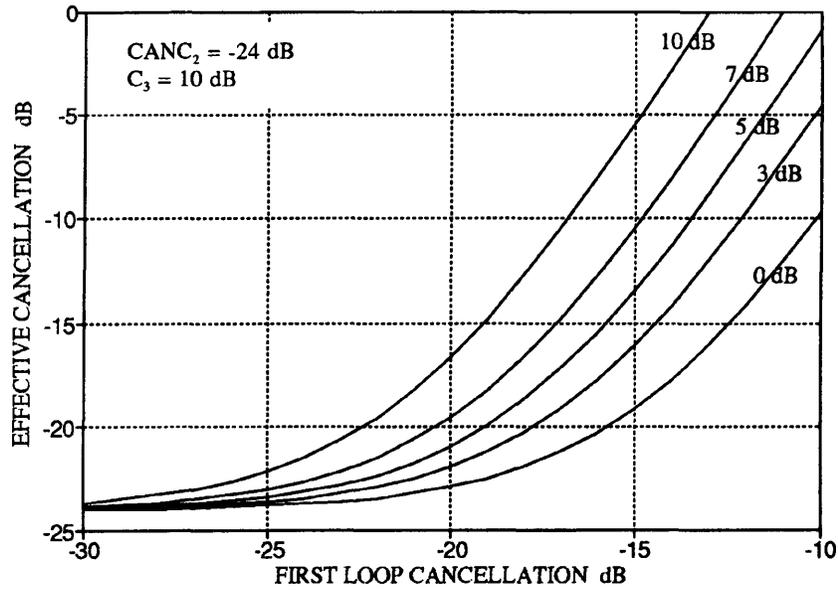
Fig.4.19 Effective cancellation for 24 dB second loop cancellation
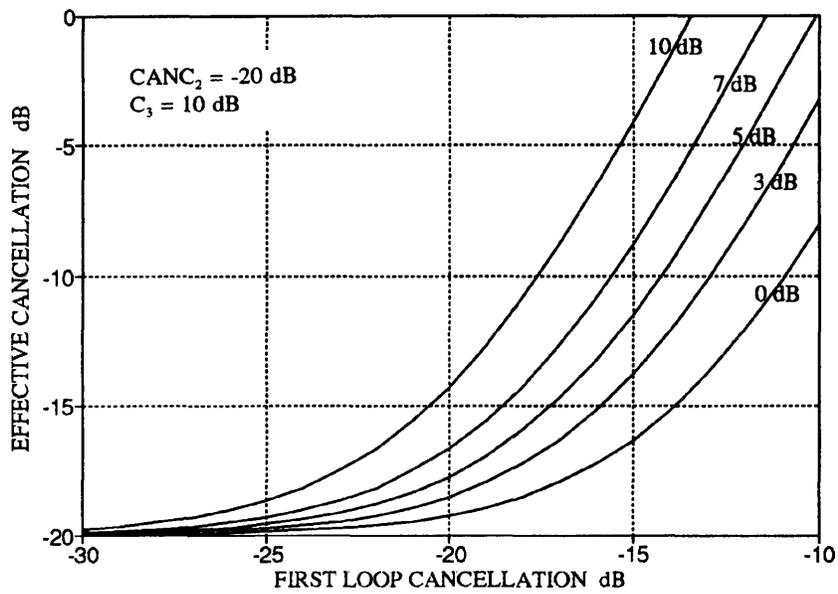
Fig.4.20 Effective cancellation for 20 dB second loop cancellation
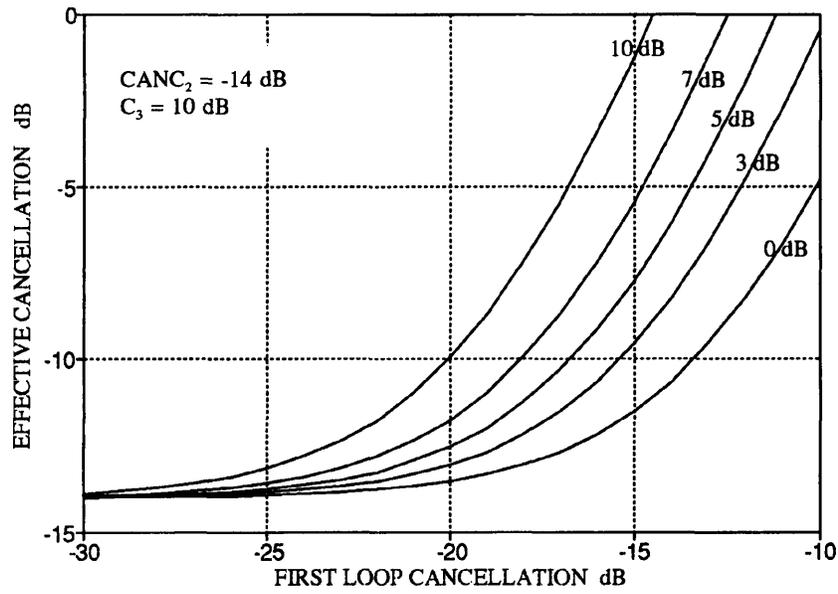
Fig.4.21 Effective cancellation for 14 dB second loop cancellation
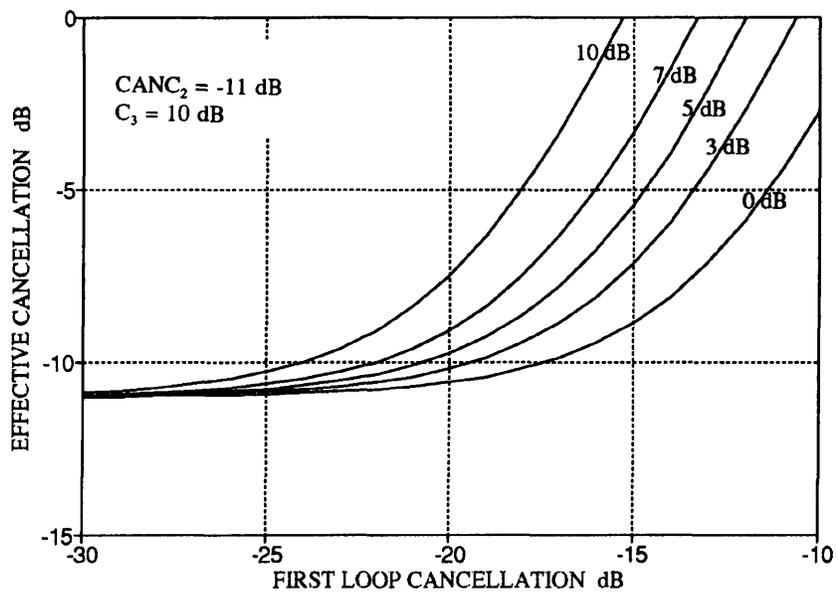
Fig.4.22 Effective cancellation for 11 dB second loop cancellation

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One important observation from the CAD analysis of section 4.3.4 is that, for high levels of imbalance in the first loop and low auxiliary amplifier power ratings, this amplifier reaches saturation before the main amplifier does. This possibility is not taken into account in the theoretical analysis of sections 4.3.2 and 4.3.3 because only mild nonlinearities were considered. It is, however, possible for the auxiliary amplifier to saturate before the main amplifier depending on the power level of the residual carriers and the power rating of the auxiliary amplifier. Nonlinear operation of the auxiliary amplifier results in reduced distortion cancellation but saturation of this amplifier totally ruins the feedforward correction and endangers the safe operation of this amplifier. Therefore, the possibility of auxiliary amplifier saturation should be taken into account in the design of the linearizer circuit.

The output power of the auxiliary amplifier due to the residual carriers is given by eq.4.6. Expressed in dB this equation becomes :

$$P_{D,carrier} = P_{B,carrier} + G_2 = P_{A,carrier} + C_2 + G_2 + CANC_1 \quad dB \qquad (4.19)$$

Substituting eq.4.15 the above equation becomes:

$$P_{D,carrier} = P_{A,carrier} + CANC_1 - C_3 + (T_2 + L_2 + T_3 - \alpha_2) \quad dB \qquad (4.20)$$

The losses $(T_2 + L_2 + T_2 - \alpha_2)$ should be in the range of 1-3 dB. Therefore, the power at the output of the auxiliary amplifier is approximately equal to the output power of the main amplifier plus the difference between the coupling ratio C_3 and the cancellation achieved in the first loop. For the linearizer to work it should be :

$$P_{sat2} \geq P_{A, carrier} + CANC_1 - C_3 + (T_2 + L_2 + T_3 - \alpha_2) \quad dB \qquad (4.21)$$

where P_{sat2} is the saturation power of the auxiliary amplifier. The above equation sets the limit for the coupling ratio of the output coupler given a specific level of first loop cancellation (i.e. a specific degree of imbalance in the loop) and the desired operating power level of the main amplifier. The effect this has on the output coupler is further discussed in the following section.

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4.5 Specification of the Output Coupler

The design criteria for the output coupler of the feedforward linearizer are based on the requirements for system efficiency. As mentioned in section 3.2, there is a trade off between the requirement for low loss through this coupler and the need to keep the gain of the auxiliary amplifier low. The higher the gain of the auxiliary amplifier the more stages are required and, most important, the higher the output power this amplifier has to deliver. Eq.4.21 sets the limit for the coupling ratio C_3 so that the auxiliary amplifier does not saturate for a given operating power level of the main amplifier. Furthermore, it would be desirable to operate the linearized main amplifier over its whole operating range up to the saturation level. This, of course, depends on the specific communication system requirements for the lower allowable C/I level. However, feedforward linearization could provide several dB improvement of the C/I and, in some cases, allow the linearized amplifier to operate at power levels as high as the saturation level. When this is the case, care should be taken in the choice of the auxiliary amplifier power rating so that the main amplifier saturates first. For such a system eq.4.21 becomes:

$$P_{sat_2} \geq P_{sat_1} + CANC_1 - C_3 + (T_2 + L_2 + T_3 - \alpha_2) \quad dB \qquad (4.22)$$

Fig.4.23 shows the allowable difference between the saturation power levels of the auxiliary amplifier and of the main amplifier as a function of the cancellation achieved in the first loop with the coupling ratio C_3 of the output coupler as a parameter. The term $(T_2 L_2)/\alpha_2$ was assumed to be 1 dB and the transmission loss through the output coupler T_3 expressed as a power ratio is:

$$T_3 = 1 - C_3 \quad \Rightarrow \quad T_3 = 10 \log (1 - C_3) \quad dB \qquad (4.23)$$

From Fig.4.23 is evident that the lower the saturation power of the auxiliary amplifier the higher the coupling ratio of the output coupler should be for a specific level of cancellation achieved in the first loop, in order to ensure that the auxiliary amplifier does not saturate. Furthermore, high coupling ratios for the output coupler improve the performance of the feedforward linearizer as expressed in eq.4.16. However, the

coupling ratio C_3 cannot be increased very much because this results in high loss in this coupler and reduced overall efficiency of the linearizer.
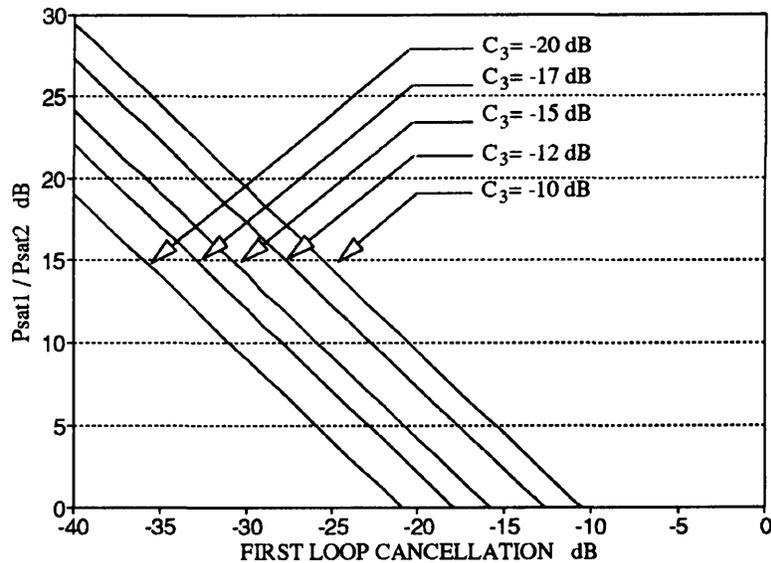
Fig.4.23 Auxiliary amplifier saturation power level as a function of cancellation

The effect of the output coupling factor on the feedforward linearizer efficiency has been considered by Kenington [25]. The author produced equations to calculate the overall linearizer efficiency as a function of output coupler coupling ratio and produced graphs for the case of linearizers employing class A and class C amplifiers. This analysis predicted that values between 10 dB and 26 dB have very little effect on the system efficiency when calculated using class A amplifier with 25 % efficiency and 35 dB C/I. However, from Fig.4.23 it can be seen that a linearizer with a 20 dB output coupler and first loop cancellation of -20 dB would require an auxiliary amplifier with the same saturation power as the main amplifier. This would significantly reduce the efficiency of the system. The result of [25] arises from the assumptions made in the analysis of the problem.

The equations in [25] assume perfect cancellation of the carriers in the first loop so that only the intermodulation products of the main amplifier determine the output power of

the auxiliary amplifier. Although this could be true for a class C main amplifier linearized over a narrow frequency range, it is hardly the case in a practical system, employing class A amplifiers with a wide bandwidth. For a class A amplifier carrier to intermodulation ratios of the order of 35 dB should be expected for output power up to 1 dB compression point and that was the value used in [25]. The cancellation that can be achieved in the first loop, however, will not necessarily be as low as that especially when a wide bandwidth is required. It is, therefore, evident that the residual carriers are the signals that dominate the power rating of the auxiliary amplifier in most practical systems where class A amplifiers are employed. Therefore, a more realistic approach for the case of class A amplifiers is presented next, where the output power of the auxiliary amplifier is the sum of the power level of the suppressed carriers and the main amplifier intermodulation products. In the following analysis the notation of section 4.3 is used and Fig.4.4 should be considered.

The output power $P_{D,2}$ of the auxiliary amplifier is:

$$P_{D,2} = P_{A, carrier} \, CANC_1 \, C_2 \, G_2 + P_{A, carrier} \left(\frac{I}{C} \right)_{1, A} C_2 \, G_2 \qquad (4.24)$$

Using eq.4.5, eq.4.6, eq.4.7 and eq.4.15 the auxiliary amplifier output power is:

$$P_{D,2} = P_{A, carrier} \left(CANC_1 + \left(\frac{I}{C} \right)_{1, A} \right) \frac{T_2 \, L_2 \, T_3}{\alpha_2} \frac{1}{C_3} \qquad (4.25)$$

According to eq.1.5 the overall RF to DC efficiency of the system n_{eff}, is defined as:

$$n_{eff} = \frac{P_{E, carrier}}{P_{DC_1} + P_{DC_2}} \qquad (4.26)$$

where P_{DC1} and P_{DC2} is the DC power consumed by the main and auxiliary amplifier respectively in order to amplify one carrier.

The RF to DC efficiencies of the main and the auxiliary amplifier n_1 and n_2 are:

$$n_1 = \frac{P_{A,\,carrier}}{P_{DC_1}} \qquad (4.27)$$

$$n_2 = \frac{P_{D,\,2}}{P_{DC_2}} \qquad (4.28)$$

Substituting equations 4.27, 4.28 and 4.25 into eq.4.26 and rearranging gives:

$$n_{eff} = \frac{n_1\, n_2\, P_{A,\,carrier}\, T_2\, L_2\, T_3}{P_{A,\,carrier}\, n_2 + P_{A,\,carrier}\left[CANC_1 + \left(\frac{I}{C}\right)_{1,\,A}\right]\frac{T_2\, L_2}{\alpha_2}\frac{T_3}{C_3}} \qquad (4.29)$$

$$n_{eff} = \frac{n_1\, n_2\, T_2\, L_2\, (1 - C_3)\, C_3}{n_2\, C_3 + n_1\left[CANC_1 + \left(\frac{I}{C}\right)_{1,\,A}\right]\frac{T_2\, L_2}{\alpha_2}(1 - C_3)} \qquad (4.30)$$

The above equations permit the calculation of the optimum coupling ratio for a given main and auxiliary amplifier efficiencies, a specific third order intermodulation distortion level and the lower cancellation allowable in the first loop.

The RF to DC efficiency characteristics as a function of the coupling ratio C_3 with the first loop cancellation as a parameter are shown in Fig.4.24. Class A amplifiers with 25% efficiency and C/I of 35 dB were considered. The loss $T_2\, L_2$ was assumed to be 1.5 dB and a 0.5 dB amplitude imbalance was allowed for the second loop. It is evident from Fig.4.24 that the higher the cancellation achieved in the first loop the higher the coupling ratio of the output coupler that provides the best efficiency.

The efficiency of the overall linearizer is reduced to 16% compared to the 25% efficiency of the main amplifier. In [25] the RF to DC efficiency of the class A configuration was calculated to be more than 20% for the same main amplifier. This

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difference is due to the assumptions made in [25] that the carriers are perfectly suppressed in the first loop and that no loss is introduced by the second coupler and the delay line in the second loop. Furthermore, both the above analysis and [25] make the assumption that the efficiency of the auxiliary amplifier remains constant and does not decrease as the gain increases. In practice, high coupling ratios require increased auxiliary amplifier gain leading to more stages configurations. This would degrade the auxiliary amplifier RF to DC efficiency and would require longer and, therefore, more lossy delay lines. It should also be noted that a lower power auxiliary amplifier is expected to have higher efficiency because of the limitations of the microwave transistors at high frequencies and high output power levels. However, it is very difficult to quantify the above parameters and, therefore, they were not taken into account in the preceding analysis for the optimum coupling ratio. Thus, the results of Fig.4.24 should be considered indicative and not precise.
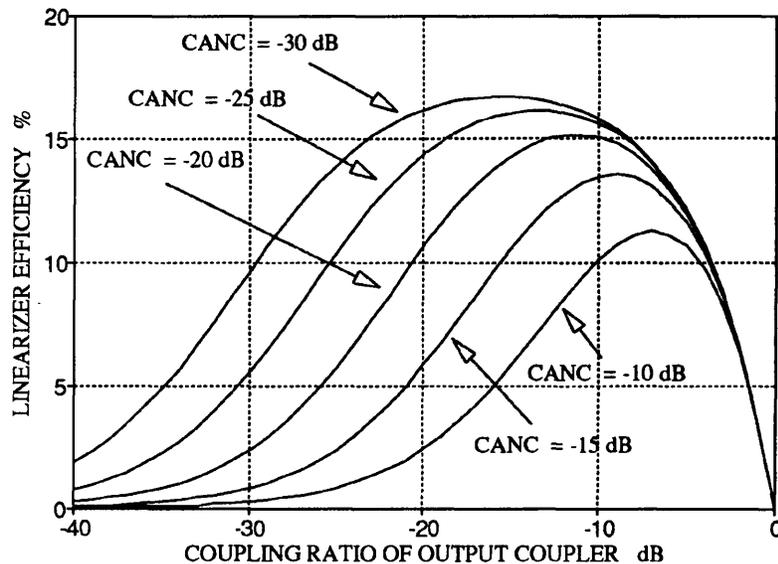
Fig.4.24 Efficiency of linearizer as a function of output coupling ratio

The choice of the coupling ratio of the output coupler will, also, be influenced by practical implementation issues like the ease of fabrication. In general, coupling ratios

lower than 10 dB are usually implemented in microstrip with directional couplers which are easy to fabricate. However, coupling ratios higher than 10 dB require such high tolerances for the width and the spacing of the coupled lines (Fig.3.9) that make the directional coupler configuration an impractical approach. When difficult coupling ratios are required other coupling circuits have to be considered. One solution could be the branch line configuration of [112], although difficulties in obtaining the required inductance and capacitance values should, also, be taken into account.

4.6 Comparison of Feedforward Linearization with Conventional Combining Techniques

The feedforward linearization technique provides a circuit approach which requires an additional amplifier and that, often, leads to questions about the overall system efficiency. As seen from Fig.4.24 the main amplifier efficiency is significantly reduced due to the linearizer circuit. Furthermore, the power rating of the linearized amplifier is not significantly increased as opposed to the power combining of two amplifiers which leads to a straightforward 3 dB improvement in the saturation level of an amplifier. Such a comparison, however, is misleading since multi-carrier systems are rarely, if ever, operated at the amplifier's saturation level. In general, amplifiers in such systems will be operated several dB below saturation level to achieve a minimum required difference between the carrier and the intermodulation product power levels.

In order to evaluate the advantages of feedforward linearization, the carrier to intermodulation ratio as a function of output power was calculated employing the nonlinear simulator of Academy, for the following cases[99]:

- The main amplifier unlinearized as described in section 3.3.1
- The linearized main amplifier as described in section 3.7
- Two amplifiers like the main amplifier used in a balanced amplifier configuration as described in section 1.5.6.

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The results are presented in Fig.4.25 indicating that, for output power of up to approximately 26 dBm, the highest C/I ratio is achieved by the feedforward linearizer circuit. Only as the amplifiers approach saturation does the balanced amplifier achieve a higher C/I ratio. Thus, for a system requiring a carrier to intermodulation ratio better than 40 dB, the feedforward linearizer configuration is the most efficient system.
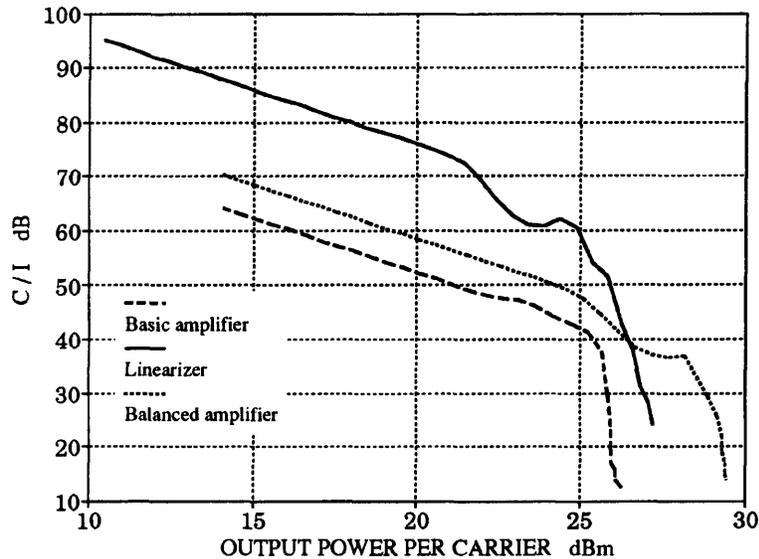
Fig.4.25 Comparison of feedforward linearizer with a balanced amplifier

The advantages of feedforward linearization are better appreciated when considering communication systems with strict requirements for low intermodulation distortion. If a system, for example, were to operate with a C/I ratio of greater than 60 dB, which is often the case in satellite communications, then the basic amplifier would need to be backed off to an output power per carrier of 16 dBm. The balanced amplifier would need to be backed off to 19 dBm. In comparison, the feedforward linearizer could be operated much nearer to its saturation power level, for at approximately 25 dBm output power per carrier.

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4.7 Conclusions

A theoretical analysis and CAD study of the feedforward linearization technique has been presented in this chapter. The design equations produced from the analytical approach permit the calculation of a feedforward linearizer distortion suppression for specific circuit parameters. It has, also, been shown that the linearizer is much more sensitive to imbalances in the first feedforward loop than to imbalances in the second loop. This arises from the third order intermodulation products properties. The power rating of the auxiliary amplifier plays an important role in this phenomenon and should, therefore, be carefully selected in the design of the linearizer.

The CAD study of high efficiency configurations verified the theoretical predictions and showed that lower power auxiliary amplifier configurations are a practical solution provided that the imbalances in the first feedforward loop remain below certain limits. If the imbalances in this loop are too high or an auxiliary amplifier with too low a power rating is employed the feedforward linearizer could deteriorate, rather than improve the performance of the power amplifier. This could be the case if the auxiliary amplifier saturates before the main amplifier does. To avoid this and ensure safe operation of the circuit eqs 4.21 or 4.22 must, always, be satisfied.

One important parameter for the correct and efficient operation of the feedforward linearizer is the coupling ratio of the output coupler. The importance of this element has been discussed in detail and an analysis based on [25] has been presented. The resulting equation and graph indicates that coupling ratios in the range of 10 dB to 15 dB are required if the cancellation achieved in the feedforward loops is of the order of 20 dB.

The efficiency of the technique was evaluated employing the Computer Aided Designs of the 6 GHz linearizer , the main amplifier alone and a balanced amplifier. For a system with requirements for high linearity the feedforward amplifier was proved to be the most efficient configuration.

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The effectiveness of the method will be further evaluated with the practical implementation of a 6 GHz feedforward linearizer system. The design, construction and testing of this experimental linearizer is further discussed in the remainder of this thesis.

CHAPTER 5

Design Fabrication and Experimental Testing of the Linearizer Components

5.1 Introduction

This chapter describes the design, construction and performance evaluation of the components used in the experimental linearizer. The linearizer was designed to operate over the 5.9-6.4 GHz frequency band providing 1 W output power. The initial objective was to achieve 20 dB improvement in the intermodulation distortion of the linearized amplifier.

In order to preserve the system efficiency the output coupler was specified, according to Fig.4.24, to have a coupling ratio in the range 10 - 15 dB. Furthermore, the auxiliary amplifier was designed to have half the power rating of the main amplifier. In order to be able to investigate the performance of the feedforward linearizer at high output power levels up to saturation, care was taken to prevent the auxiliary amplifier saturating before the main amplifier did. From eq.4.22 for a 3 dB difference in the two amplifiers' power rating, a 2 dB loss in the output path and a coupling ratio C_3 of 10-15 dB, the required cancellation in the first loop is 11-16 dB. However, the requirement for 20 dB effective cancellation of the overall linearizer sets more strict requirements on the first loop cancellation. As explained in section 4.4, in order to achieve a specific performance the required cancellation is not the same for both the feedforward loops. From Figs 4.18 - 4.22 it is evident that, for an auxiliary amplifier with 3 dB lower power rating than the main amplifier and a first loop cancellation of 25 dB, the effective cancellation is determined by the cancellation achievable in the second loop. As has

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been discussed in the same section, the cancellation that can be obtained in the first loop is, generally, better than the second loop cancellation. It was, therefore, decided to aim for 25 dB cancellation in the first loop and 20 dB cancellation in the second loop. The results obtained from the simulated linearizer of chapter 3 indicate that these requirements are realistic for the bandwidth of interest and could result in the desired 20 dB effective cancellation for the overall linearizer.

Having decided that a cancellation of 25 dB is required for the first loop, the constraints for the imbalances in that loop are set by eq.4.17. From Fig.4.3. +/-1° phase imbalance and +/-0.5 dB amplitude imbalance has to be maintained in the first loop to obtain that level of cancellation. The main amplifier was, therefore, designed for maximum gain and phase ripple of that order. According to eq.4.18, for a second loop cancellation of 20 dB the required maximum phase and amplitude imbalance are +/-1.4° and +/-0.8 dB respectively. Therefore, when designing the auxiliary amplifier it was aimed to keep the gain and phase ripple below these levels.

The linearizer was constructed employing MIC technology and each component was fabricated and tested before the overall design and assembly of the feedforward system. Both amplifiers were designed on microstrip employing the Fujitsu family FLC packaged GaAs FETs and were fabricated using the facilities at Ferranti, Poynton. In order to ease the testing procedure both the main and the auxiliary amplifiers were designed to have the same dimensions so that the same measurement jig could be used. The test jig was an aluminium case with SMA coaxial ports and its dimensions were designed to prevent propagation of waveguide modes at frequencies below 7 GHz.

Different coupler configurations were considered for use in the experimental linearizer. The practical evaluation of these couplers is presented in section 5.4. Practical implementation difficulties for a coupled lines microstrip filter are, also, discussed in section 5.5. The HP 85107A network analyzer system was used for the measurements of the gain, phase response and return loss of the various circuit designs.

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5.2 Main Amplifier

5.2.1 Design of the Main Amplifier

The main amplifier was designed for operation over the 5.9 - 6.4 GHz frequency band with 30 dBm output power. Taking into account a reduction of gain in the range 3-5 dB due to the linearizer circuit, the gain of the main amplifier was specified to be at least 20 dB. The devices employed, with their output power and associated gain, are shown in Fig.5.1. The relevant data sheets are included in Appendix 1.

Input — | **FLC 053WG** Gain 8 dB Output Power 25.5 dBm | — | **FLC 091WF** Gain 7.5 dB Output Power 27.5 dBm | — | **FLC 161WF** Gain 6.5 dB Output Power 30.5 dBm | — Output
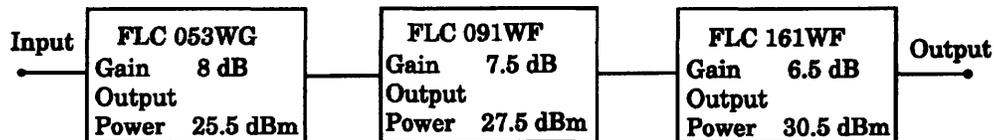
Fig.5.1 Main amplifier gain stages

The transistors employed in the design of the amplifier are stable within the operating band (eqs 1.17 - 1.18) and the matching networks were initially designed for a conjugate match employing the relevant equations in [1]. Single and double stub matching techniques, employing open circuited stubs, were used. The circuit was simulated with the CAD software Academy and was further optimized for flat gain across the band allowing for a gain ripple of +/-0.5 dB. Mismatches had to be introduced to improve gain flatness and, in order to ensure good return loss, isolators were placed at the input and output ports of the amplifier. The isolators employed were Mullard, type 272216901071 microstrip drop-in isolators. Since no S parameter data are provided for these elements it was not possible to account for their effect on the phase characteristics of the overall amplifier. Therefore, the phase response of the main amplifier was not simulated. It was directly determined from measurements of the practical circuit.

The schematic diagram of the optimized circuit is given in Fig.5.2. As with the design of the amplifiers of chapter 3 the stability was checked outside the band with the DC bias networks included and it was verified that the reflection coefficients at both ports remained less than one.

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The layout and assembly details of the main amplifier are shown in Fig.5.3. The amplifier was designed to be built on 0.02" Rogers RT/Duroid material, type 5880, with 0.125" aluminium backing. The grey shaded areas are the DC and RF ground. In these areas the dielectric material was removed and the aluminium was silver plated to allow soldering. These channels were machined to the dimensions of the transistors which were, then, soldered on the aluminium. This way a ground surface was, also, created and the appropriate pads for the DC bias were grounded by soldering copper shims between the end of the pad and the aluminium. The DC blocking capacitors used were 10 pF miniature single layer ceramic filled parallel plate capacitors manufactured by American Technical Ceramics, type 11XCC100C100πV. The bias inductors employed were three turn air core chokes, with a nominal inductance of 32 nH. The DC bias decoupling capacitors used were 1 nF, multi-layer ceramic chip capacitors, also manufactured by American Technical Ceramics, type ATC100A. The gate biasing resistors were commercial surface mount chip resistors of 400 Ω. The overall dimensions of the circuit were 20.3 x 132.1 mm^2.

5.2.2 Practical Evaluation of the Main Amplifier

The measured gain of the main amplifier is shown in Fig.5.4 together with the predicted gain from the simulation of the design shown in Fig.5.2. The practical amplifier exhibits 4 dB higher gain than the simulated amplifier. This was probably due to the devices providing higher gain than that specified with the provided S parameters. One possible explanation for this is that the grounding of the transistors was different from the one used for the measurement of the S parameters resulting in different gain response. Another possibility is high device manufacturing tolerances. This higher gain result was also observed in the testing of the auxiliary amplifier which employed the same devices. To obtain the flat response of Fig.5.4, the practical amplifier was tuned with small copper shims soldered on the appropriated places on the microstrip to provide adjustment of the stubs length. The practical amplifier exhibits a gain of 25.8 dB with a ripple of +/-0.5 dB across the 5.9 - 6.4 GHz band.

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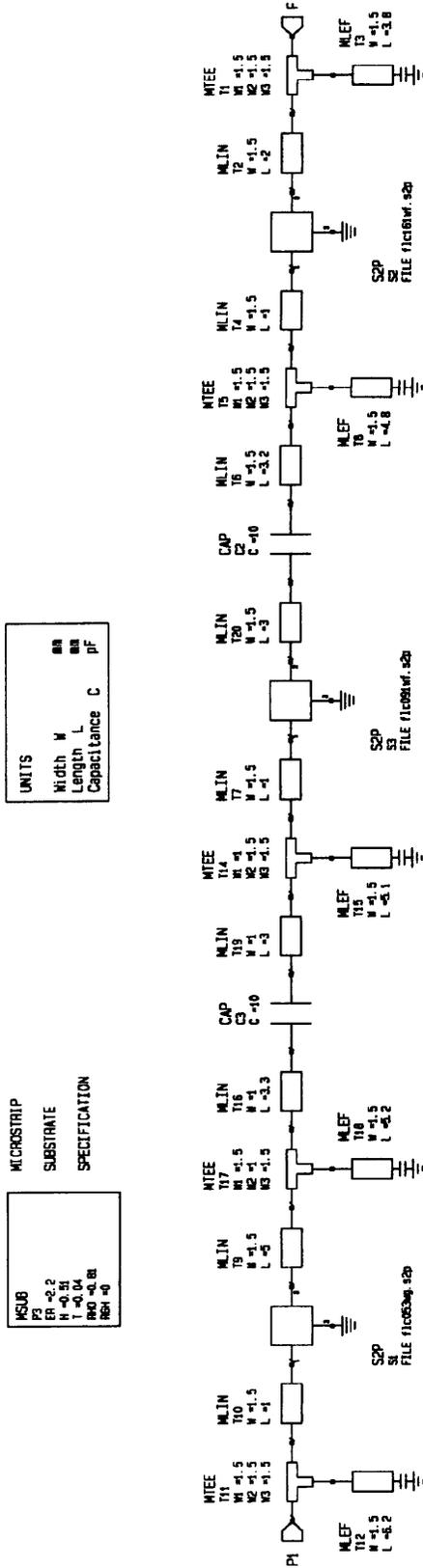
Fig.5.2 Academy schematic of the main amplifier
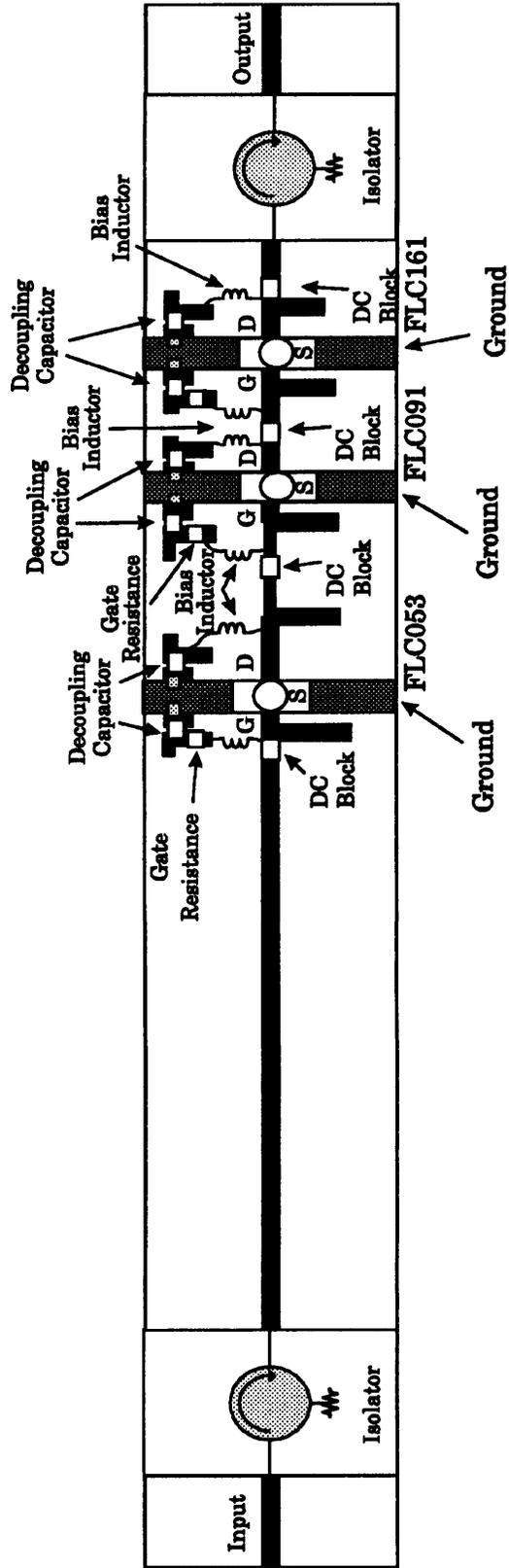
Fig.5.3 Layout of the main amplifier

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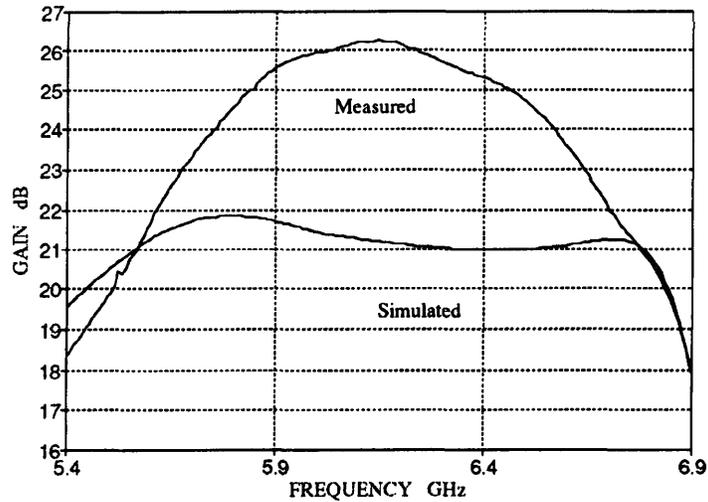
Fig.5.4 Measured and simulated gain of the main amplifier

For the phase characteristics measurements the "delay subtraction" facility of the HP 85107A network analyzer was employed to represent the amplifier as a delay element and a phase shift element. The same procedure had been followed in section 3.5 where the amplifiers were modelled as ideal delay and phase shift elements. One problem encountered in the phase measurements is that the amplifier was mounted in the measurement jig so that the measured phase included the effect of the input and output SMA connectors. To overcome this problem the phase response a 50 Ω line with a known length was measured first. The line was mounted in a measurement jig having SMA connectors of the same length as the ones employed in the amplifiers' measurement jig. This response was then subtracted from the amplifier's phase response and the 50 Ω line length was added to the overall delay. This way the effect of the SMA connectors was estimated and subtracted from the overall amplifier's phase response. The measured phase response is shown in Fig.5.5. The main amplifier introduces a delay of 1.636 ns and a phase shift of -7.5° with a phase ripple of +/-1° across the band.

The power characteristics of the main amplifier were, also, measured and are shown in Fig.5. 6. The amplifier provides 30.5 dBm output power at 1dB compression point.

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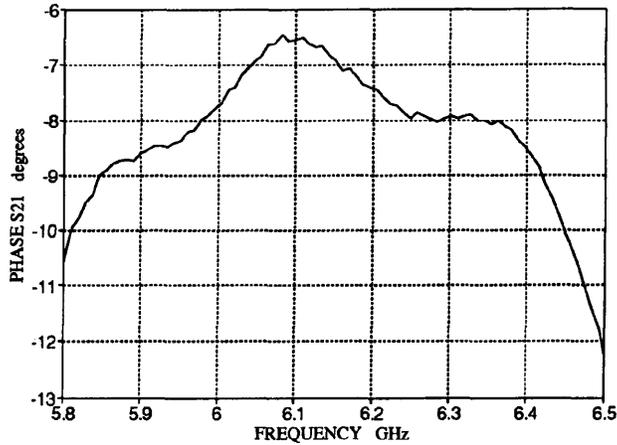
Fig.5.5 Phase response of the main amplifier

The phase characteristics of the amplifier as a function of output power were not measured because the HP 8510 network analyzer sources do not provide enough power to drive the amplifier into saturation. The input return loss was measured to be better than 20 dB across the band indicating that the isolators perform satisfactorily The output return loss was, therefore, expected to be at a similar level although it was not measured because the output of the amplifier was always followed by an attenuator to protect the measurement equipment. The output of the amplifier followed by the delay line and the coupler of the second loop (Fig.3.1) was measured during the assembly of the linearizer. No gain ripple was observed, indicating that the amplifier is well matched to 50 Ω.
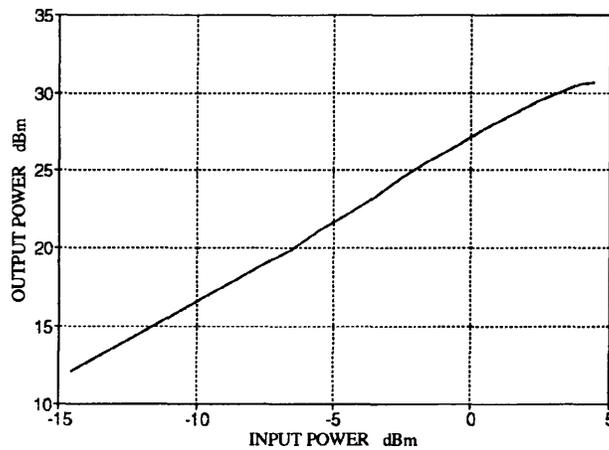
Fig.5.6 Output power of the main amplifier as a function of input power

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5.3 Auxiliary Amplifier

5.3.1 Design of the Auxiliary Amplifier

The gain of the auxiliary amplifier, derived from eq.3.6, should be approximately equal to the gain of the main amplifier plus the coupling ratio of the output coupler. Accounting for a coupling ratio of 10-15 dB, four gain stages were required. Again, the Fujitsu family FLC GaAs FETs were used. The transistors employed in the amplifying chain with their output power capabilities and the associated gain are shown in Fig.5.7.

| Input | FLC 053WG
Gain 8 dB
Output
Power 25.5 dBm | FLC 053WG
Gain 8 dB
Output
Power 25.5 dBm | FLC 053WG
Gain 8 dB
Output
Power 25.5 dBm | FLC 091WF
Gain 7.5 dB
Output
Power 27.5 dBm | Output |
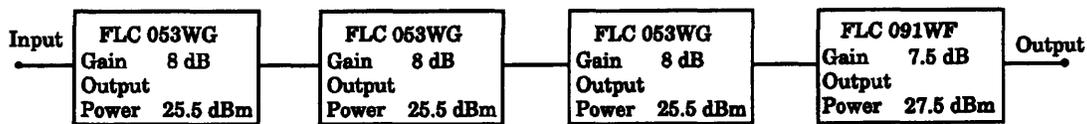
Fig.5.7 Auxiliary amplifier gain stages

Designing a multiple gain stage amplifier by directly matching the input of one transistor to the output of the preceding one results in a narrow band amplifier. It was advised by the technical personnel at Ferranti, not to cascade more than three gain stages employing interstage matching networks. The auxiliary amplifier was, therefore, designed as two 50 Ω amplifier modules, each having two gain stages. These two modules were then cascaded with a microstrip isolator in - between to ensure good matching to 50 Ω. All the matching networks were designed for a conjugate match employing single and double stub matching techniques with open circuited stubs. The initial values for the matching network parameters were calculated using the equations in [1] and the circuit was further optimized for flat gain across the 5.9 - 6.4 GHz band, allowing for a gain ripple of +/-0.8 dB. To ensure good input and output return loss microstrip drop-in isolators were placed at the input and output ports of the auxiliary amplifier. The isolators employed were of the same type as the ones used in main amplifier design. As with the main amplifier design, the phase response of the auxiliary amplifier could not be simulated and was determined later from measurements.
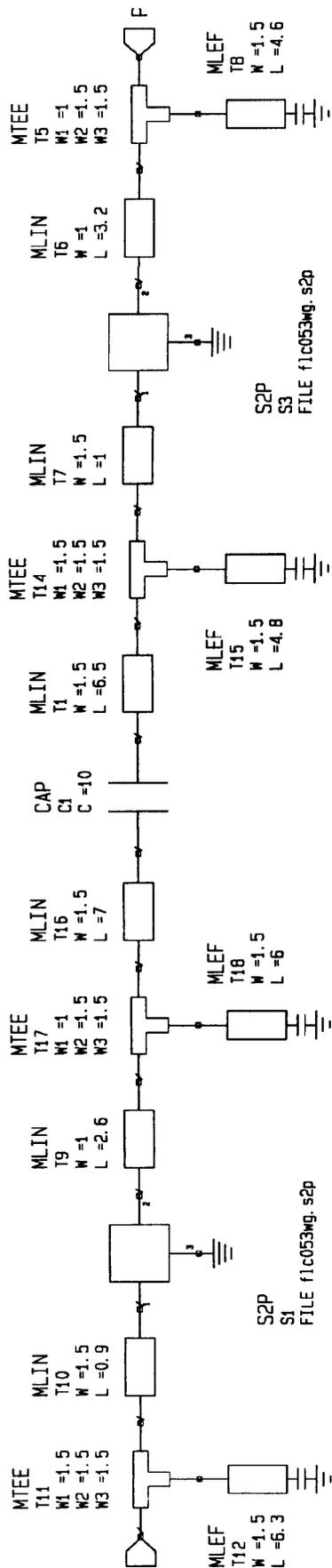
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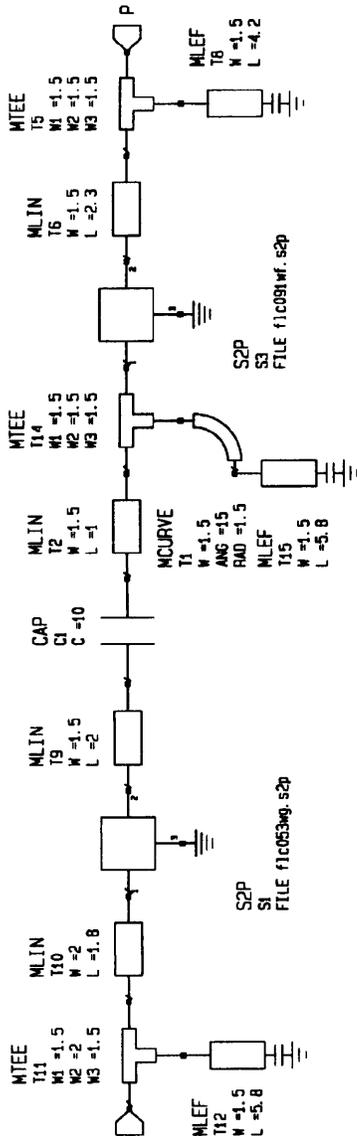
Fig.5.8 Academy schematic of the auxiliary amplifier

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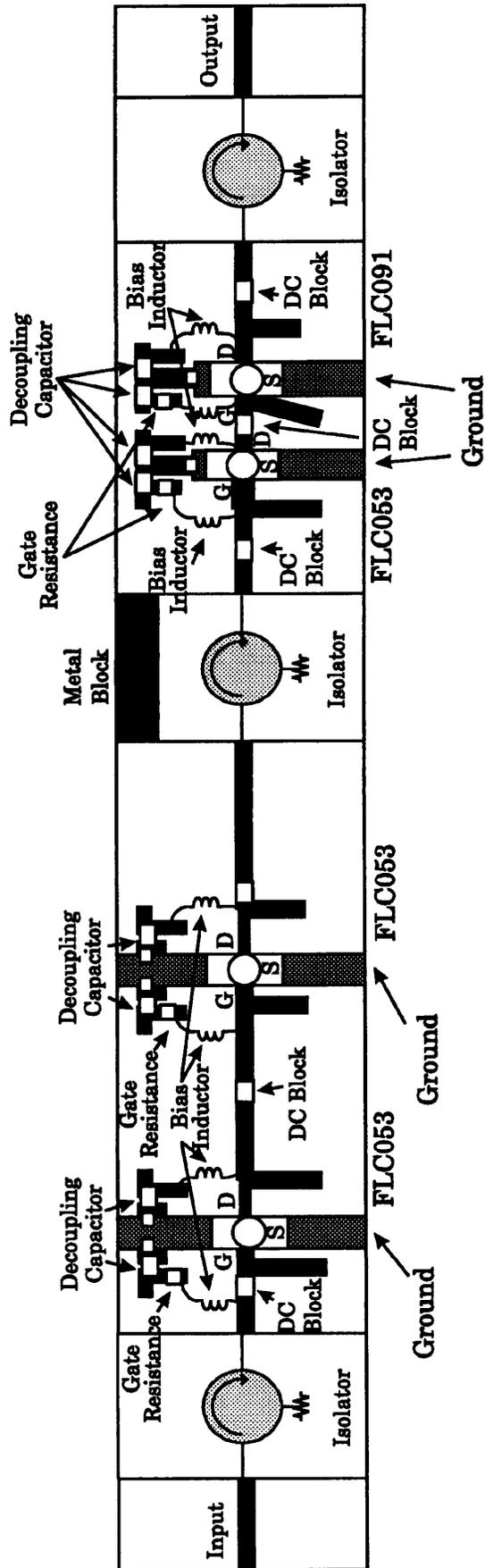
Fig.5.9 Layout of the auxiliary amplifier

The schematic diagram of the optimized amplifier's modules is shown in Fig.6.8. The layout and assembly details are shown in Fig.5.9. Details of the assembly procedure and the DC bias circuit elements are as described in section 5.2.1 for the main amplifier design. The overall board dimensions were again 20.3 x 132.1 mm^2.

5.3.2 Practical Evaluation of the Auxiliary Amplifier

The simulated and measured gain of the amplifier is shown in Fig.5.10. Again, the practical amplifier was tuned for flat gain. The final amplifier has a gain of 36.7 dB with a ripple of +/-0.25 dB across the 5.9 - 6.4 GHz band. As in the case of the main amplifier, the practical auxiliary amplifier, also, exhibits about 4 dB higher gain than the simulation predictions. The phase response of the amplifier is given in Fig.5.11. The circuit introduces a delay of 1.837 ns and a phase shift of -86.5° with a phase ripple of +/-2°. The method employed for the phase measurements of the main amplifier was again used to obtain the results shown in Fig.5.11. The input return loss of the amplifier was measured to be better than 20 dB and similar performance should be expected for the output port due to the isolators.
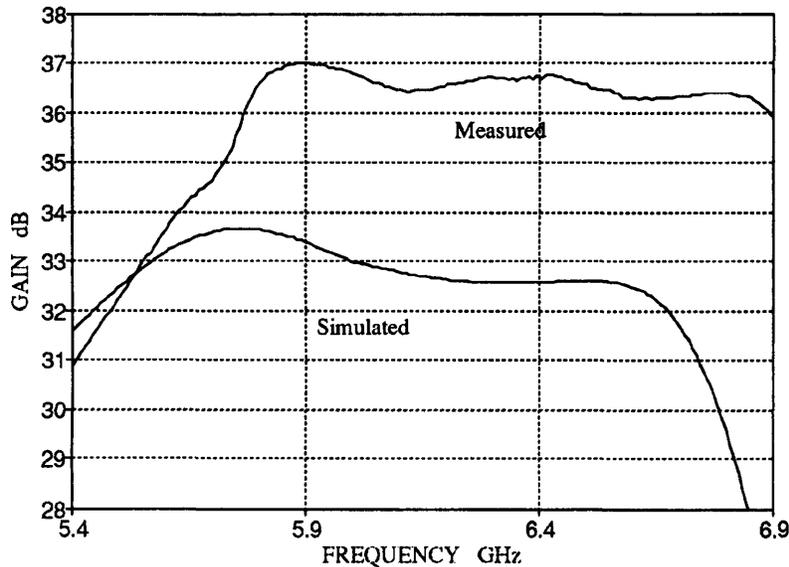
Fig.5.10 Measured and simulated gain of the auxiliary amplifier

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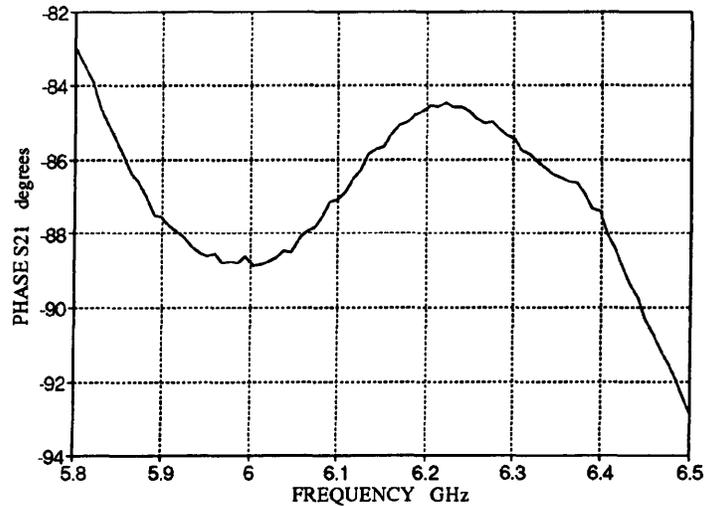
Fig.5.11 Phase response of the auxiliary amplifier

Although the phase ripple of the practical auxiliary amplifier is higher than the desired +/-1.4° the corresponding amplitude ripple is only +/-0.25 dB. For these levels of amplitude and phase imbalance the resulting second loop cancellation is 22 dB according to eq.4.18. Thus, the measured values for the phase and amplitude ripple of the practical auxiliary amplifier across the band are not a limiting factor for the desired 20 dB effective cancellation.

The amplifier exhibits high gain above 7 GHz and, when initially tested, it oscillated at frequency 7.2 GHz. This was due to the measurement jig dimensions permitting propagation above 7 GHz. To solve this problem a metal block was placed, as shown in Fig.5.9, on one of the aluminium channels to suppress the mode.

The power characteristics of the auxiliary amplifier were, also, measured and are presented in Fig.5.12. The amplifier provides 27 dBm output power at 1 dB compression point. Again, it was not possible to measure the phase characteristics as a function of input power because the measurement equipment did not provide enough power to saturate the amplifier.

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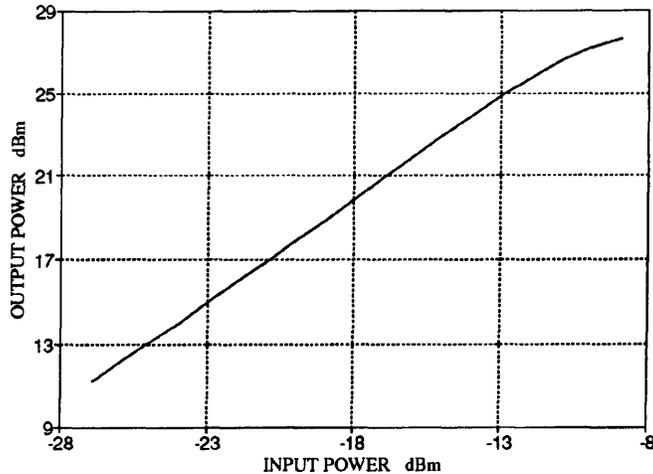
Fig.5.12 Output power of the auxiliary amplifier as a function of input power

5.4 Couplers

The input coupler was a 3 dB hybrid for the reasons explained in the design of the simulated linearizer in chapter 3, section 3.2. The configuration chosen was the Wilkinson divider[38] because it is a broad band element and it provides two identical outputs, as opposed to the branch line coupler configuration[35] which is not a symmetrical circuit and provides only 5% bandwidth. Both kinds of couplers were designed and fabricated on the 0.020" Rogers RT/Duroid material, type 5880 and were tested prior to their use in the linearizer circuit. The practical circuits exhibited return loss better than 18 dB, insertion loss of about 3.7 dB and isolation better than 18 dB.

The coupling ratio of the second coupler of the feedforward linearizer is determined by eq.3.4. The gain of the main amplifier is 26 dB and the loss L_1 through the linear arm A (Fig.3.1) is 6 dB due to the phase shifter which was employed in this path as will be discussed in chapter 6. The coupling ratio of the second coupler was, therefore, of the order of 32 dB. This can be easily realized in microstrip with the directional coupler configuration[107]. However, one problem encountered with the use of a directional

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coupler as the second coupler of the linearizer is the layout of the structure. In a microstrip directional coupler the coupled port is at the same side as the input port as seen in Fig.3.9. Therefore, in order to form the two feedforward loops, a crossover is necessary. To overcome this problem, a structure consisting of two cascaded directional couplers was employed. The schematic diagram and the layout of such a coupler are shown in Fig.5.13 and Fig.5.14 respectively. The input, output and coupled ports are at the appropriate place to allow the implementation of this coupler circuit in the practical linearizer.

```
NSUB                    MICROSTRIP
P5
ER =2.2                 SUBSTRATE
H =0.51
T =0.04                 SPECIFICATION
RHO =0.84
RGH =0

UNITS

Width    W      mm
Length   L      mm
```

MLIN
T24
W =1.5
L =21

MBEND3
T88
W =1.5

P2

MLIN
T93
W =1.5
L =2

MBEND3   MLIN
T89   T97
W =1.5   W =1.5
                L =11

P4

MTAPER
T186
W1 =1.22
W2 =1.5
L =4

MTAPER
T187
W1 =1.22
W2 =1.5
L =4

MBEND3
T195
W =1.22

MBEND3
T192
W =1.22

MRSTUB
T14
WI =1.25
L =6.1
ANG =60

RES
R5
R =50

MTAPER
T184
W1 =1.22
W2 =1.5
L =4

MBEND3
T194
W =1.22

MCLIN
S3
W =1.22
S =0.4
L =8.8
W1 =1.22
W2 =1.22
W3 =1.22
W4 =1.22

MLIN
T191
W =1.22
L =4

MLIN
T190
W =1.22
L =4

MBEND3
T193
W =1.22

MTAPER
T188
W1 =1.22
W2 =1.5
L =4

RES
R4
R =50

MBEND3
T199
W =1.22

MBEND3
T196
W =1.22

MRSTUB
T13
WI =1.25
L =6.1
ANG =60

MBEND3
T198
W =1.22

MTAPER
T189
W1 =1.22
W2 =1.5
L =2

MLIN
T26
W =1.5
L =2

MCLIN
S2
W =1.22
S =0.4
L =8.8
W1 =1.22
W2 =1.22
W3 =1.22
W4 =1.22

MBEND3
T197
W =1.22

MTAPER
T185
W1 =1.22
W2 =1.5
L =4

MLIN
T74
W =1.5
L =8

P3

MLIN
T36
W =1.5
L =6.6

MBEND3
T31
W =1.5

P1

Fig.5.13 Academy schematic of the second coupler configuration

147
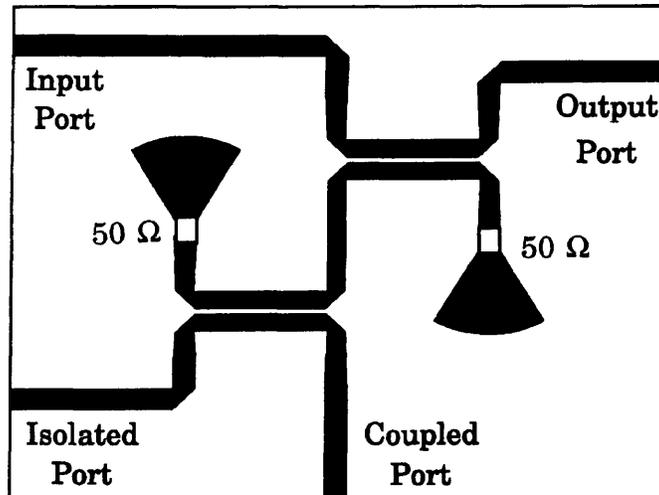
Fig.5.14 Layout of the second coupler

A further advantage of this coupler is the fact that its isolation is the sum of the isolation of the two directional couplers. As a result the coupler exhibits excellent isolation, of the order of 40 dB. This is an important property for the practical linearizer because high isolation of the second coupler ensures that no feedback paths are present in the feedforward circuit and, therefore, stability is secured.

The simulated and measured performance of a 30.3 dB coupler with the layout of Fig.5.14 is shown in Fig.5.15. The coupler has an isolation better than 45 dB and return loss better than 30 dB. The coupling ratio of the practical coupler, however, is 2 dB lower than the predicted 30.3 dB. This is probably due to the fabrication processes. The coupler was fabricated with a standard Printed Circuit Board etching procedure which often leads to the over-etching of the copper tracks. Since the microstrip coupled line width and spacing are critical parameters for the coupling ratio, the fabrication tolerances could have led to the discrepancy observed. The overcome the problem, a number of couplers with different coupling factors were fabricated and tested. The one exhibiting the desired value was employed in the final linearizer circuit.

The output coupler was a directional coupler with one port terminated with a 50 Ω resistor. Again, a number of couplers were fabricated and tested to ensure the correct coupling ratio was used.
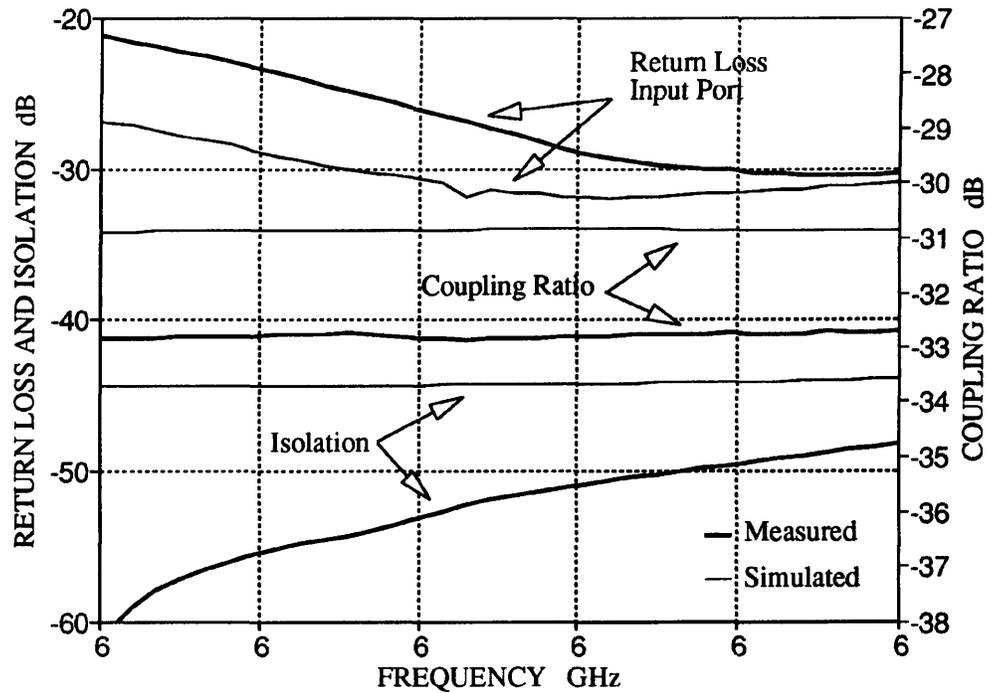
Fig.5.15 Measured and simulated performance of the second coupler

5.5 Microstrip Coupled Lines Filter

The overall performance of the feedforward linearizer is deteriorated if the auxiliary amplifier introduces significant intermodulation distortion. The power level of the intermodulation products introduced by the auxiliary amplifier depends on the linearity of this amplifier and the level of the residual carriers, as has been discussed in chapter 4. In addition, the out - of - band second order mixing products at frequencies $F_1 - F_2$ and $F_2 - F_1$ when combined with the residual carriers at frequencies F_1 and F_2

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could lead to further intermodulation distortion introduced by the auxiliary amplifier. This phenomenon has been discussed in detail in section 3.4.3. The solution proposed in this section was to employ a band pass filter at the input of the auxiliary amplifier in order to suppress the out - of - band second order products. The configuration used in the design of the simulated linearizer of chapter 3 was a microstrip coupled lines filter[107]. However, such a filter requires tight fabrication tolerances for the width and spacing of the coupled lines (Fig.3.12). The practical evaluation of such a filter showed that, given the limited PCB facilities at UMIST, the response of a simulated coupled lines filter cannot be reliably obtained with a practical circuit. The measured response of such a filter is shown in Fig.5.16. The practical circuit exhibits an insertion loss of 2 dB within the band and a return loss of only 7 dB at the lower end of the band.
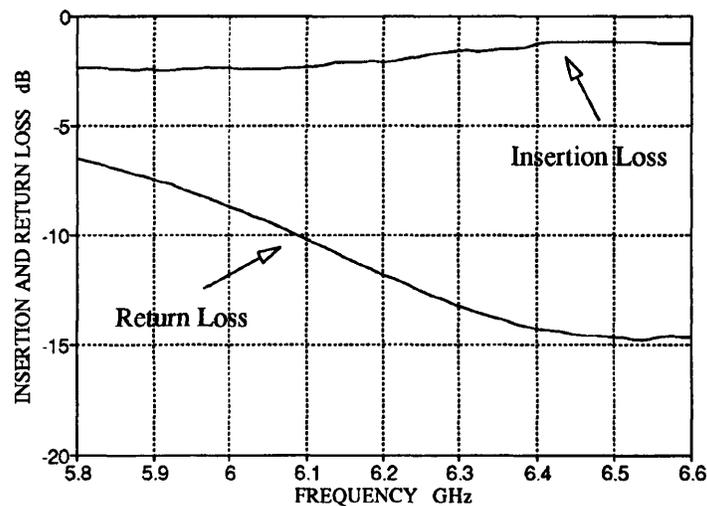
Fig.5.16 Insertion and return loss of the microstrip coupled lines filter

It was, therefore, decided not to use this element in the experimental feedforward linearizer. This decision is, also, justified from the use of a "double" directional coupler as the second linearizer coupler. The coupled port transmission loss of a directional coupler at low frequencies is of the order of 40 dB. Combining two such structures results in increased total transmission loss for the coupled port for frequencies below

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500 MHz. The simulated response of the directional coupler described in Fig.5.14 is shown in Fig.5.17 which indicates that the insertion loss of the double directional coupler would be adequate to effectively suppress the lower frequency second order intermodulation products.
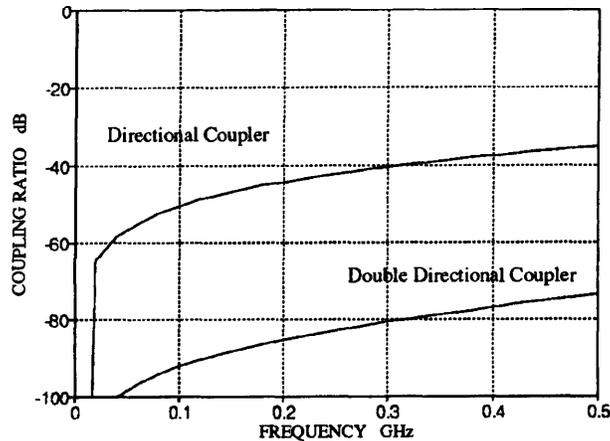
Fig.5.17 Coupling ratio of the second coupler at low frequencies

5.6 Conclusions

The design and performance evaluation of the feedforward linearizer components have been presented in this chapter. The main and auxiliary amplifiers have been tested and their response measured for use in the experimental linearizer design. The configuration of the couplers employed in the feedforward system has, also, been presented and the choice of specific circuits has been discussed based on practical implementation issues and measured results. The implementation difficulties encountered in the use of a microstrip coupled lines filter have, also, been discussed. The measured response of the various components were further used in the computer aided design of the experimental linearizer, as will be described in chapter 7.

CHAPTER 6

Design and Practical Evaluation of Phase and Amplitude Control Circuits

6.1 Introduction

The design and fabrication of phase and/or amplitude control circuits is presented in this chapter. Their performance is, also, practically evaluated considering the use of these circuits in the experimental feedforward linearizer circuit.

The Schiffman phase shifter employed in the design of the simulated linearizer of chapter 3 is practically evaluated here. The experimental results show very good agreement with the CAD predictions, indicating that this circuit can be reliably employed in the practical linearizer design.

Vector modulators were, also, designed and experimentally evaluated for use in the linearizer. The configuration investigated was quadrature phase shifters employing PIN diodes and single gate GaAs FET devices. The design considerations for each type of quadrature phase shifter are discussed in detail. The PIN diodes were characterized at the operating frequency band using the Through-Reflect-Line (TRL) calibration technique for the required measurements. They were, then, modelled by an equivalent circuit optimized to fit the measured S parameters. This way the performance of the simulated PIN diode phase shifter was obtained employing the CAD software Academy and was further evaluated by measurements. The phase and gain response of the practical PIN diode phase shifter was in good agreement with the results for the simulated circuit, but the practical circuit exhibited high nonlinearity, as will be further discussed in detail in section 6.4.4.

The design and practical evaluation of a GaAs FET phase shifter is presented in section 6.5. The design and modelling of the amplifiers employed in the phase shifter were based on the optimum load method developed in [32]. The practical evaluation of this phase shifter showed that single gate FETs can be an attractive solution for quadrature phase shifters. The advantages they offer over the commonly used dual gate FETs are availability, variety of characteristics and low cost. The measured performance of the practical phase shifter clearly indicate that it adequently meets the required specifications for implementation in the linearizer circuit.

Finally, considerations on the use of these quadrature phase shifters in the experimental linearizer are discussed in detail leading to the selection of the specific configuration.

6.2 Practical Evaluation of the Schiffman Phase Shifter

In Schiffman phase shifters[109] a differential phase shift is obtained by subtracting the phase response of a coupled lines C-section from the phase response of a suitably long transmission line. The related theory has been discussed in section 3.4.2, along with the associated CAD model of Fig.6.1. As explained in section 3.4.2 limitations of the software package lead to the use of a microstrip gap element MGAP[111]. The validity of this model is evaluated here for a 90° Schiffman phase shifter built on the 0.03" Rogers RT/Duroid material, type 5880.

The optimized Academy schematic of the C-section of a 6 GHz 90° Schiffman phase shifter is shown in Fig.6.1. The layout of the practical circuit is shown in Fig.6.2. The phase difference between the coupled lines C-section and the 21 mm microstrip delay line should be 90°. The initial values of the elements were calculated using the design equations in [110] and then optimized for phase flatness and return loss better than 20 dB across the 5.9 - 6.4 GHz band.

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MLIN
T3
W =2.1
L =6

MTEE
T13
W1 =2.1
W2 =2.1
W3 =1.04

MGAP
T7
W =2.1
S =0.25

MTEE
T14
W1 =2.1
W2 =2.1
W3 =1.04

MLIN
T4
W =2.1
L =6

P2

UNITS		
Width	W	mm
Space	S	mm
Length	L	mm
Angle	ANG	degrees

MCLIN
T2
W =1.04
S =0.25
L =6.5
W1 =1.04
W2 =1.04
W3 =1.04
W4 =1.04

MICROSTRIP

SUBSTRATE

SPECIFICATION

MSUB	
P4	
ER =2.5	
H =0.762	
T =0.04	
RHO =0.84	
RGH =0	

MBEND
T9
W =1.04
ANG =90
M =0

MLIN
T10
W =1.04
L =0.25

MBEND
T8
W =1.04
ANG =90
M =0
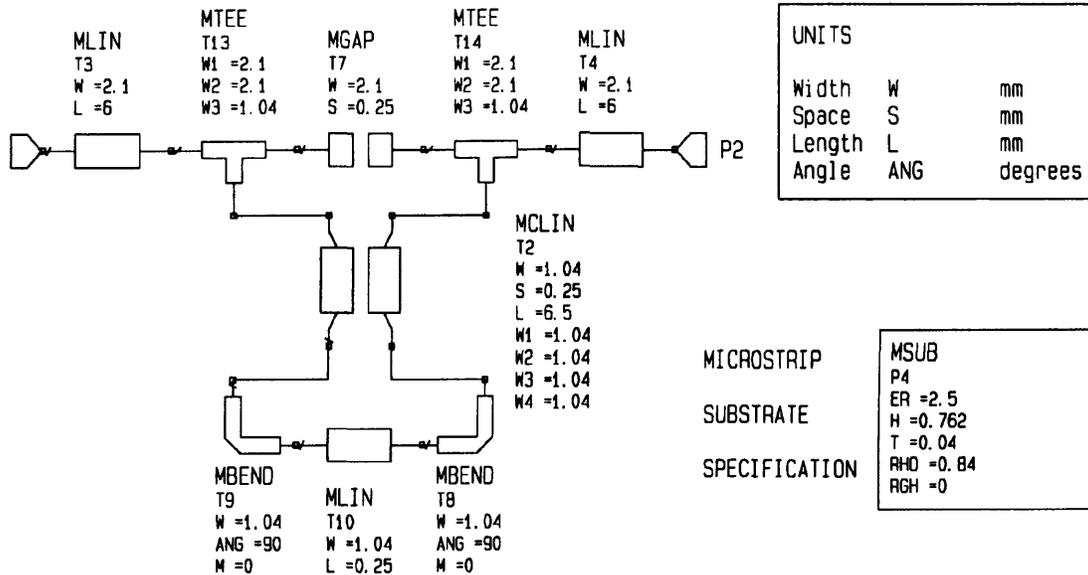
Fig.6.1 Academy schematic of the C-section of a 90° Schiffman phase shifter

The simulated and measured phase response of the circuit are presented in Fig.6.3. The phase response of the practical phase shifter closely agrees with the simulated results. The shape of the response graph is similar to the predicted response and the phase difference of 2° is well within the experimental errors. The measured results for the practical circuit, shown in Fig.6.4, indicate a phase variation of +/-1.5°, an insertion loss of 0.7 dB and a return loss better than 20 dB.

Schiffman phase shifters when built in microstrip exhibit poor matching to 50 Ω, because of the difference in the phase velocities of the odd and even

Delay Line

Coupled Line C-section

90

Fig.6.2 Layout of Schiffman Phase Shifter

modes of the structure[107]. For a 90° Schiffman phase shifter, the theoretical prediction for the return loss is worse than 11 dB[113]. This problem is often encountered in coupled microstrip lines. A method suggested to solve the problem in directional

couplers is to use capacitors at the edge of the coupled lines[114]. However, the Schiffman phase shifter of Fig.6.2 includes an extra coupling at the edge of the coupled lines due the specific layout forced by limitations on the software. An MGAP element, which is effectively some extra capacitance, was employed to take into account the extra coupling in the structure used in Fig.6.2. This extra coupling probably acts as the capacitor proposed in [114] and improves the return loss of the structure.
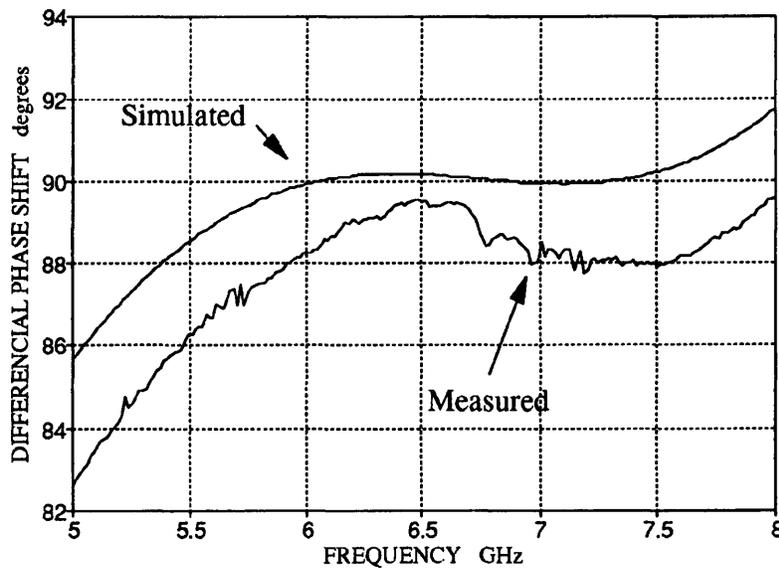
Fig.6.3 Phase response of the 90° Schiffman phase shifter

The performance of the practical Schiffman phase shifter verified the CAD predictions and showed that this circuit can be reliably used in the design of the experimental feedforward linearizer. However, the Schiffman phase shifter is not adjustable and can only be used to produce a fixed differential phase shift between two paths in the feedforward loops. Furthermore, fabrication errors that may affect the predicted phase shift cannot be tuned without degrading the return loss of the structure. Since phase balance is very critical for the linearizer performance alternative phase shifter configurations are, also, considered.
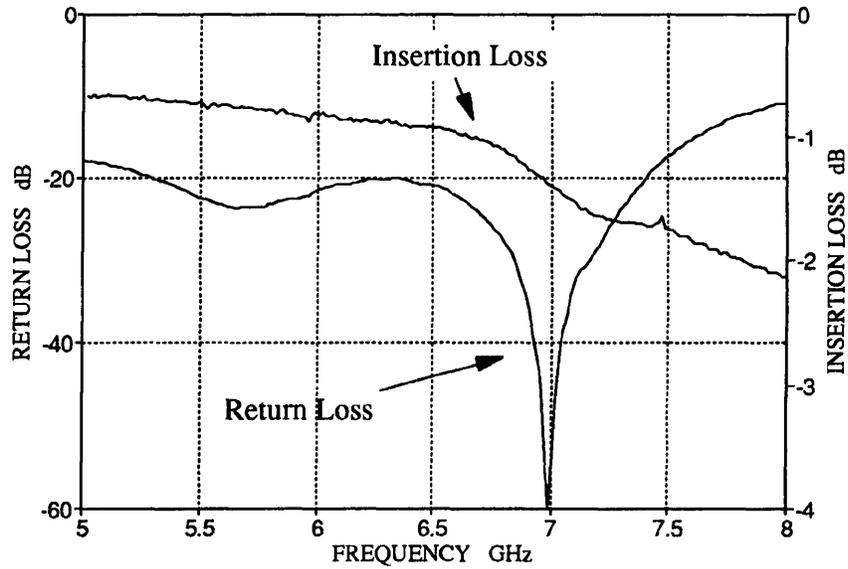
Fig.6.4 Insertion and return loss of the 90° Schiffman phase shifter

6.3 Quadrature Phase Shifters - Vector Modulators

The block diagram of a quadrature phase shifter is shown in Fig.6.5. Its principle of operation is based on the complex addition of two orthogonal variable vectors, to achieve a continuous 0-90° phase change.
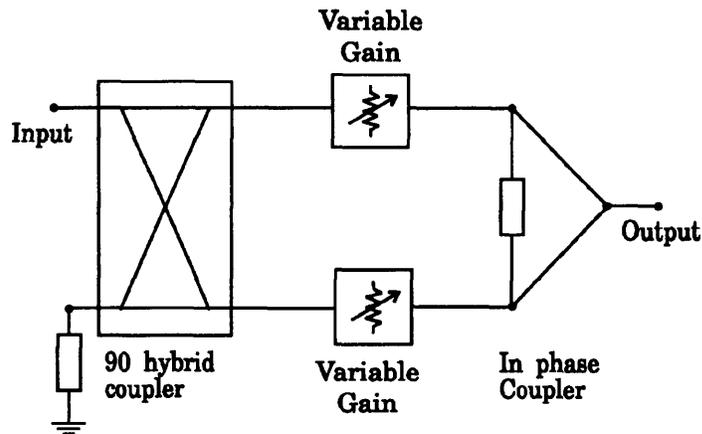
Fig.6.5 Quadrature phase shifter

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The input signal is split into two paths $90°$ out of phase, represented in Fig.6.6 by vectors A and B. The amplitude of each vector is controlled by a variable gain/loss circuit. These signals are then added by an in-phase combiner to produce the output resultant vector R. The magnitude and phase of the output voltage R are:

$$R = \sqrt{A^2 + B^2}$$ (5.1)

$$\theta = \tan^{-1}\left(\frac{A}{B}\right)$$ (5.2)

From the above equation it can be seen that the amplitude and phase of the vector R can be controlled by adjustment of the individual A and B components. Therefore, a continuous $90°$ phase shift can be achieved without varying the overall gain of the circuit by properly selecting the transmission coefficient of circuits A and B. Alternatively, the phase of the output voltage can be kept constant and its magnitude varied within the range R to zero. Furthermore, by properly varying the transmission coefficient of circuit A and B, both amplitude and phase can be varied simultaneously so that all the quadrant can be covered. Hence, the structure is also called vector modulator.
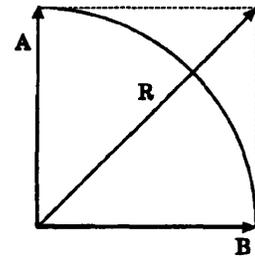
Fig.6.6 Vector addition

By combining two such structures the whole circle, $0\text{-}360°$, can be covered[115].

The vector modulator circuit allows both the amplitude and the phase of the output signal to be adjusted independently and is, therefore, ideal for use in the feedforward linearizer circuit. One disadvantage of this phase shifter circuit, however, is that it introduces a minimum 3 dB loss due to the $90°$ vector addition. Furthermore, in order to achieve the full $0\text{-}90°$ range, one of the vectors A or B should be completely suppressed for the extreme phase shifts, resulting in a total loss of 6 dB at the input and output couplers.

The most commonly used gain/loss varying elements for vector modulators are PIN diodes[116-117] and GaAs FETs[115][118]. The advantages and disadvantages of these

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configurations are further discussed in the following sections of this chapter. The design and practical evaluation of vector modulators employing PIN diodes and single gate GaAs FETs is, also, presented.

6.4 PIN Diode Phase Shifters

Quadrature phase shifters employing PIN diodes are a popular approach for analogue and multi-level digital phase shifters and are frequently used in phased array antennae applications[116-117]. The PIN diode element is used in these circuits as a variable attenuator to control the vectors A and B (Fig.6.6). This section presents the CAD modelling, design and practical evaluation of a quadrature phase shifter employing the beam lead HPND 4050 PIN diodes.

6.4.1 PIN Diode Characterization

Microwave PIN diodes are, usually, specified at frequencies up to a few hundred MHz. In the case of the HPND 4050 PIN diodes, the manufacturer data sheet (Appendix 1) provides data only at a single frequency of 100 MHz. It was, therefore, decided to further characterize and model the diode for use at 6 GHz. The calibration technique employed and the measurement results are presented next.

PIN diode modelling

The PIN diode is used at microwave frequencies as a variable resistance. This arises from the structure of the device. The PIN diode consists of an intrinsic semiconductor layer I placed between heavily doped p and n type regions. This I region is the variable resistive element in the diode. When a forward DC bias is applied to the PIN diode, free charges from the p and n regions flood the I region, thus, converting it into a conducting medium. The resistivity of the I region is dependent on the forward current and the diode behaves as a current controlled variable resistance. On the other hand, when a reverse bias is applied, the I region gets completely depleted of charge carriers and the diode

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behaves virtually like an open circuit, having a large capacitive reactance. For a microwave signal superimposed on the DC voltage, the time period of the positive half voltage would be too short when compared with the life time of the charge carriers with the result that no conduction can take place through the I region. Thus, in theory, for microwave signals the PIN diode acts as a linear device whose impedance is governed by the slope of the DC characteristic at the operating point.

The operation of the PIN diode as a variable resistance is based on the assumption that the RF frequency is high enough compared to the carriers lifetime so that no rectification takes place. Therefore, the linearity of a PIN diode is usually associated with the frequency of operation and the carriers' lifetime. According to the relevant HP manual[119] the nonlinear distortion of the diodes is kept at a minimum if the carrier lifetime of the diode used is greater than the inverse of the signal frequency. A figure of merit proposed is given by[119]:

$$\tau > \frac{1.6}{F} \tag{6.3}$$

where τ is the carrier lifetime and F is the signal frequency. For the diode chosen, the HPND 4050, $\tau = 25$ ns $> (1.6 / 6\times10^9)$. Therefore, the diode was modelled by the linear circuit shown in Fig.6.7. Further considerations on the linearity of the diode will be discussed in section 6.4.4.

At reverse bias condition the diode was modelled as capacitance C_1 in series with a resistance R_1, as shown in Fig.6.7. The resistance R_1 is the sum of the resistances of the p and n layers and the contact resistance. At forward bias condition the diode was modelled as a variable resistance R_2 which should, ideally, be 0 Ω for the fully on condition. The value of R_1 is typically in the range 0.2 - 5 Ω[120].
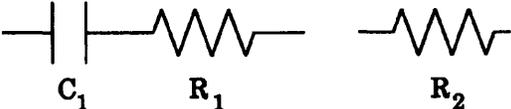
Fig.6.7 PIN diode model

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Typical values for the capacitance C_1 and the resistance R_2 for the fully on condition are in the range of 0.01 - 2 pF and 0.2 - 5 Ω respectively[120].

TRL Measurements

A major problem encountered when making network measurements in microstrip or other noncoaxial media is the need to separate the effect of the transmission medium, in which the device is embedded for testing, from the device characteristics. The accuracy of the measurement depends on the availability of quality calibration standards. Unlike the coaxial measurements, a set of distinct impedance standards are unavailable for microstrip. An alternative calibration approach has, therefore, been adopted for the PIN diode measurements.

The measurement jig constructed for these measurements is shown in Fig.6.8. The technique employed is called Through-Line-Reflect(TRL)[121] and allows the measurement system to be calibrated at the microstrip measurement plane of Fig.6.8. The TRL technique relies on the characteristic impedance of the short transmission line the length of which must be: $20^\circ < L < 160^\circ$ over the frequency range of interest. The calibration procedure requires two 2-port measurements and two 1-port measurements. The first standard, the Through, involves connecting the Port 1 microstrip line with the Port 2 microstrip line directly at the measurement plane and taking full 2-port S parameter measurements. The second standard, the Reflect, involves measuring the open (or short) circuit parameters at the measurement planes of Port 1 and Port 2. The third standard, the Line, requires the measurement of the 2-port S parameters with the line inserted in-between the measurement planes.

The measurements were performed on the vector network analyzer system HP 85107A which provides a TRL calibration facility. All calibration lines were designed to be 50 Ω and were fabricated on the 0.020" Rogers RT/Duroid material, type 5880. Connection to the calibration and test devices was provided by soldering thin copper shims on the microstrip lines to be connected. According to the HP TRL manual[121], connection

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repeatability is the largest single factor that limits the effectiveness of this calibration. To evaluate the performance of the calibration, the connection was broken and, then, the same device was reconnected and remeasured. Measurement repeatability of the reflection coefficient of a 50 Ω line was better than 40 dB the day the calibration was performed.
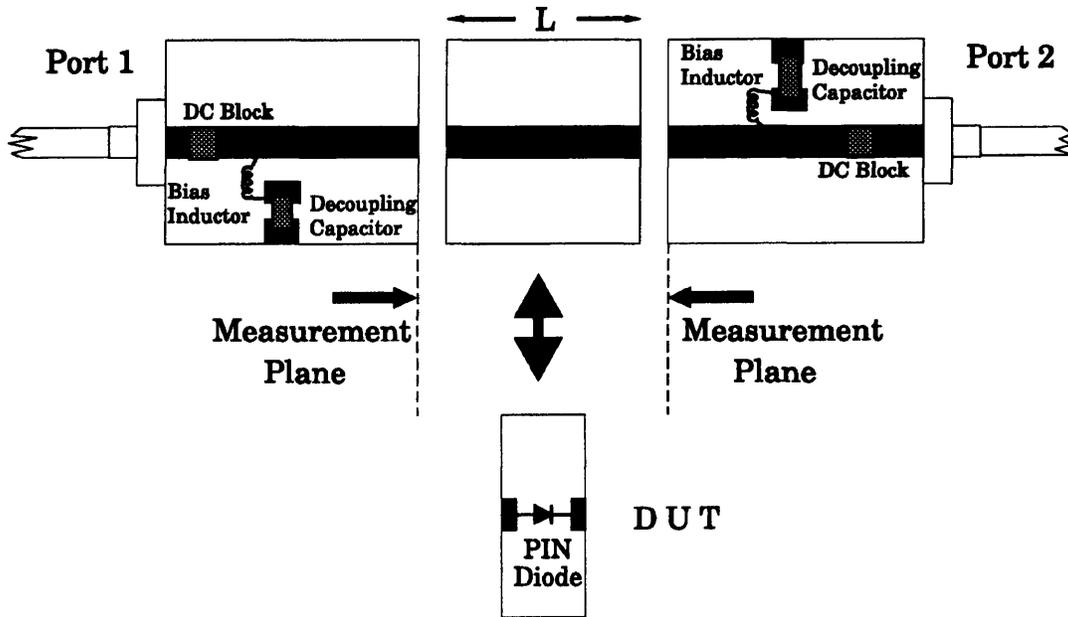
Fig.6.8 TRL measurement jig

Once the calibration to the measurement planes was completed, the central section of line was removed and replaced with the circuit that contained the PIN diode. That circuit consisted of two 50 Ω lines 4 mm long with a 0.2 mm gap, across which the diode was mounted. Conductive epoxy glue was used for the diode connection. The biasing networks and the DC blocking capacitors were included in the circuits beyond the measurement plane, Fig.6.8, so that their effect was taken into account in the calibration procedure. The DC blocking capacitors and the bias decoupling capacitors were 10 pF multi-layer ceramic chip capacitors manufactured by Tekelek, type CH-A. The bias inductors were precision three turn miniature air core chokes, manufactured by Piconics, type number M3T47SS, with a nominal inductance of 9.6 nH. The ground was provided with a metal pin connecting the case of the jig to the ground pad of Fig.6.8.

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Experimental Results

The TRL measurement jig allows the calibration of the network analyzer at the measurement planes of Fig.6.8. Therefore, the effect of the 50 Ω microstrip lines, where the diode was mounted on, is also included in the measured S parameters. These lines were modelled as well so that their characteristics were de-embedded and the correct values for the diode lumped element model parameters were obtained. The HPND 4050 PIN diodes are available in a beam lead package. Therefore, the diode chip was modelled as in Fig.6.7 and the leads were modelled as microstrip lines having the same dimensions. The Academy schematic of the equivalent circuit for the reversed bias condition is shown in Fig.6.9.

MSUB
P1
ER =2.2
H =0.51
T =0.04
RHO =0.84
RGH =0

MICROSTRIP

SUBSTRATE

SPECIFICATION

UNITS

Width	W		mm
Space	S		mm
Length	L		mm
Resistance	R		Ohms
Capacitance	C		pF

MLIN
T1
W =1.5
L =2

MGAP
T3
W ^wg
S ^lg

MLIN
T2
W =1.5
L =2

MLIN
T4
W ^w1
L ^l1

CAP
C1
C ^c1

RES
R1
R ^r1

MLIN
T5
W ^w1
L ^l1

Wg = 1.5

lg = 2l1 + 0.2
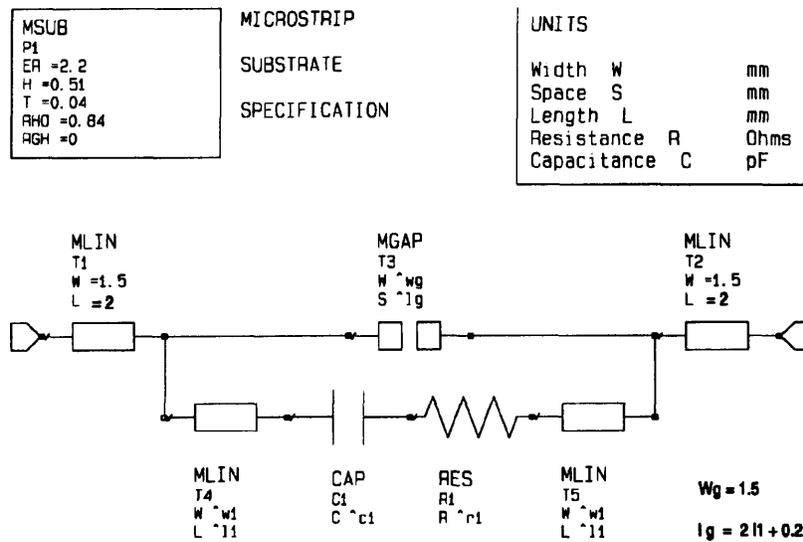
Fig.6.9 Academy schematic of PIN diode circuit model

The S parameters of the diode equivalent circuit (Fig.6.9) were curve fitted to the measured S parameters by varying C_1 and R_1 for the reverse bias condition. For the forward bias condition the capacitance C_1 and the resistance R_1 were replaced by the forward resistance R_2 of Fig.6.7 which was, then, optimized to produce the measured S parameters. The length L_1 and the width W_1 of the microstrip lines modelling the leads of the package were, also, allowed to vary 5%. The final values for the diode parameters were:

R_2 = 7 Ω   Forward bias fully on

C_1 = 0.154 pF   Reverse bias fully off

R_1 = 0.2 Ω

L_1 = 0.2 mm

W_1 = 0.1 mm

The equivalent circuit S parameters fitted to the measured S parameters are included in Appendix 3 for the various bias conditions. The modelled value for the reverse bias capacitor is in agreement with the manufacturers data which quote a value of 0.15 pF. The forward resistance corresponding to the fully on condition, however, is quite high, 7 Ω. In the relevant catalogue a forward resistance of 2 Ω is quoted for the HPND 4050 diode. This difference between the quoted and the on-circuit forward resistance of the diode is of particular significance for the performance of the phase shifter because it deteriorates the on / off ratio of the diode. As a result, the range of adjustment of the A and B components in Fig.6.6 is limited and, therefore, the available phase shift is less than 90°.

6.4.2 Computer Aided Design of the PIN Diode Phase Shifter

The configuration of the PIN diode phase shifter is shown in Fig.6.10. The diodes are connected in shunt and when switched off they appear to be open circuit so that the input signal propagates through the phase shifter paths. When one diode is forward biased its series resistance decreases and, as a result, the attenuation through this path of the phase shifter increases. When the diode is completely switched on it appears to be a short circuit and, ideally, no signal propagates through this path. One drawback of this circuit is that, in order to attenuate the signal in each path, mismatches are created resulting in poor input and output return loss. For a 0-90° phase change, a return loss of 6 dB has to be tolerated at the extreme phase shifts. This is fundamental limitation of the PIN diode vector modulators employing single diodes.

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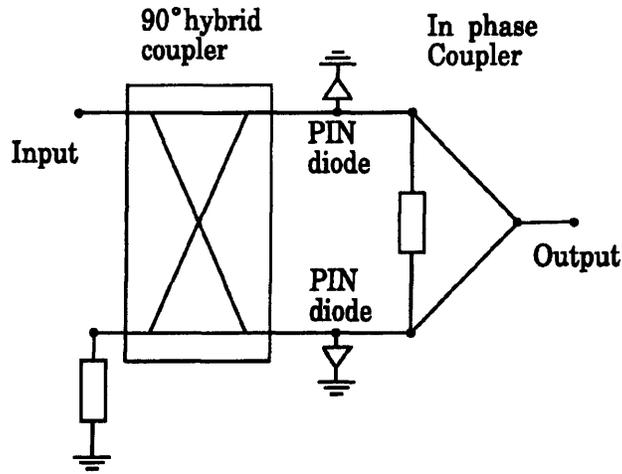
Fig.6.10 PIN diode quadrature phase shifter

The phase shifter structure was simulated employing the Eesof Academy software with the diode model as described in the section 6.3.1. For the forward biased condition the diode was modelled as a variable resistance and the phase shifts achieved for a 7-300 Ω range of the forward resistance R_2 values, are shown in Fig.6.11. The middle plot corresponds to both diodes reversed biased with $R_1 = 0.2$ Ω and $C_1 = 0.154$ pF. When the forward resistance R_2 changes the phase response of the circuit is shifted to higher or lower values. The range of phase variation that can be achieved is 82° due to the reduced on/off ratio of the PIN diode.
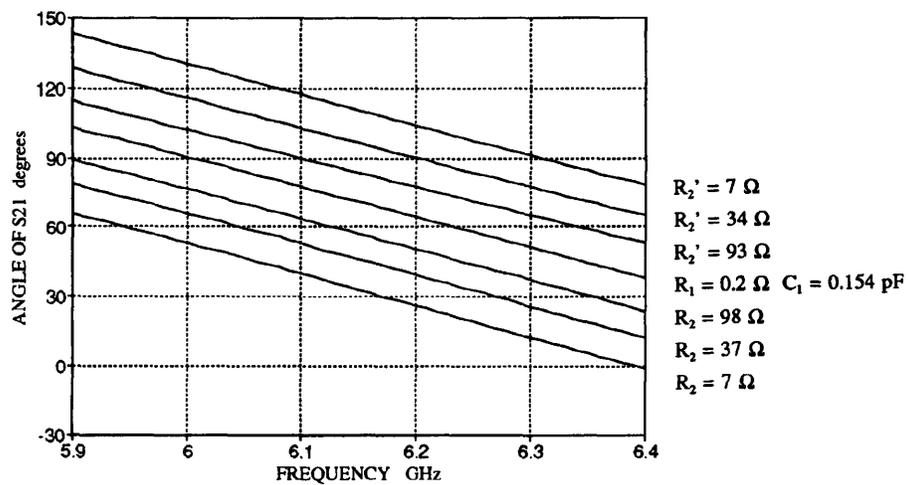
Fig.6.11 Simulated phase response of the PIN diode phase shifter

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The layout and assembly details of the phase shifter are shown in Fig.6.12. Radial quarter wavelength open circuit stubs were used to create an RF ground for the diodes. The length of the stubs was made shorter than $\lambda/4$ to account for the inductance introduced by the package leads. The microstrip lines at both sides of the diode were designed to be have an impedance higher than 50 Ω in order to introduce the extra inductance required to tune out the diode reverse bias capacitance and to provide broad band matching. The bias networks consisted of one $\lambda/4$ radial open circuit stub followed by a $\lambda/4$ high impedance line.
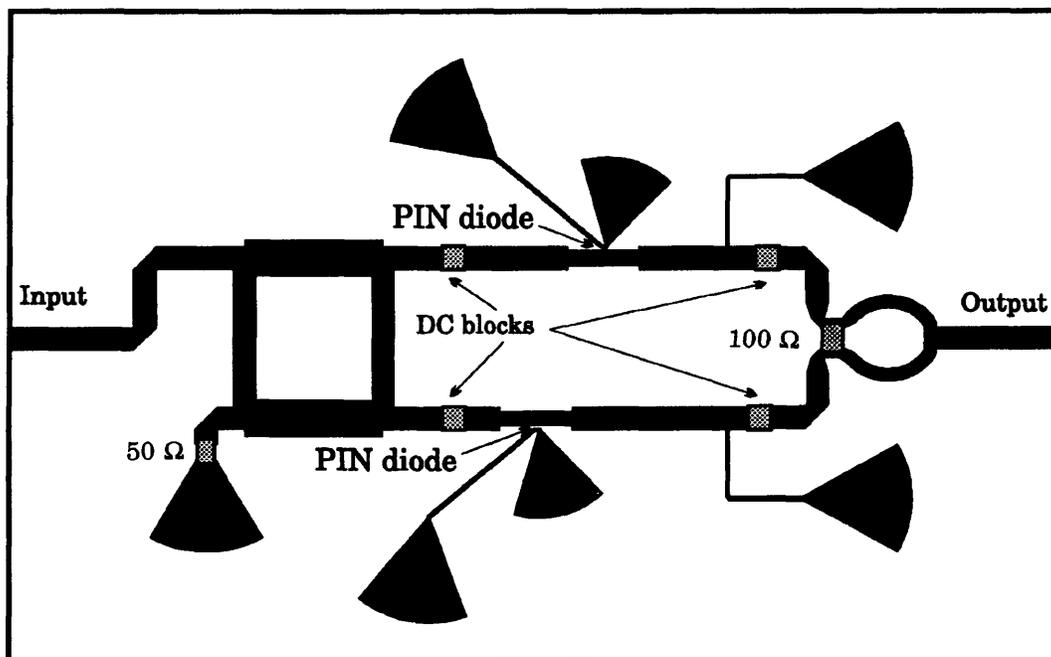
Fig.6.12 Layout of the PIN diode phase shifter

Since a branch line coupler is employed at the input, the circuit is not symmetrical and the reflected signals that occur at different bias conditions of the diode in one path can affect the performance of the other path. Although the isolation of the input coupler is 18 dB, the substraction or addition of an 18 dB lower voltage signal can cause a fluctuation of the order of 2 dB in the total output power. The simulation results indicated that the loss through the phase shifter was 5 dB or 7 dB depending on which path was attenuated. To overcome this problem, the distance of the two diodes from the

input coupler was adjusted so that the loss through the phase shifter circuit remained the same for both the extreme cases of 0° and 82°.

The PIN diode phase shifter was designed to be built on the 0.02" Rogers RT/Duroid material, type 5880. The DC blocking capacitors were 10 pF ceramic chip capacitors manufactured by Tekelek, type CH-A.

6.4.3 Practical Evaluation of the PIN Diode Phase Shifter

The relative phase shift of the practical phase shifter, taking the reverse bias condition as a reference, is shown in Fig.6.13 which indicates that the maximum phase range is 70°. To produce these results each diode was varied through the available resistance range by altering the applied DC voltage. When obtaining the results of Fig.6.13 the amplitude of the transmission coefficient of the phase shifter was allowed to vary. The variation of the insertion loss was in the range of 4-7 dB. It was, however, possible to maintain the same loss for the different phase conditions by properly adjusting the bias conditions.
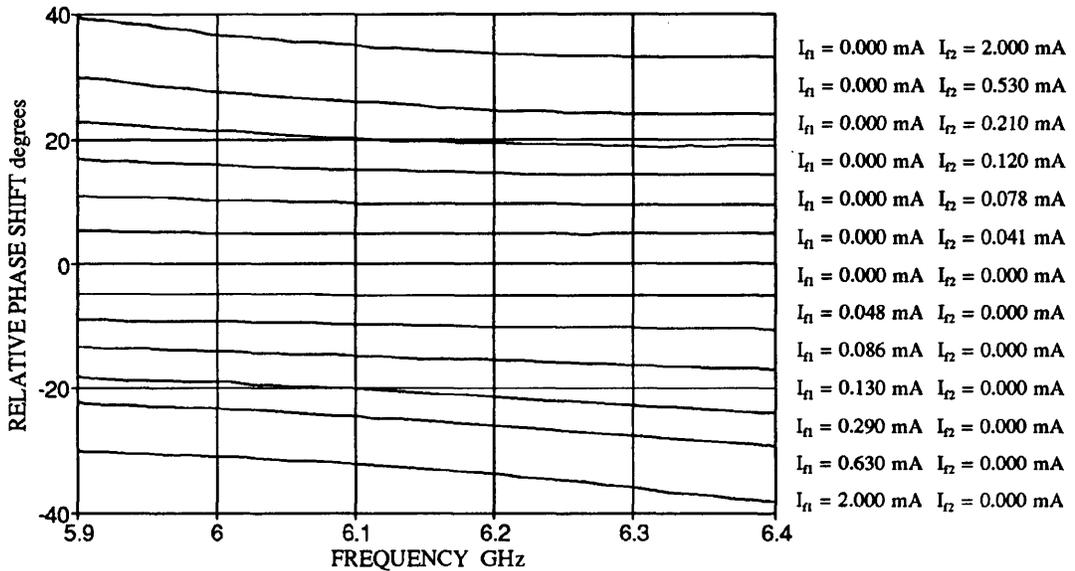
Fig.6.13 Phase response of the PIN diode phase shifter

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For the full 70° phase range a total loss of 6.5 dB has to be tolerated. Furthermore, as the relative phase shift increases the phase ripple across the band also increases. In order to keep the phase response of the phase sifter flat and reduce the insertion loss, it was decided to allow only for a +/-10° variation of the transmission coefficient phase. In this case the insertion loss of the circuit remained less than 5.5 dB and the return loss was better than 11 dB, as shown in Fig.6.14. The relevant phase shift, taking the state with both diodes reverse biased as a reference, is shown in Fig.6.15. The control currents for the phase states of Fig.6.15 are given in Fig.6.16.
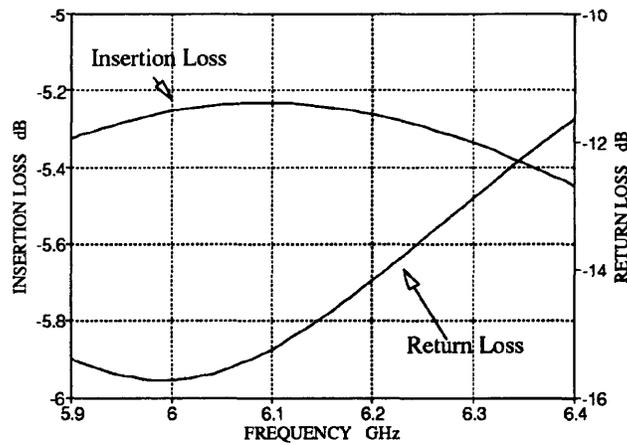
Fig.6.14 Insertion and return loss of the PIN diode phase shifter
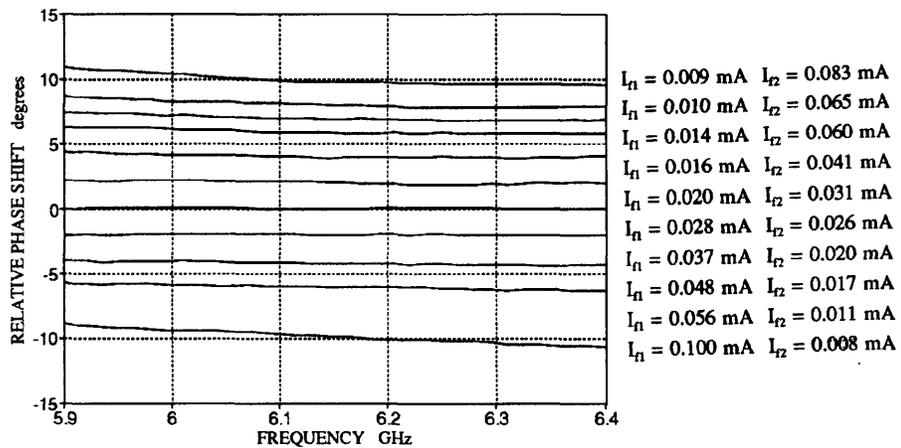
Fig.6.15 Phase response of the PIN diode phase shifter

167
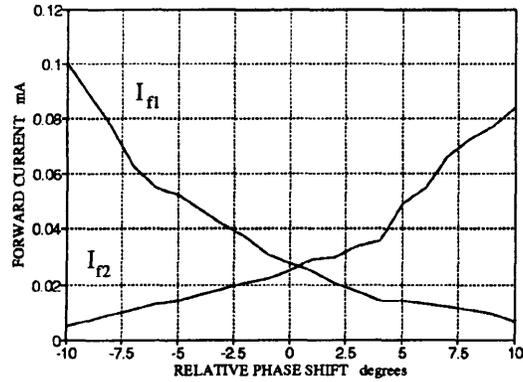
Fig.6.16 Control currents for the PIN diode phase shifter

6.4.4 Further Considerations on the Performance of the PIN Diode Phase Shifter

The PIN diode phase shifter linearity has been evaluated by two tone measurements. The spectrum at the output of the phase shifter is shown in Fig.6.17 for two carriers at frequencies F = 6.1 GHz and F = 6.2 GHz. The power level of the intermodulation distortion introduced by the PIN diode is only 35 dB lower than the fundamental signals. One possible explanation for this considerably nonlinear behaviour is given in [122].
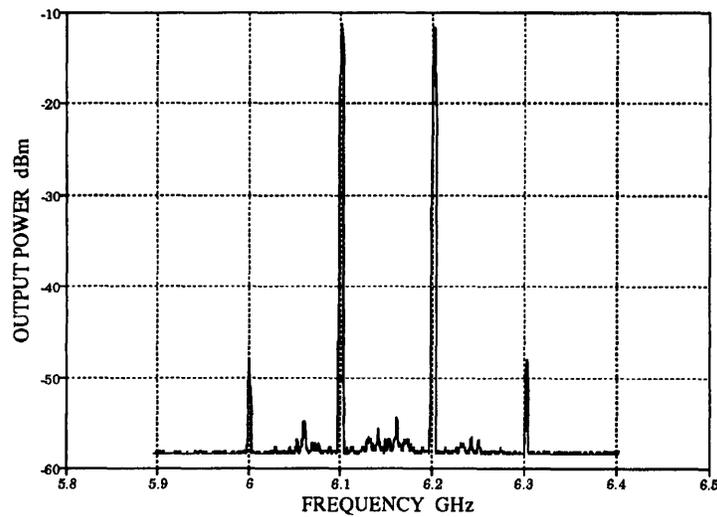
Fig.6.17 Spectrum of the PIN diode phase shifter

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Traditionally, distortion in PIN diodes has been thought to be only a function of the carrier lifetime and frequency of operation. However, more accurate analysis of the PIN diode behaviour showed that this is not entirely accurate and that the magnitude of the distortion signals generated in the diode is directly related to the frequency and the stored-charge to resistance ratio at the PIN diode operating point[122]. The distortion decreases with increasing the frequency. However, as the frequency is decreased or the power is raised or thinner I regions are used a self biasing mechanism becomes significant resulting in a behaviour resembling rectification. Single diode attenuator circuits like the ones employed in the phase shifter have been examined in this publication. It was shown that the carrier lifetime has no impact on distortion and that the significant factor controlling distortion at a given attenuation level is the I region width. Nevertheless, the manufacturer does not provide any relevant data for the HP PIN diodes and it was not possible to calculate the distortion that they introduce according to the relevant equations provided in [122]. The measured performance, however, indicates that the diodes used are significantly nonlinear devices and unsuitable for a phase shifter intended to be used in the linearizer circuit.

6.5 GaAs FET Phase Shifter

The use of amplifiers as variable gain elements in the paths of a vector modulator circuit leads to phase shifters with inherent gain. This is an important advantage over the PIN diode configuration because of the high 6 dB insertion loss inherent in quadrature phase shifters. The favourable devices for active analogue phase shifters are usually the dual gate FETs, mainly because of their high on/off ratio. Such phase shifters have been implemented in the past[115] and recently, simulation results for a MMIC vector modulator employing dual gate FETs have been reported[118]. Single gate FETs, however, could be an attractive alternative. Single gate FETs are the most commonly used devices for microwave applications and fully developed by all the manufacturers and are, therefore, the most practical solution when considering availability, cost and the

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range of power and gain characteristics offered. This section describes the design and practical evaluation of a single gate FET vector modulator for use in the linearizer circuit.

6.5.1 Design considerations

The block diagram of a FET phase shifter is shown in Fig.6.18.
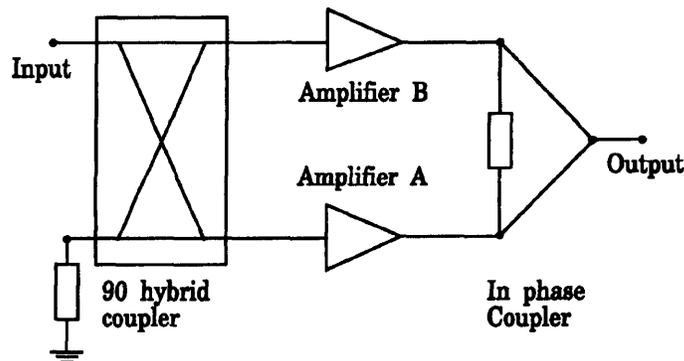
Fig.6.18 Block diagram of a FET quadrature phase shifter

In general, quadrature phase shifters employing FETs as variable elements are limited by changes in the transmission characteristics of the devices when the bias conditions change. In practical circuits the gain of the amplifiers is varied by adjusting the gate voltage. However, variation of the gain voltage also results in variation of the phase transmission characteristics of the transistor. This is a limiting factor inherent in such type of phase shifters, resulting in phase and amplitude ripple and reducing the range of phase shifts that can be achieved in practice. The performance of such phase shifters has been evaluated in [123] which showed that when considering magnitude errors single gate FETs are expected to show a better amplitude control, than dual gate FETs and, if biased at low gate voltage conditions, similar phase errors compared to dual gate FETs.

The performance of single and dual gate FET quadrature phase shifters has been simulated and the results for the single gate devices are shown in Fig.6.19. This simple

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graphical representation provides an insight into the problem although only a single frequency is considered. From this figure it can seen that the whole quadrant cannot be covered. Furthermore, in order to achieve a wide phase range the transistors have to be biased at low gate voltages.
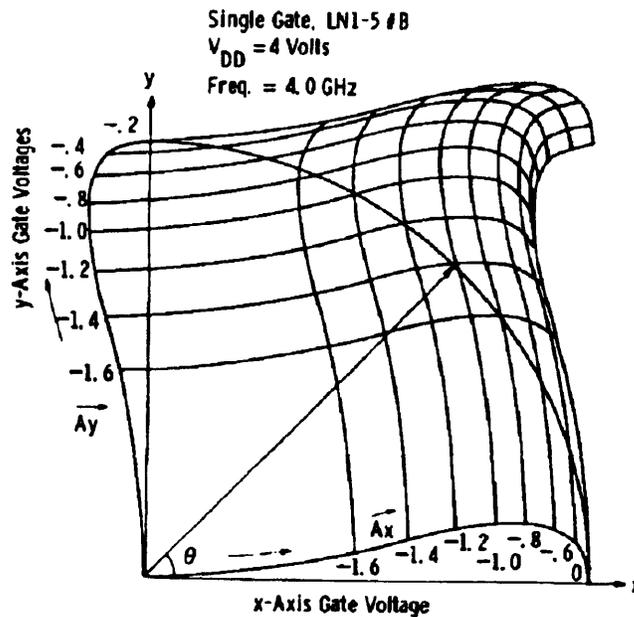
Fig.6.19 Predicted performance of a single gate GaAs FET phase shifter[123]

6.5.2 Prediction of the Optimum Load

The device used for the phase shifter was the Avantek ATF13136. The relevant data sheets are included in Appendix 1. It is medium power transistor providing an output power of 17.5 dBm at 12 GHz with a corresponding gain of 8 dB. However, this transistor is often used as a low noise device and the S parameter data provided by the manufacturer were measured at low current bias conditions. Since the phase shifter was intended to be used in a linearizer circuit, where maximum linear power is desirable, it was decided to bias the device for class A operation, at the middle of its I-V characteristics. In order to do that, DC measurements were performed and the measured I-V curves of the device are shown in Fig.6.20. The chosen bias conditions for the transistor are: $V_{ds} = 2.6$ V and $I_{ds} = 31$ mA.

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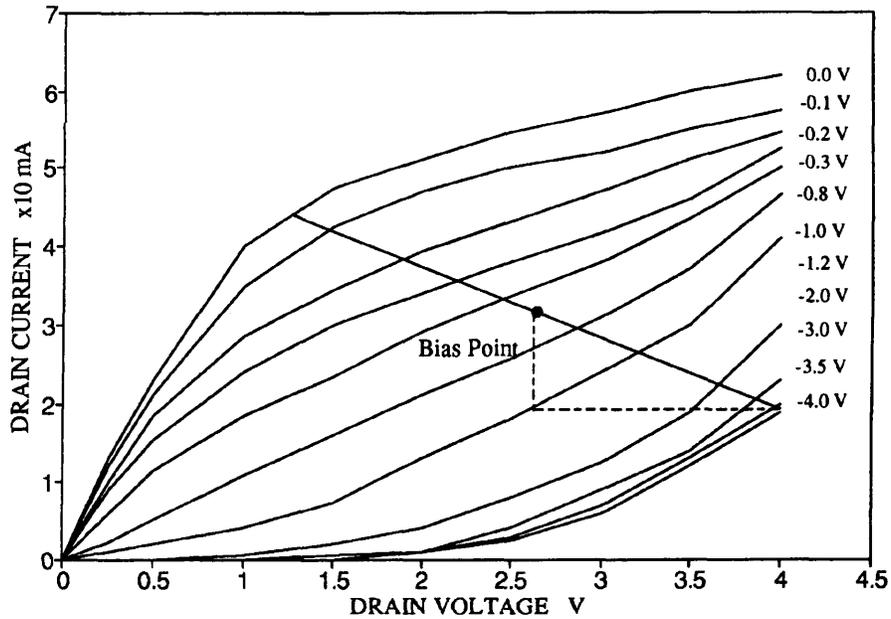
Fig.6.20 I-V characteristics of the GaAs FET ATF13136

The optimum load for the device was defined following Cripps' method [32] previously discussed in section 1.5.4. The resistive part of the optimum load is the slope of the load line which allows the maximum current and voltage swing. It was therefore, determined from the DC measurements shown in Fig.6.20 to be R_{opt} = 110 Ω. In order to take into account the high frequency parasitic elements of the device, the transistor was, then, modelled using the small signal measured S parameters. At large signal condition the S parameters of the FET change and, according to Cripps, the drain resistance becomes equal to the optimum resistance R_{opt}. Thus, to model the device for large signal operation the drain resistance of the small signal model was replaced by the optimum resistance R_{opt}.

6.5.3 CAD Analysis and Modelling of the Amplifier

The transistor ATF13136 was modelled using the lumped element equivalent circuit suggested by the manufacturer for the Avantek packaged GaAs FETs. The relevant data book includes parameter values for the elements of both the chip and the package

models. Nevertheless, the parameter values suggested correspond to different bias condition than the ones used for the measurement of the small signal S parameters. Thus, the chip parameter values had to be optimized for the bias conditions corresponding to the measured S parameters. The modelling procedure suggested in[124] was followed. The package element values, however, were only allowed to vary 10 % from the values suggested by the manufacturer. The equivalent circuit used to model the ATF13136 is shown in Fig.6.21 and the S parameters of the optimized equivalent circuit are included in Appendix 4. The optimized values for the various elements are, also, included in Appendix 4.
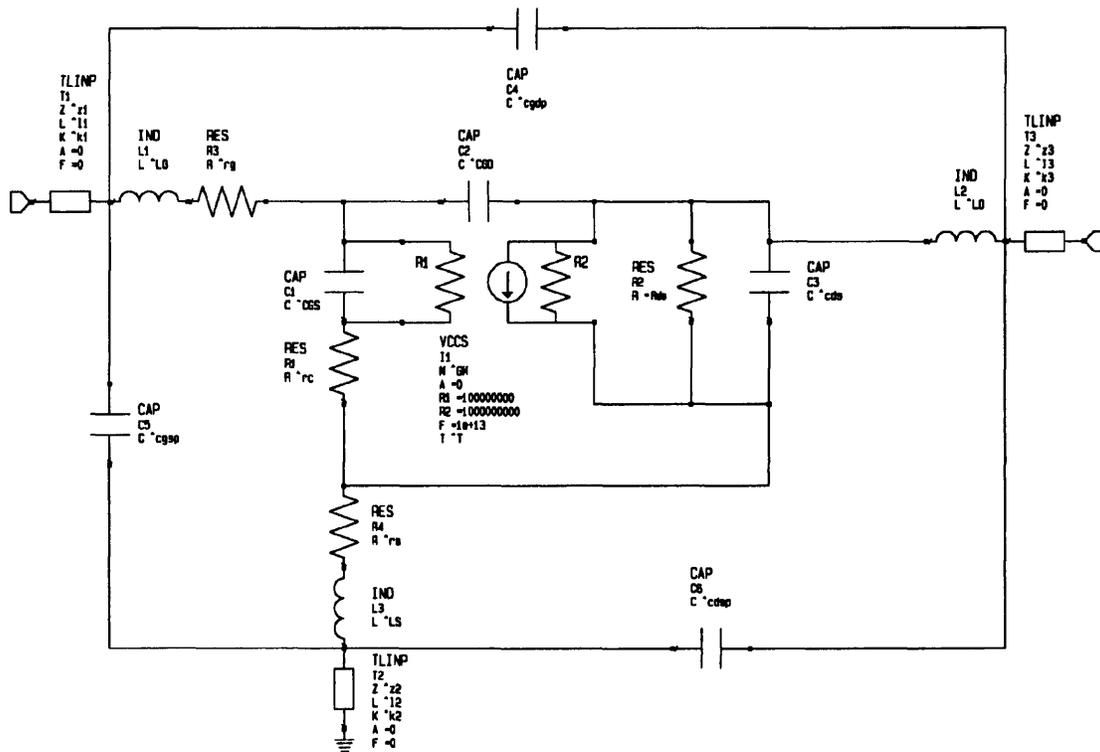
Fig.6.21 Lumped element equivalent circuit of the GaAs FET ATF13136

Once the linear equivalent circuit was obtained, the drain resistance R_{ds} was substituted by the optimum resistance R_{opt} determined from the DC measurements. This new circuit should correspond to the large signal model of the device.

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The amplifier was optimized for optimum output power. The output matching network consisted of one λ/4 transformer and a 50 Ω line. For the input matching network the single stub matching technique with open circuit stubs was employed. The power performance of a GaAs FET is determined by the load presented to the device, as discussed previously in section 1.5.3. Therefore, in order to design the amplifier for optimum output power the input port was matched to 50 Ω and the output matching network was optimized for output return loss better than 20 dB. The resulting output matching circuit corresponds to the optimum load for the large signal operation of this transistor over the frequency range 5.9-6.4 GHz. The input matching network was then optimized for high linear gain over the band, employing the small signal model. The performance of the final design was, also, verified with the measured S parameters and it was confirmed that the small signal equivalent circuit and the measured S parameters produce the same amplifier response. The Academy schematic of the optimized circuit is given in Fig.6.22. The simulated performance parameters of the designed amplifier are shown in Fig.6.23. The amplifier has a gain of 13 dB and an output return loss better than 16 dB. The input return loss, however, was allowed to be as low as 7 dB in order to maintain the gain flatness across the band.

MSUB
P3
ER =2. 2
H =20
T =0. 2
RHO =0. 84
RGH =0

MICROSTRIP

SUBSTRATE

SPECIFICATION

UNITS

Width   W   mil
Length   L   mil

MTEE
T7   MLIN
W1 =61. 46   T6
W2 =61. 46   W =61. 46
W3 =61. 46   L =170

MLIN   MLIN
T4   T5
W =61. 46   W =90
L =107. 5   L =357. 75

MLEF
T8
W =61. 46
L =160

S2P
S1
FILE 13135n. s2p
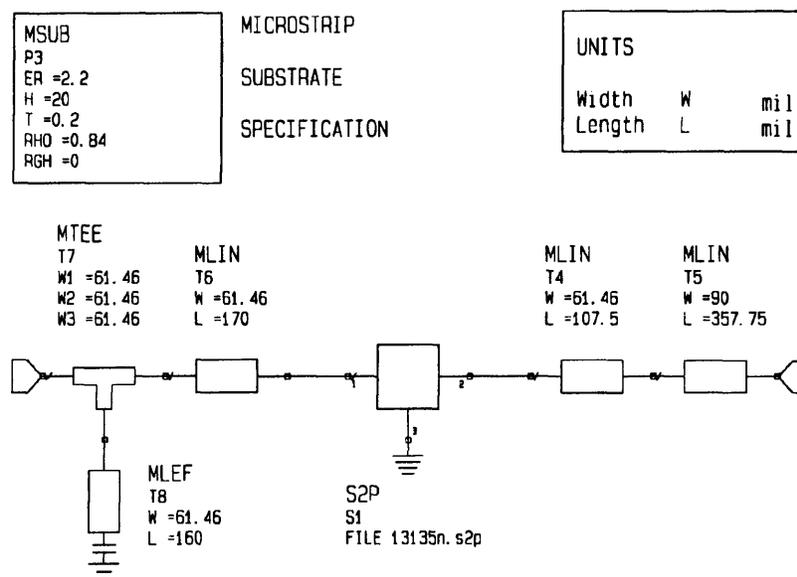
Fig.6.22 Academy schematic of the amplifier
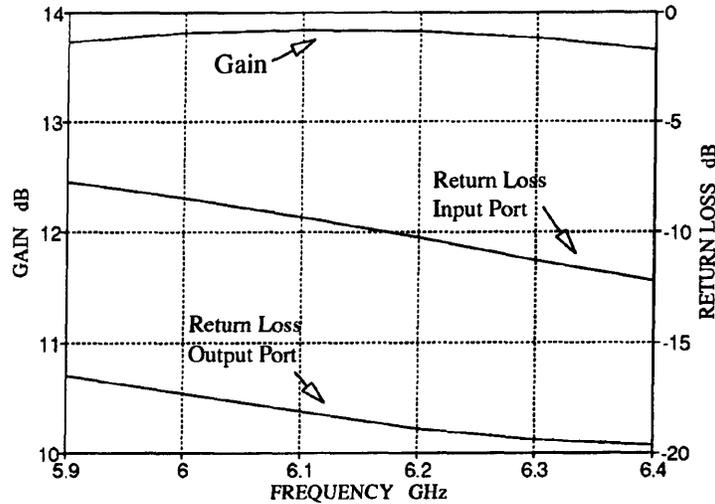
Fig.6.23 Simulated gain and return loss of the amplifier

6.5.4 Design of the Phase Shifter

It was not possible to simulate the performance of the FET phase shifter because no data were available for the behaviour of the transistors for different gate voltages. The amplifier was, therefore, placed in a quadrature phase shifter structure and its performance was evaluated with the practical circuit. The layout and assembly details of the FET phase shifter are shown in Fig.6.24.

The phase shifter was constructed on the 0.02" Rogers RT/Duroid material, type 5880 and it was mounted on a 0.125" brass block. The grey shaded areas are the DC and RF ground. In this area the circuit board was cut and the dielectric material removed. Two metal blocks having the same width as the transistors' diameter were placed in this area to provide a ground plane at the surface of the circuit. The source leads of the transistors were held down on the ground by metal clamps, as seen in the detail box of Fig.6.24. The DC blocking capacitors were the same type employed in the diode phase shifter circuit. The bias network consisted of two quarter wavelength lines terminated in an

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open circuit. The same bias point was used for the drain terminals of both devices while two different networks were designed for the gate bias in order to adjust the gain of each device independently.
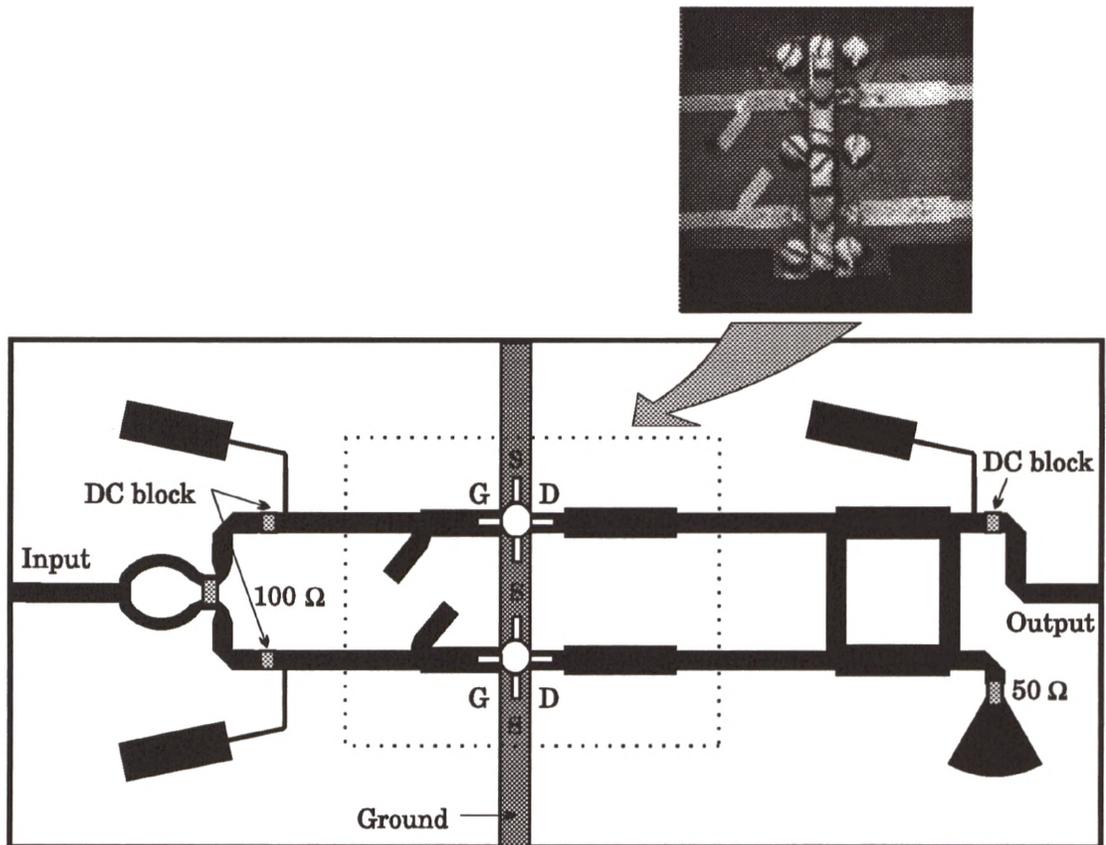
Fig.6.24 Layout of the GaAs FET phase shifter

6.5.5 Practical Evaluation of the FET Phase Shifter

The gain and return loss of the experimental single gate FET phase shifter are shown in Fig.6.25 for the bias conditions $V_{ds} = 2.6$ V and $I_{ds} = 31$ mA. The circuit exhibits a gain of 9.5 dB and return loss better than 11 dB across the band. In order to evaluate the success of the optimum load method the power characteristics of the transistor were measured. The output power as a function of the input power for the a single device is shown in Fig.6.26. The amplifier appears to be very linear with 1 dB compression point

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at the same power level as the saturation. Taking into account about 4 dB losses in the phase shifter circuit and the SMA connectors the saturation power is 19 dB which compares well to the typical output power 17.5 dB at 12 GHz quoted by Avantek for the ATF13136.
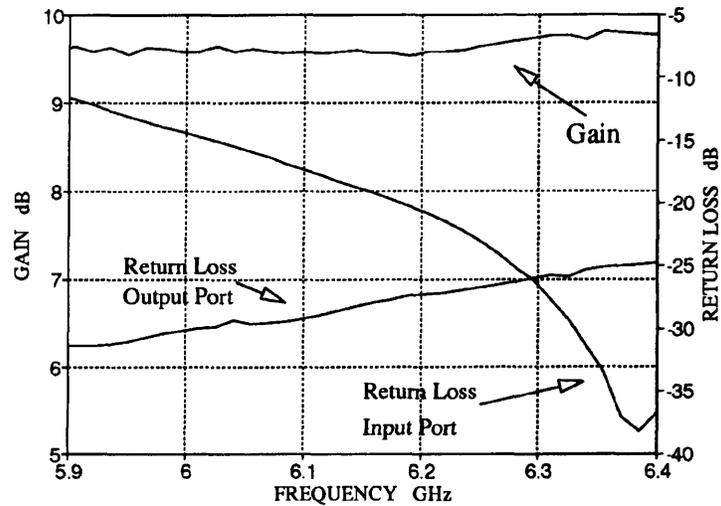
Fig.6.25 Gain and return loss of the experimental FET phase shifter
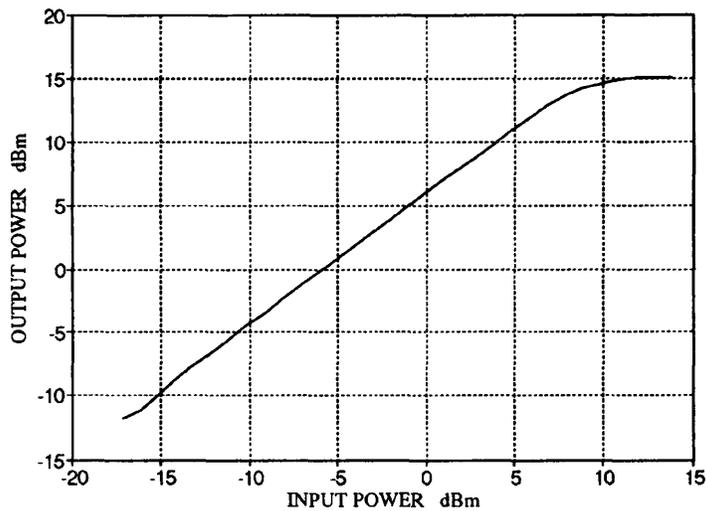
Fig.6.26 Output power characteristic of the ATF13136 GaAs FET phase shifter

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The phase range that was achievable with the practical FET phase shifter, for a gain variation of +/- 1.7 dB, is shown in Fig.6.27. Taking as the reference the phase of the output signal with both amplifiers exhibiting the same gain, the relative phase shift that can be achieved with the experimental phase shifter is $50°$.

$V_{gs1} = 1.19$ V	$V_{gs2} = 1.05$ V
$V_{gs1} = 1.14$ V	$V_{gs2} = 1.10$ V
$V_{gs1} = 1.04$ V	$V_{gs2} = 1.20$ V
$V_{gs1} = 0.98$ V	$V_{gs2} = 1.29$ V
$V_{gs1} = 0.92$ V	$V_{gs2} = 1.38$ V
$V_{gs1} = 0.88$ V	$V_{gs2} = 1.49$ V
$V_{gs1} = 0.86$ V	$V_{gs2} = 1.63$ V
$V_{gs1} = 0.81$ V	$V_{gs2} = 1.72$ V
$V_{gs1} = 0.80$ V	$V_{gs2} = 2.01$ V
$V_{gs1} = 0.79$ V	$V_{gs2} = 2.58$ V
$V_{gs1} = 0.79$ V	$V_{gs2} = 3.65$ V
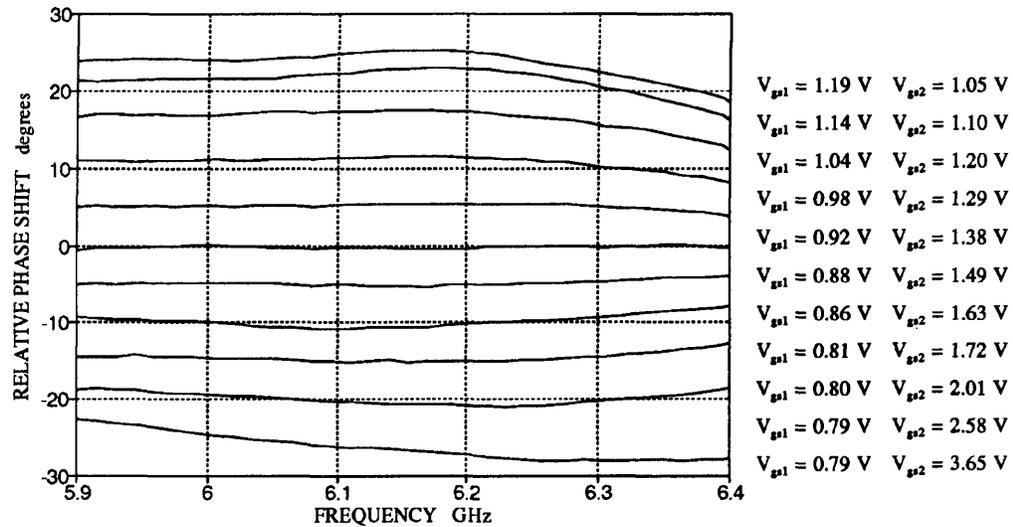
Fig.6.27 Phase response of the GaAs FET phase shifter

In practice, it was proved complicated to map the phase shifter due to the nonlinear behaviour of Fig.6.19 and because each transistor has different characteristics. The control voltages corresponding to the phase states of Fig.6.27 are given in Fig.6.28(a). The apparent difference in the level of the required gate voltages is due to the devices manufacturing tolerances. The drain currents give a more reliable indication of the bias conditions required as shown in Fig.6.28(b). The devices were biased at low gate voltages because of the better control of gain and phase at low drain currents. These results agree with the ones predicted in [123] and presented in Fig.6.19, where it is shown that in order to cover a large phase range the transistors have be biased near pinch off. Although this allows $50°$ phase change, the gain of the phase shifter is greatly reduced, as seen in Fig.6.29. Furthermore, the resulting gain ripple is +/- 1.7 dB. The phase ripple is, also, quite high as shown in Fig.6.27. Although this level of amplitude

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and phase ripple is of the same order as the practical dual gate FET vector modulators reported in the literature[115] such levels of ripple are unacceptable for use in a feedforward linearizer. It should, also, be noted that for the 50° phase change the transistors have to be biased away from their optimum point of Fig.6.20 resulting in reduced output power.

(a)

(b)
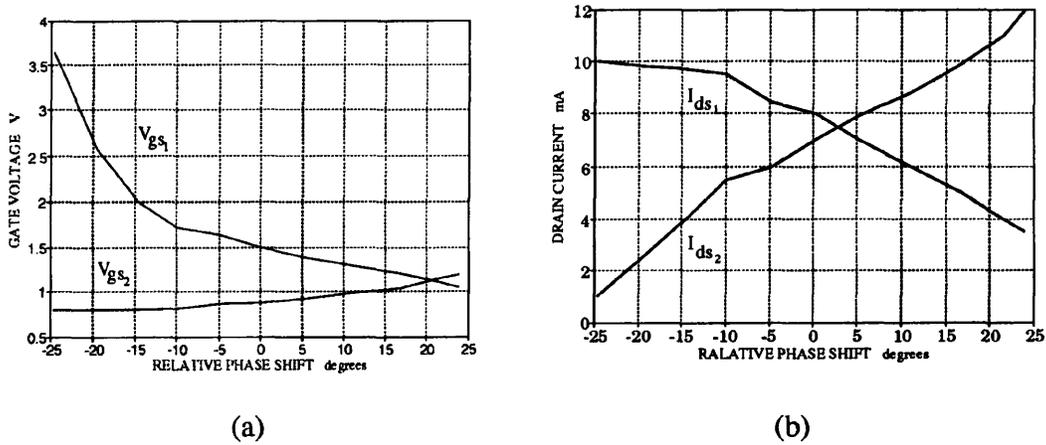
Fig.6.28 (a) Gate control voltage (b) drain current for various phase shifts
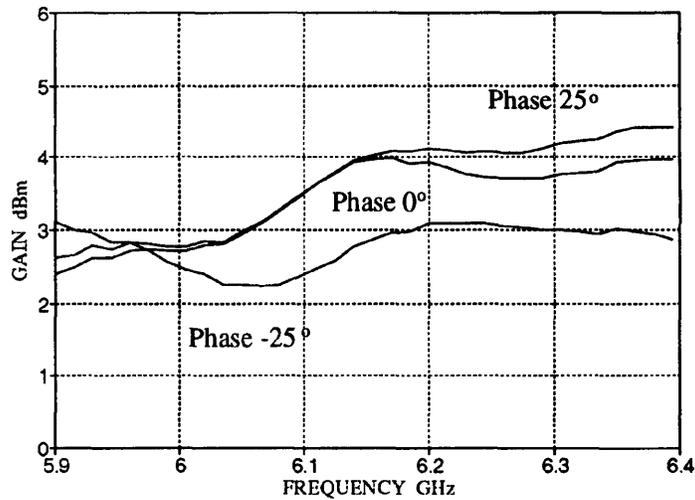
Fig.6.29 Gain of the FET phase shifter for various phase states

In order to allow for more gain, higher current bias conditions and flat phase response across the band, it was decided to bias the transistors such that a phase range of only +/-10° was obtained. The relative phase shift for 17° phase range is shown in Fig.6.30. The associated gain was 9.5 dB with a ripple of +/-0.1 dB for the various phase states. The control voltages for 20° phase range are shown in Fig.6.31.

S12/M1   ∠
REF 0.0 °
∠   2.0 °/
∇   -42.572 m°

START   5.500000000 GHz
STOP   7.000000000 GHz
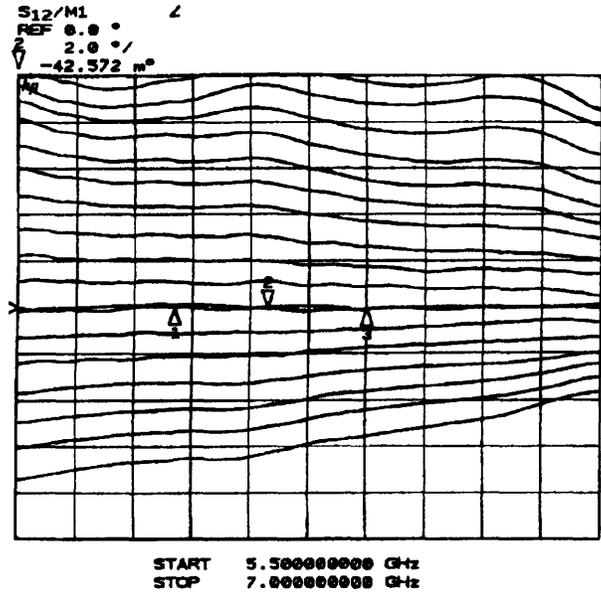
Fig.6.30 Phase response of the FET phase shifter
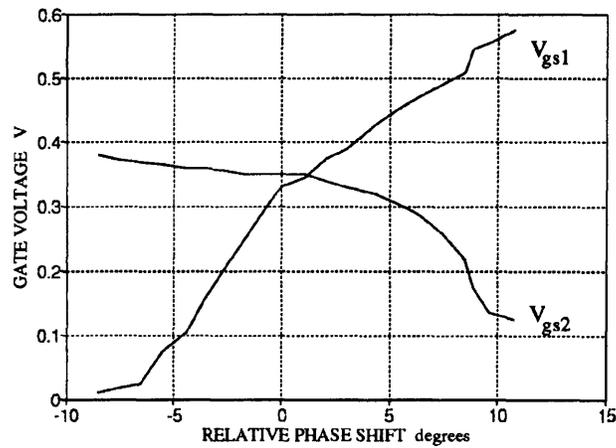
Fig.6.31 Control voltages for the various phase shifts of Fig.6.30

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6.6 Discussion

The phase and amplitude balance achieved in the feedforward loops determines the cancellation that can be achieved by a feedforward linearizer circuit, as discussed previously in chapter 4. Therefore, it is necessary to employ a kind of phase and amplitude control circuit in each loop in order to compensate for fabrication tolerances. The vector modulator circuits evaluated in this chapter are a PIN diode and a single gate GaAs FET quadrature phase shifter.

The FET phase shifter power rating does not allow this circuit to be placed at the arm A of the first loop (Fig.3.1). Furthermore, if this phase shifter is placed at the input of the main amplifier it imposes requirements for high gain auxiliary amplifier. From eq.3.6 the gain of the auxiliary amplifier is approximately equal to the gain of the main amplifier plus the output coupling ratio. The auxiliary amplifier described in section 5.3 has a gain of 36 dB. The main amplifier described in section 5.2 has a gain of 26 dB. If this gain is increased by cascading the FET phase shifter and the main amplifier, a further gain stage is required for the auxiliary amplifier or very tight coupling for the output coupler. The tight coupling, however, would reduce the efficiency of the system according to eq.4.30. It was, therefore, decided to employ the FET phase shifter at the input of the auxiliary amplifier. The signals entering the phase shifter at this point of the circuit consist of the residual carriers and the main amplifier's intermodulation distortion. The power rating of the phase shifter is high enough to handle them.

The inherent high loss of the diode phase shifter restricts the use of this element at the input of the main amplifier because it would reduce significantly the main signal gain. If, however, the diode phase shifter was employed at the arm A of the first loop its loss would only impose requirements for higher coupling ratios for the second coupler and, according to eq.3.3, would require higher gain for the auxiliary amplifier. Employing the FET phase shifter, which has a gain of 9.5 dB, at the input of the auxiliary amplifier compensates for this loss. It was therefore, decided to employ the PIN diode phase

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shifter at the arm A of the first loop. However, this path is used as a reference and the distortion introduced in it should be kept very low. Nevertheless, when this configuration was decided the nonlinearity of the PIN diode had not yet been evaluated. As explained in section 6.4.4, the practical PIN diode phase shifter produced much higher distortion than expected. Time limitations did not allow for a change in the linearizer configuration layout or an extensive research for the optimum PIN diode for linear phase shifters. Instead, it was decided to replace the diodes with resistors. To adjust the phase shift, different values of resistors were soldered on the circuit. This solution, although crude, was successful for implementation in the final practical linearizer circuit.

6.7. Conclusions

In this chapter the design, fabrication and performance evaluation of phase and amplitude varying circuits has been presented. The practical evaluation of the Schiffman phase shifter and of the associated CAD model showed that this circuit can be reliably used in the experimental linearizer circuit to produce the required fixed phase shift between the two paths of the feedforward loops. Furthermore, optimization of this element allows one path to tailor the phase response of the other, as has been explained in section 3.6. However, variable phase and amplitude circuits are, also, necessary. The configuration investigated was the quadrature phase shifter.

A PIN diode and a single gate GaAs FET quadrature phase shifter were designed and practically evaluated. In order to keep the insertion loss at low levels and the phase and amplitude response flat, the allowable phase variation was limited within +/-10°. This range of phase change should be adequate to compensate for fabrication tolerances. The PIN diode phase shifter exhibited high nonlinearity and was not appropriate for use in the feedforward circuit. The problem was overcome by using the appropriate resistors to replace the diodes in the phase shifter circuit. The performance of the FET phase shifter, however, was satisfactory and it was, therefore, employed in the experimental linearizer circuit.

CHAPTER 7

Computer Aided Design and Construction of the Experimental Linearizer

7.1 Introduction

The computer aided design of the practical feedforward linearizer is described in this chapter. The initial calculations were based on the fundamental design criteria established in chapter 3. Given the specific measured performance of the linearizer components described in chapters 5 and 6, the initial values for the remaining circuit parameters were calculated employing the equations presented in section 3.2. Further optimization of these circuit parameters was performed to obtain the optimum balance in the feedforward loops across the 5.9 - 6.4 GHz frequency band.

In order to incorporate the measured data in the design, an optimization method similar to the one described in section 3.6 was developed. The method allowed a linear approach to the CAD optimization of feedforward linearizers[97] and is further described in detail in section 7.3. The values for the optimized parameters are, also, provided. The predicted cancellation of the simulated linearizer was better than 25 dB for the first loop and better than 22 dB for the second loop. These levels of cancellation are within the required limits discussed in section 5.1 and should result in an overall effective cancellation of at least 20 dB.

The overall layout, assembly and construction details of the optimized practical linearizer are provided in the two last sections of this chapter.

7.2 Design Considerations

The design, construction and performance evaluation of the major components of the feedforward linearizer have been presented in chapters 5 and 6. The phase and amplitude response of these components determine the selection and operation requirements for the remaining system circuits.

The phase responses of the vector modulators described in sections 6.4 and 6.5 were measured employing the same procedure as for the measurements of the amplifiers. The characteristics of the individual components constructed and measured before the final design of the linearizer are summarised below:

Main amplifier

gain: (25.8 +/-0.5) dB

phase response: (-7.5 +/-1)° phase shift, 1.636 ns delay

Auxiliary amplifier

gain: (36.7 +/-0.25) dB

phase response: (-86.5 +/-2)° phase shift, 1.837 ns delay

Phase shifter in the first loop

gain: (-5.3 +/-0.15) dB

phase response: (-147 +/-1)° phase shift, 444 ps delay

Phase shifter in the second loop

gain: (9.6 +/- 0.1) dB

phase response: (-87 +/-1)° phase shift, 606 ps delay

These data were the starting point for the CAD design of the linearizer. Design calculations were based on the requirement for phase and amplitude balance in the feedforward loops as governed by the conditions implied by equations of section 3.2. The input coupler was a Wilkinson divider[38], for reasons explained previously in section 5.4. The coupling ratio of the second coupler was, therefore, derived from eq.3.4

to be 32 dB. The coupling ratio of the output coupler was derived from eq.3.5 to be 15 dB. For these initial calculations a loss of 1 dB in the microstrip delay lines was assumed.

The measured components were incorporated in the design represented by their measured S parameter values. This representation did not include their delay time which was separately modeled with an ideal delay element[111]. Schiffman phase shifters[109] were employed to compensate for the phase shift in the components of each loop and microstrip lines to compensate for the delay time in each component.

Since linear CAD techniques were employed, an optimization method that allows a linear approach to the design of linearizers was developed. The procedure adopted for the optimization of the overall system is described next.

7.2 Linear Approach to the Optimization of Feedforward Linearizers

Ideally, feedforward linearizers, being nonlinear circuits, should be designed and optimized using nonlinear CAD software. However, a limited number of nonlinear device models is available in such programs. This is a restricting factor for the amplifiers and nonlinear systems that can be analyzed in this way. One immediate limitation of the Eesof CAD software, used in the work carried out in this thesis, is the lack of nonlinear models for any packaged devices. A method of optimizing the feedforward circuit employing linear CAD techniques was, therefore, developed to allow the design of the experimental linearizer.

The method is based on the requirement that the feedforward loops operate linearly and independently. In practice, the cancellation achieved in the first loop affects the operation of the second loop through the nonlinear behaviour of the auxiliary amplifier, as explained in detail in chapter 4. If, however, the auxiliary amplifier is correctly

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selected, the performance of the overall linearizer will primarily depend on the phase and amplitude balance within the feedforward loops.

Independent analysis of the two loops allows the feedforward linearizer performance to be optimized over the desired frequency range using a linear CAD program and small signal measurements.

7.2.1 First Loop Optimization

The individual components were intergrated into a complete model of the first loop as shown in Fig.7.1.
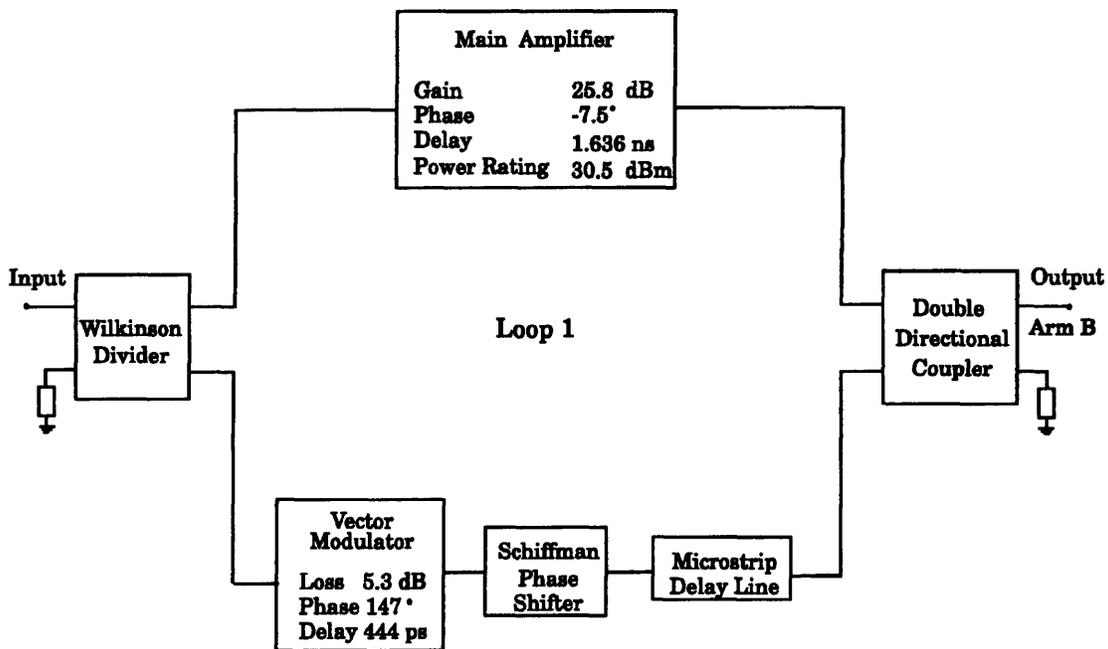
Fig.7.1 Block diagram of the first loop

The first loop compares the output of the main amplifier with a reference signal proportional to the input. Gain compression, phase distortion and intermodulation resulting from the nonlinearity of the main amplifier, contribute cumulatively to the error signal generation. Thus, for a single frequency input signal the error signal should be zero at the output of the loop, if the first loop is correctly set up and the amplifier is

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operating at its linear region. The circuit was, therefore, optimized to give a minimum output at the arm B of the second coupler over the 5.9 - 6.4 GHz frequency band. The elements allowed to vary in the optimization process were the length of the microstrip delay line, the phase of the Schiffman phase shifter and the coupling ratio of the second coupler. In order to ensure good matching for the optimized components their parameter values were restricted to provide a return loss better than 20 dB. The predicted optimum cancellation for the first loop is better than 25 dB as shown in Fig.7.2
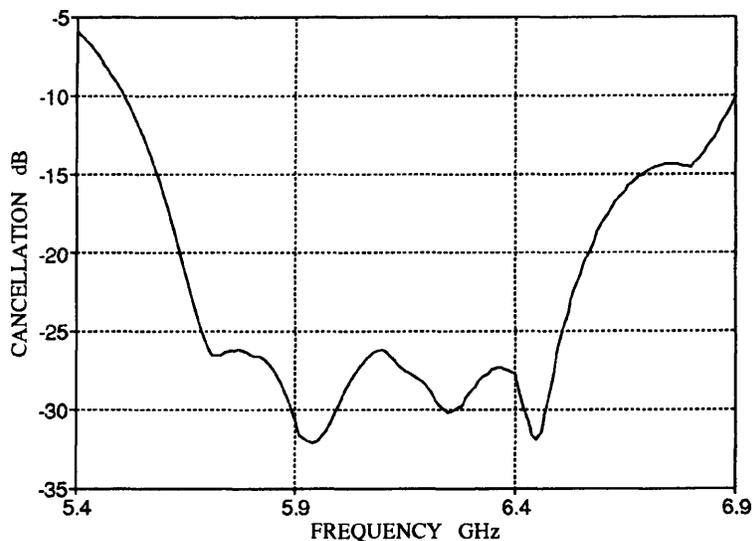
Fig.7.2 Predicted cancellation in the first loop

The required value for a Schiffman phase shifter employed in the first loop was 120°. High phase shifts, however, require tight coupling of the C-section line of the Schiffman phase shifter[109] (Fig.5.1). Because the limited PCB facilities at UMIST, coupled lines with high tolerance requirements for the width and spacing of the lines could not be reliably fabricated. It was, therefore, decided to employ two 60° Schiffman phase shifters which were, then, optimized independently.

Parameter values for the optimized components are listed below.

Double directional coupler 32.9 dB (parameters referring to Fig.5.13):
W = 1.22 mm
S = 0.41 mm
L = 8.80 mm
Schiffman phase shifters (parameters referring to Fig.3.11):
W_1 = 0.84 mm W_2 = 0.96 mm
S_1 = 0.26 mm S_2 = 0.37 mm
L_1 = 8.27 mm L_2 = 7.82 mm
Microstrip delay line (total time delay 1.287 ns):
L = 25.74 cm
Total loss in Schiffman phase shifter and delay line 1.4 dB

7.2.2 Second Loop Optimization

The objective of the second loop is to amplify the error signal to the required value and subtract it from the output of the main amplifier. If the second loop is considered independently of the first loop and the arm A input to the second coupler is terminated to a matched load, as shown in Fig.7.3, then the error signal presented to the auxiliary amplifier will be directly proportional to the signal in arm B of the loop. The resultant output should be a null for a correctly adjusted loop.
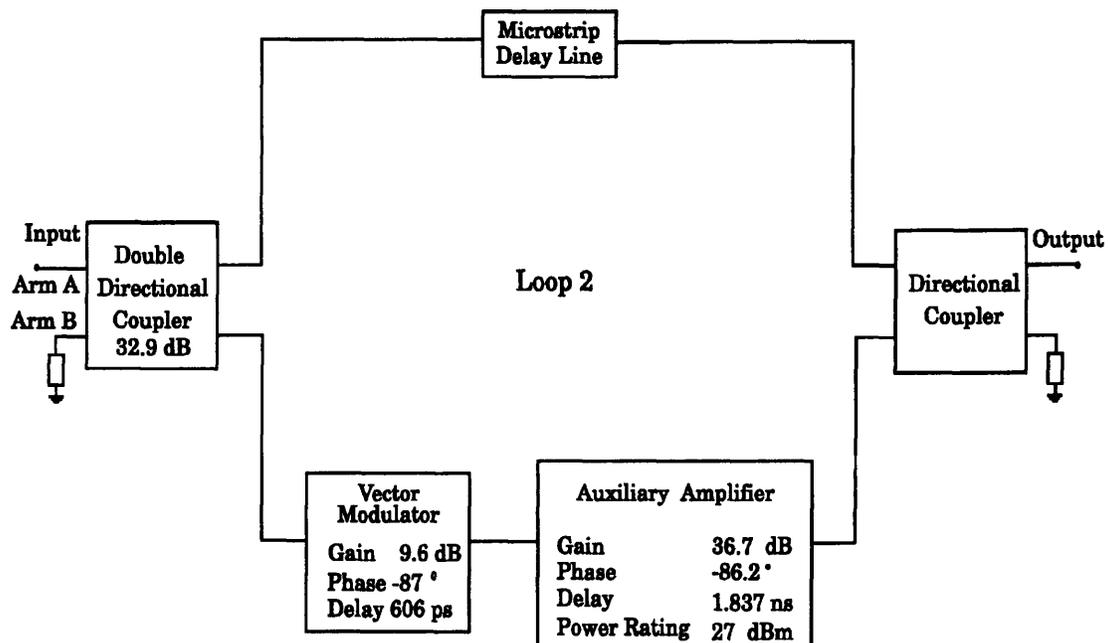
Fig.7.3 Block diagram of the second loop

The optimized elements were the length of the delay line and the coupling ratio of the output coupler. The required phase for a Schiffman phase shifter was only 2°. It was therefore, decided not to employ such an element in the second loop. The target of the optimization was a minimum at the output of the circuit over the full operating bandwidth with the restriction of a 20 dB match for the optimized components. The predicted cancellation for the second loop is better than 22 dB, as shown in Fig.7.4. Parameter values for the optimized components are listed below.

Directional coupler 14.8 dB (parameters referring to Fig.3.9):
W = 1.05 mm
S = 0.26 mm
L = 9.02 mm
Microstrip delay line (time delay 2.573 ns):
L = 52.28 cm
Total loss 2.1 dB
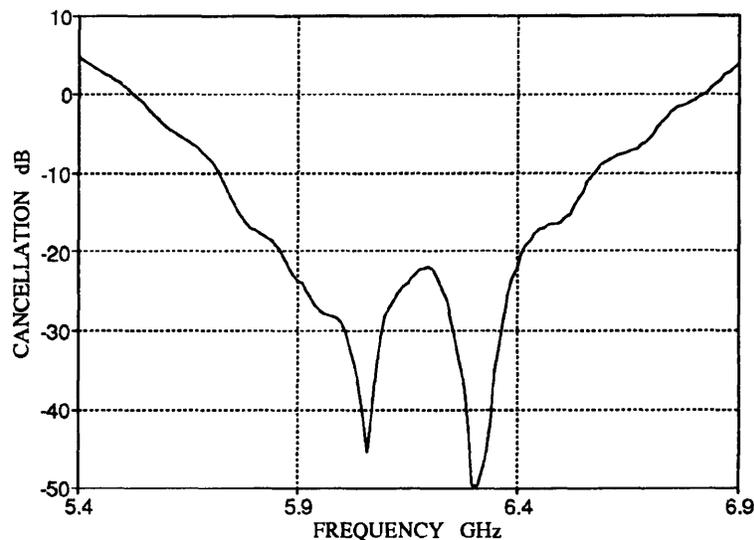
Fig.7.4 Predicted cancellation for the second loop

7.2.3 Discussion

The optimization method presented in the previous sections allows a linear approach to the design of feedforward linearizers. Any distortion introduced by the main amplifier

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is seen as deviation from the reference signal and is corrected. This feedforward correction would result in suppression of the intermodulation products as well as correction of any phase and amplitude nonlinear behaviour. However, as the output power of the main amplifier increases, its distortion becomes significant and the error signal fed into the auxiliary amplifier will produce further intermodulation products and will, consequently, deteriorate the effective cancellation as expressed by eq.4.16. Therefore, the optimization method described in the previous sections 7.3.1 and 7.3.2 results in the optimum feedforward correction up to the point where the auxiliary amplifier starts to significantly deteriorate the performance of the linearizer.

The method developed in chapter 3 for the design of the simulated linearizer accounts for the nonlinear behaviour of the amplifiers in order to compensate for high power operation. The nonlinearity of the amplifiers is regarded as an extra phase and amplitude imbalance which is compensated for by adjusting the phase and gain/loss of the other linearizer components. This relaxes the requirement for high power rating of the auxiliary amplifier and results in better cancellation of the intermodulation products in the second loop. It does not, however, result in the optimum correction of the gain compression and phase distortion.

The Computer Aided Design of the experimental linearizer was based on the small signal performance of the various components. Alternatively, large signal S parameter measurements could have been incorporated in the design to allow optimization of the circuit for a specific output power level. However, this was not considered necessary for the design of the linearizer. This is justified because typical values for the phase distortion given in Fig.1.3[10] and measured results in [83] indicate that Solid State Power Amplifiers produce only a few degrees of phase distortion. Such levels of phase distortion could be adjusted by the variable phase shifters employed in the linearizer circuit.

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7.4 Layout of the Optimized Amplifier

The layout of the optimized linearizer circuit is shown in Fig.7.5. The linearizer components were designed to be built on the 0.02" Rogers RT/Duroid material, type 5880. Since the amplifiers were fabricated on a similar material with a 0.125" aluminium backing the rest of the circuits were mounted on aluminium plates of 0.125". The various sub-circuits were isolated using metal walls to prevent coupling between the parallel paths of the feedforward loops and avoid wide cavities that support propagation in the operating band. This, however, was not always feasible. In order to avoid possible oscillation of the FET phase shifter due to its dimensions, the board was cut and metal blocks were placed on the ground plate to reduce the dimensions of the cavity around the gain stages. Sections of standard SMA connectors that consisted of uncovered PTFE material and the central conductor pin were employed though a hole in the aluminium walls to provide connection between the linearizer components. This element was modelled in the CAD optimization as a 50 Ω coaxial line with 4 mm length which was the thickness of the metal walls employed in the practical linearizer.

In the design the final linearizer layout, provision was made to allow breaking the feedforward loops at the appropriate places, in order to enable a practical set-up procedure similar to the optimization method described in section 7.3. This set-up method will be further discussed in the next chapter. The first loop delay line component consisted of three separate boards connected together with thin copper shims. In order to break this path, the two boards namely D1 and D2 were replaced by circuits with the same dimensions consisting of 50 Ω resistors connected to ground. Radial $\lambda/4$ open circuits stubs were used to provide the RF ground. Furthermore, a number of circuits with different length delay lines were fabricated having the same dimensions as the board D1. This way the overall delay introduced in this path of the loop could be adjusted to allow for fabrication errors greater than +/-10° which was the allowable phase range of the practical phase shifters. Similar provisions were made for the second loop. The replaceable boards are shown in Fig.7.5 marked as D3 and D4.

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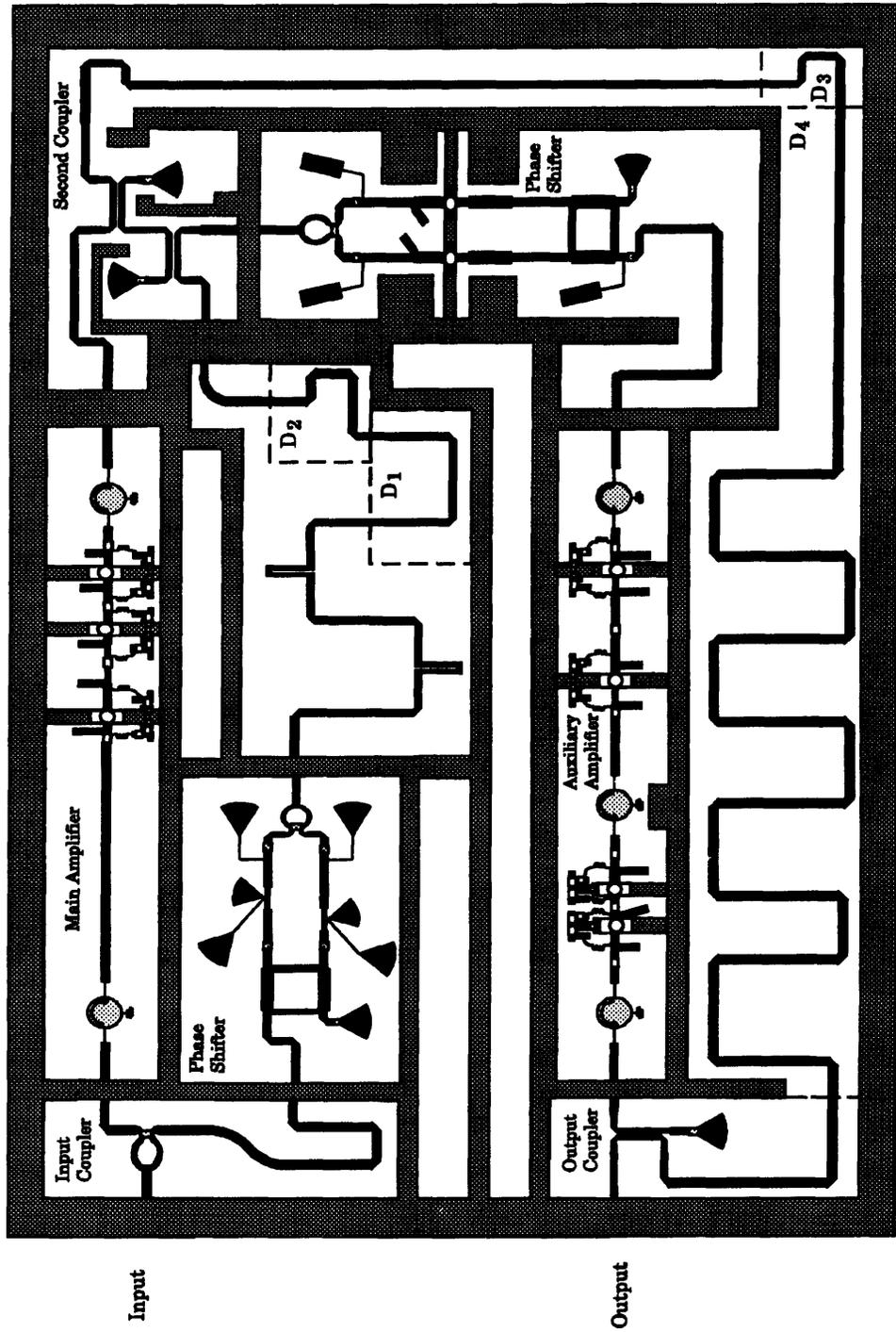
Fig.7.5 Layout of the experimental linearizer

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The overall dimensions of the linearizer circuit were 24x16.7 cm³. Aluminium lids were fabricated to cover different sections of the circuit. The choice of the area covered by the same lid was based on the requirement for accessibility of the boards that allowed the loop delay adjustment and breaking of the loops.

7.5 Construction

The linearizer aluminium case was constructed in the mechanical workshop, Ferranti building, at UMIST. The dimensions of the case were 24.8x17.5x5.3 cm³. The height of the box was designed to accommodate the microwave circuit isolated by four lids from the DC circuit which was mounted on the top lid. Standard SMA connectors were used at the input and output ports. The practical circuit is shown in Fig.7.6.
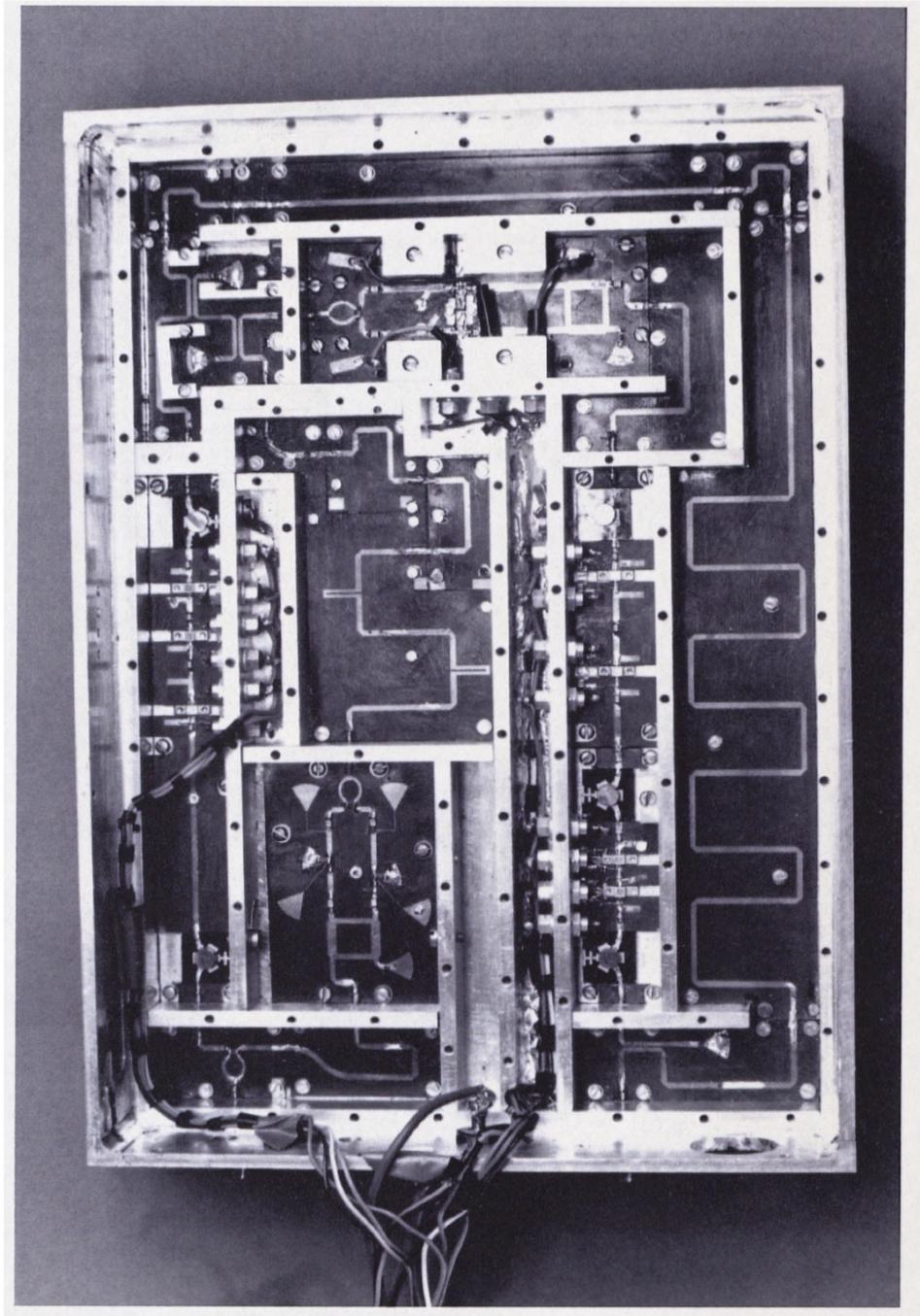
Fig 7.6 Experimental linearizer

CHAPTER 8

Assessment of the Experimental Feedforward Linearizer

8.1 Introduction

The performance of the experimental linearizer is evaluated in this chapter. The cancellation of the nonlinear distortion due to the feedforward correction is first determined by two and three tone tests. A range of carrier combinations is employed to investigate the improvement in the intermodulation distortion over the full 5.9-6.4 GHz frequency range.

The improvement in linearity is, also, evaluated over a range of output power. In particular, the linearizer is optimized for operation at various power levels resulting in enhanced linearity in the vicinity of the optimum point of operation.

Finally, the carrier to intermodulation ratios of the linearized and the unlinearized amplifier are calculated and compared with the linearizer being optimized for two different output power conditions. The results clearly demonstrate that for systems requiring high linearity the feedforward circuit is an efficient configuration.

8.2 Practical Set-up and Optimization

The practical linearizer was set-up following a similar procedure as the one used in the CAD design of section 7.3. The measurements were performed on the HP 85107A network analyzer system for a single frequency input. In order to optimize each loop independently the feedforward paths were broken at points S_1 and S_2, Fig.8.1, and the circuit was adjusted to provide a minimum at the output of the linearizer.
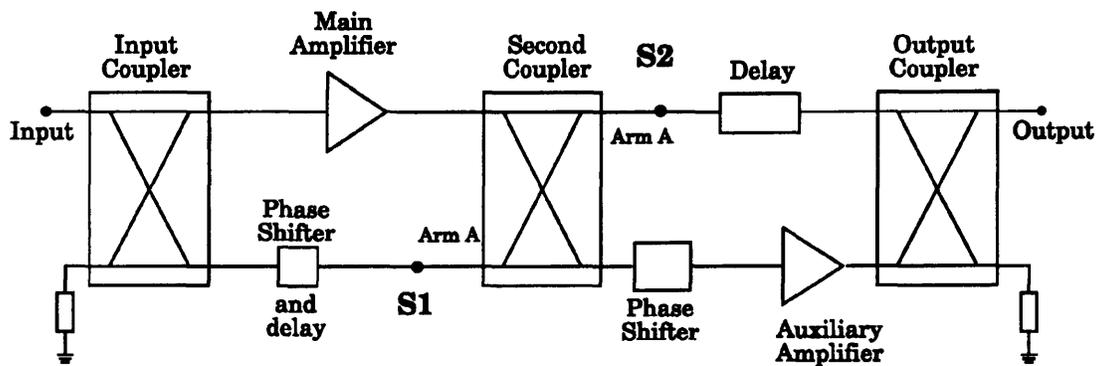
Fig.8.1 Block diagram of the feedforward linearizer

For the first loop optimization, the arm A of the second loop was broken by replacing part of the microstrip delay line with two 50 Ω terminations. The phase shifter in the first loop was adjusted to provide a minimum at the output of the circuit. The required delay for optimum phase balance in the first loop was measured to be $20°$ more than the one predicted from the CAD optimization. The board D_1 was therefore replaced by one with $20°$ longer microstrip line and two resistors 100 Ω and 120 Ω were used in the first loop vector modulator. The measured cancellation obtained in the first loop was better than 25 dB as shown in Fig.8.2.

Similarity, for the set-up of the second loop, the arm A of the first loop was broken by replacing part of the delay line with two 50 Ω terminations. The phase shifter of the second loop was, then, adjusted to provide a minimum at the output. The measured cancellation achieved in the second loop was better than 20 dB as shown in Fig.8.3.

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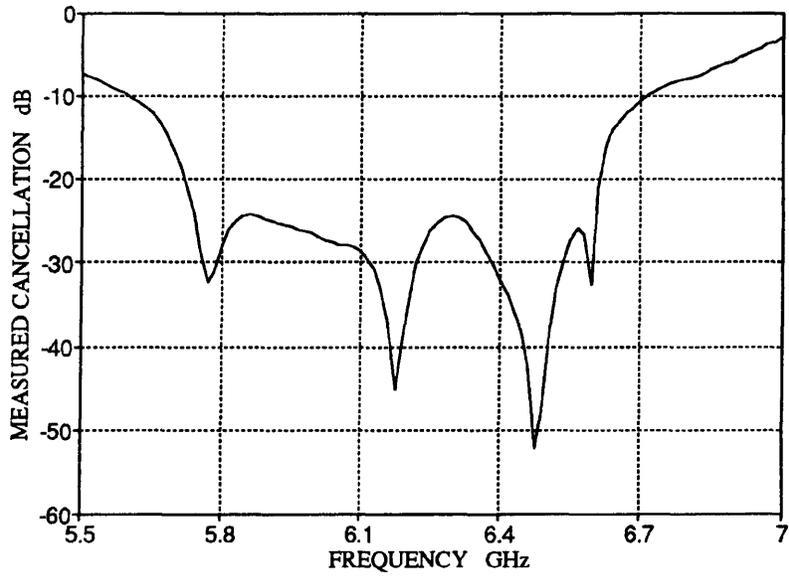
Fig.8.2 Measured cancellation for the first loop
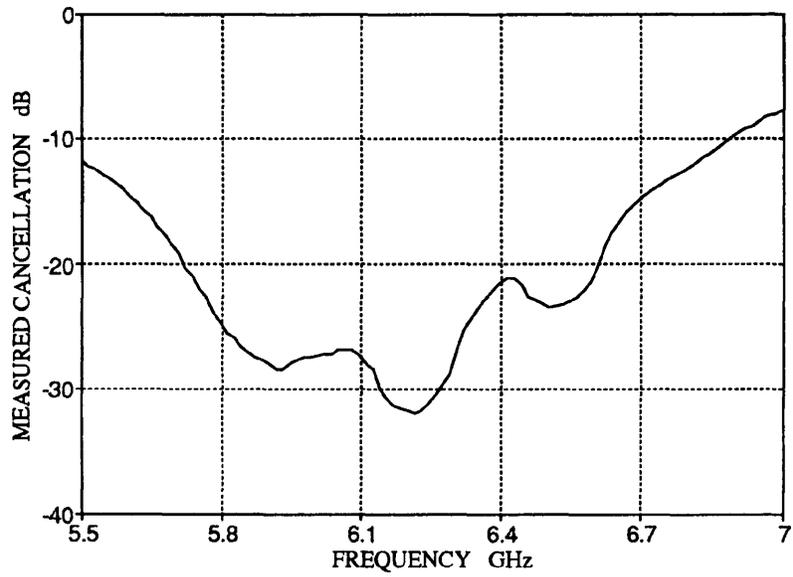
Fig.8.3 Measured cancellation for the second loop

The measured cancellation achieved in the individual feedforward loops of the practical linearizer is of the same order as the cancellation predicted by the CAD design described in section 7.2. According to the design graphs of section 4.3, these levels of cancellation should result in the desired 20 dB effective cancellation at the output of the linearizer.

8.3 Performance Evaluation of the Linearizer

Once the feedforward loops were set up and optimized independently, the feedforward paths were reconnected and the performance of the linearizer was evaluated by performing two and three tone tests to determine the effective cancellation of the intermodulation distortion products. The power characteristics of the linearizer were, also, measured to determine the effect of the feedforward circuit. The distortion of the main amplifier with and without feedforward correction was measured for a range of carrier combinations and for the linearizer circuit optimized for two different output power conditions.

The results presented in the next sections correspond to the closed and open loop configurations of the linearizer. To obtain the open loop configuration the feedforward correction path was disabled by switching off the auxiliary amplifier.

8.3.1 Two tone tests

The linearity of the system was first investigated by means of two tone measurements. Particular care was taken to ensure that the sources of the two tones produced distortion levels that were below those to be measured. For this purpose coaxial isolators with isolation better than 15 dB were employed at the output of each source to avoid coupling between the two signals.

The spectrum at the output of the feedforward amplifier with and without linearization is shown in Figs 8.4 - 8.7 for various frequencies and carrier separations within the 5.9-6.4 GHz band. At least 20 dB suppression of the intermodulation distortion was apparent. Furthermore, the results indicate that the intermodulation cancellation is neither dependant upon the frequency of the input signal nor upon the frequency separation of the input carriers.

8.3.2 Three tone tests

Three tone tests were also performed to evaluate the intermodulation suppression achievable by the feedforward linearizer. Again, two isolators and a 10 dB attenuator were employed at the output of the sources to avoid coupling between them.

A range of carrier combinations was employed to evaluate the distortion suppression capabilities of the feedforward circuit across the full operating band. Some of the results are presented in Figs 8.8-8.12. Again, at least 20 dB improvement in the intermodulation product level was achieved. The cancellation achievable with the linearizer did not show any dependence on the frequency or carrier separation.
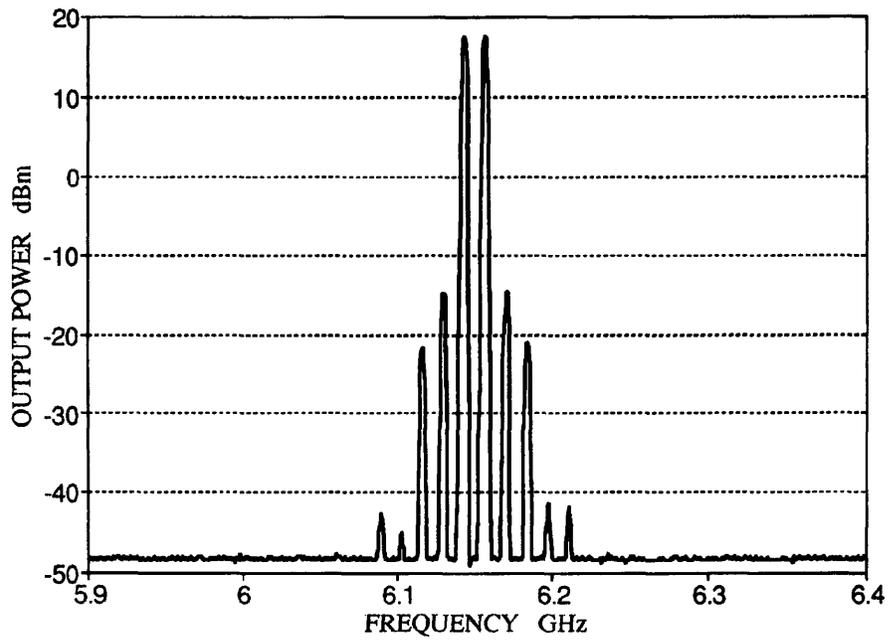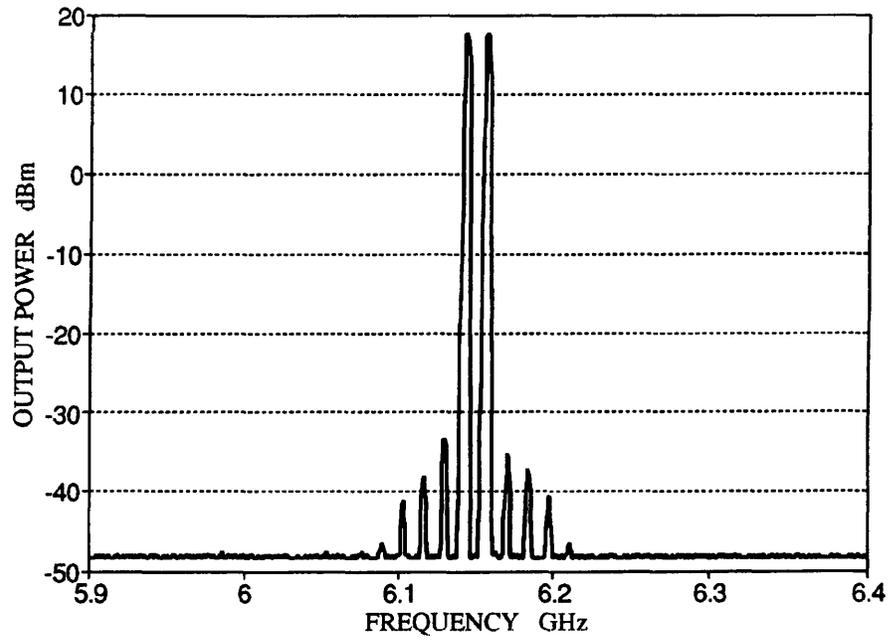
Fig.8.4 Output power with and without linearization F_1=6.14 GHz and F_2=6.16 GHz
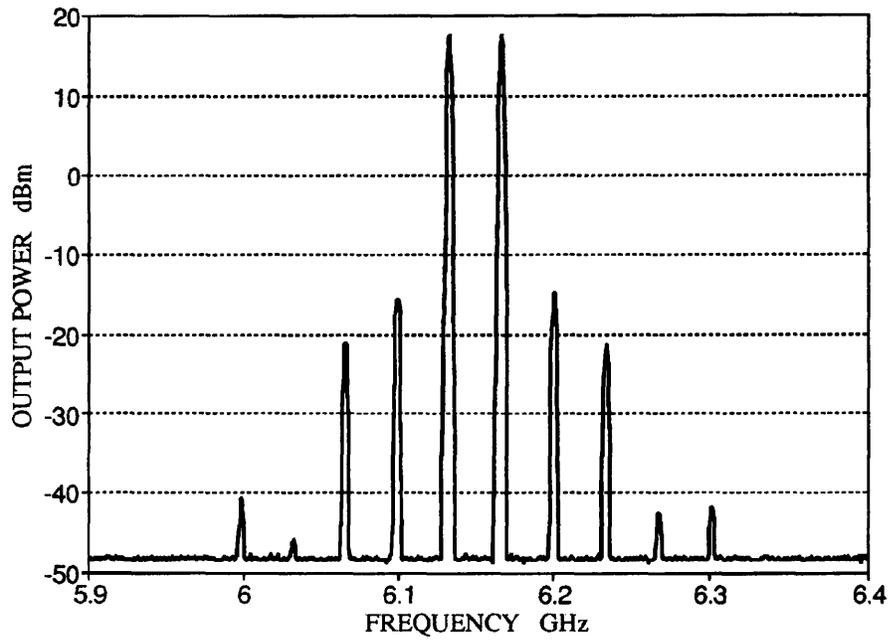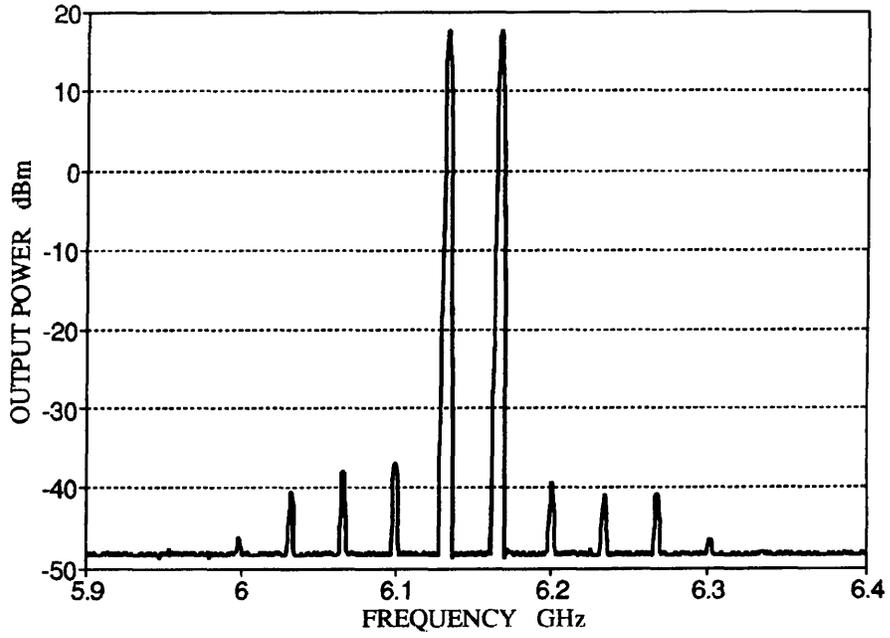
Fig.8.5 Output power with and without linearization F_1=6.13 GHz and F_2=6.17 GHz
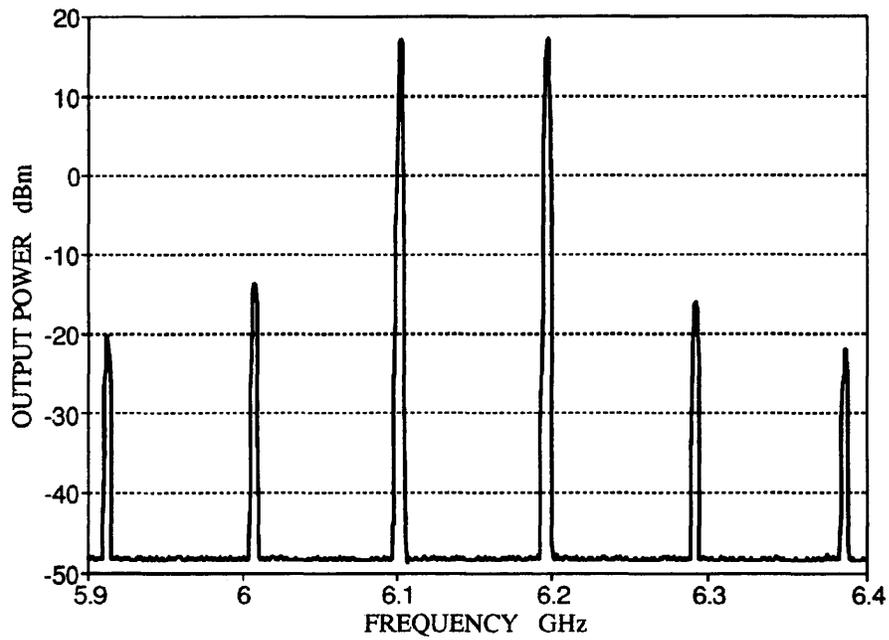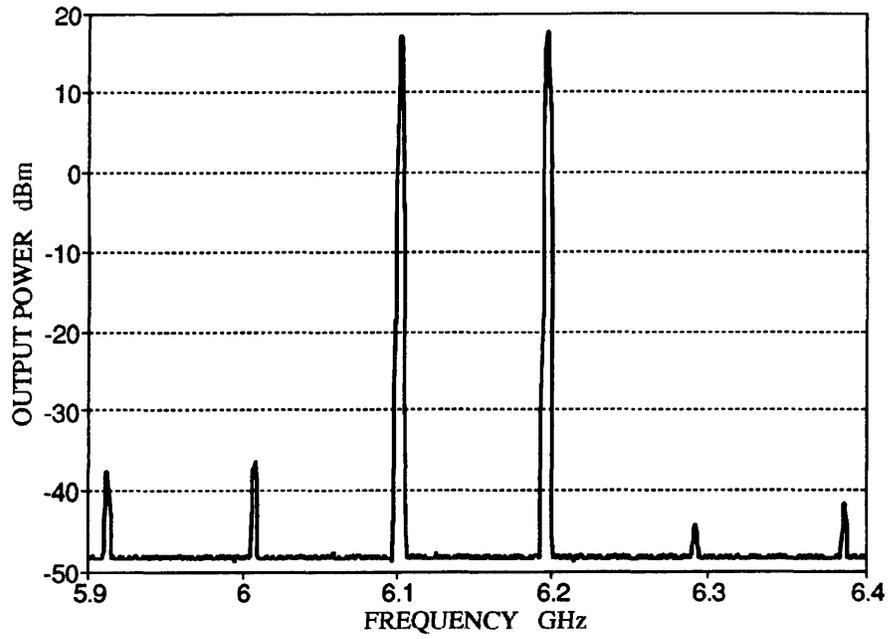
Fig.8.6 Output power with and without linearization F_1=6.1 GHz and F_2=6.2 GHz
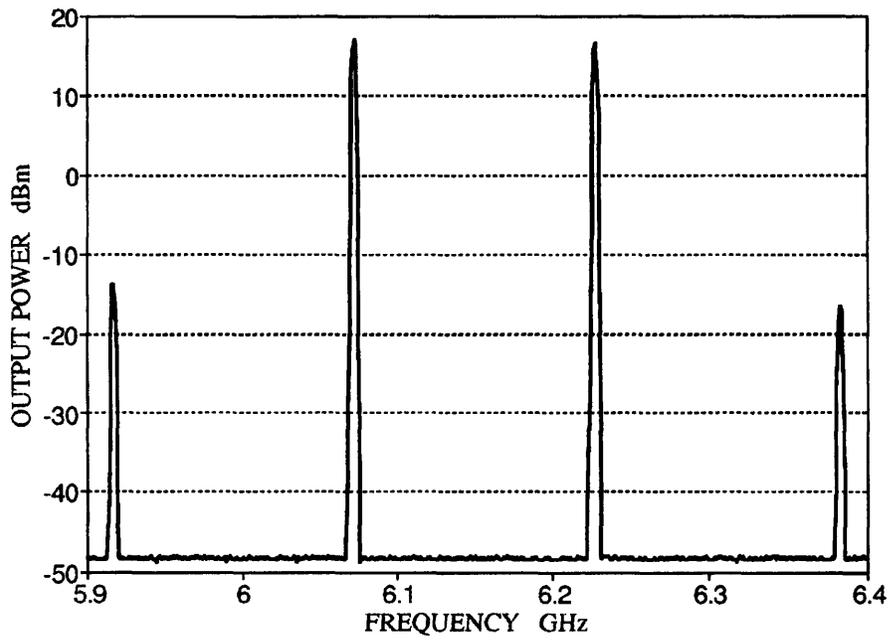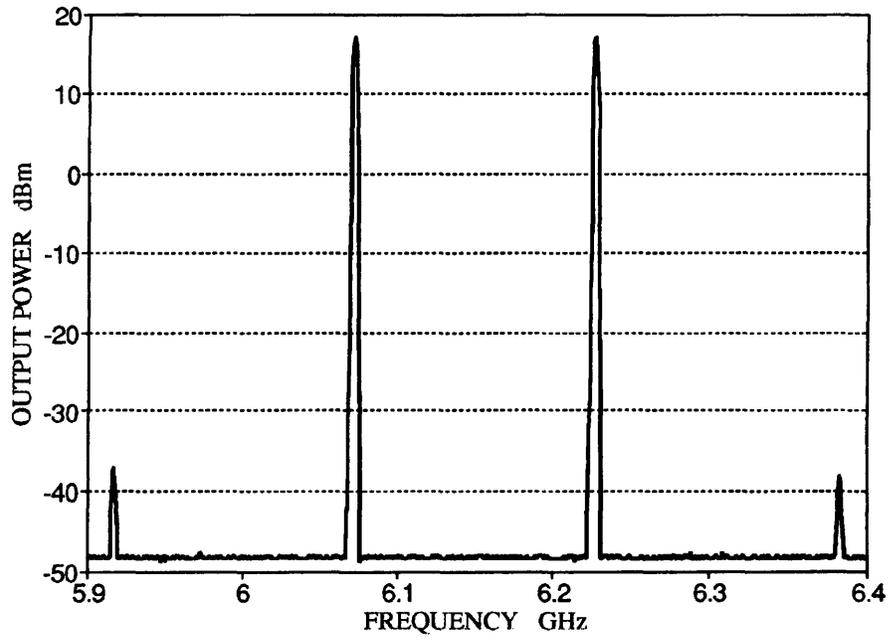
Fig.8.7 Output power with and without linearization F_1=6.07 GHz and F_2=6.26 GHz
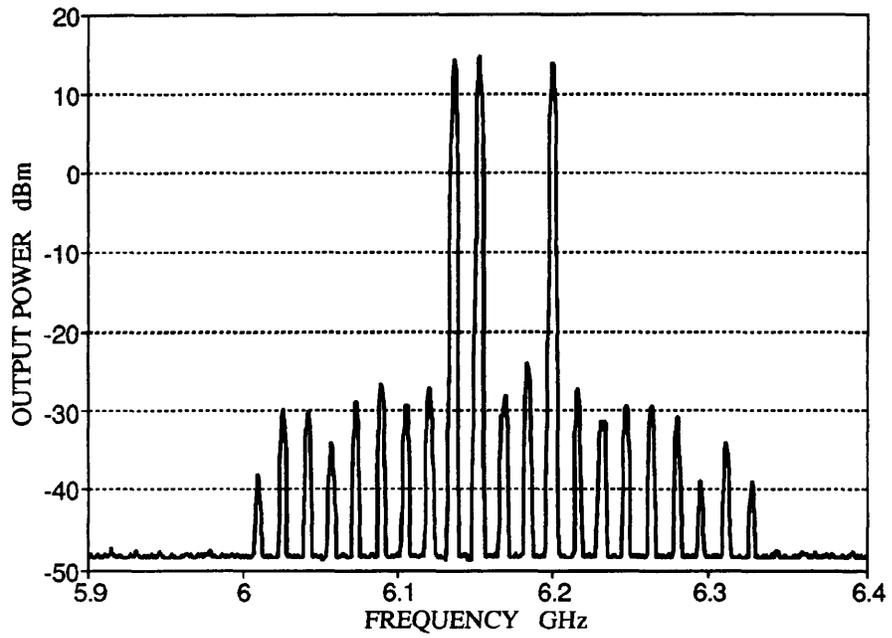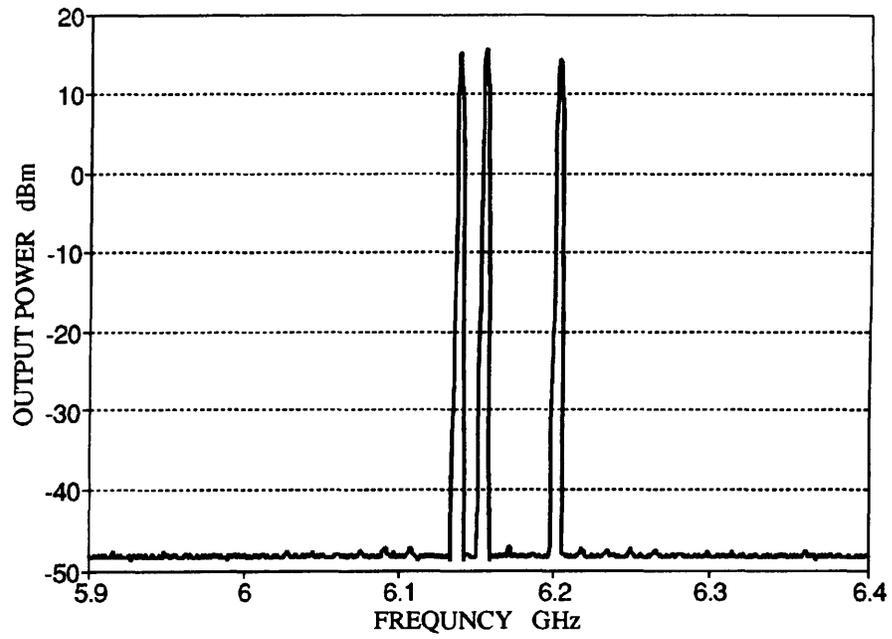
Fig.8.8 Output power with and without linearization $F_1=6.135$, $F_2=6.15$, $F_3=6.2$ GHz
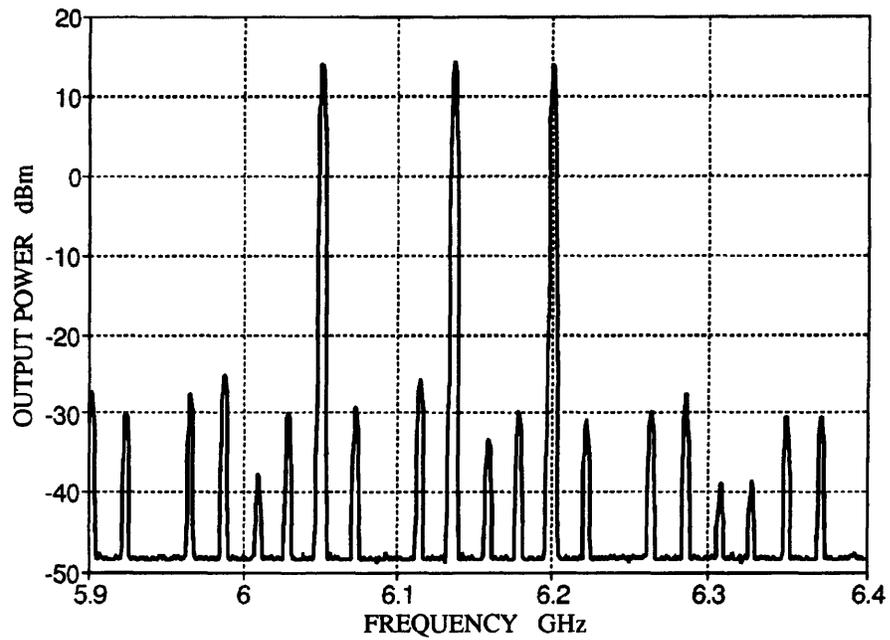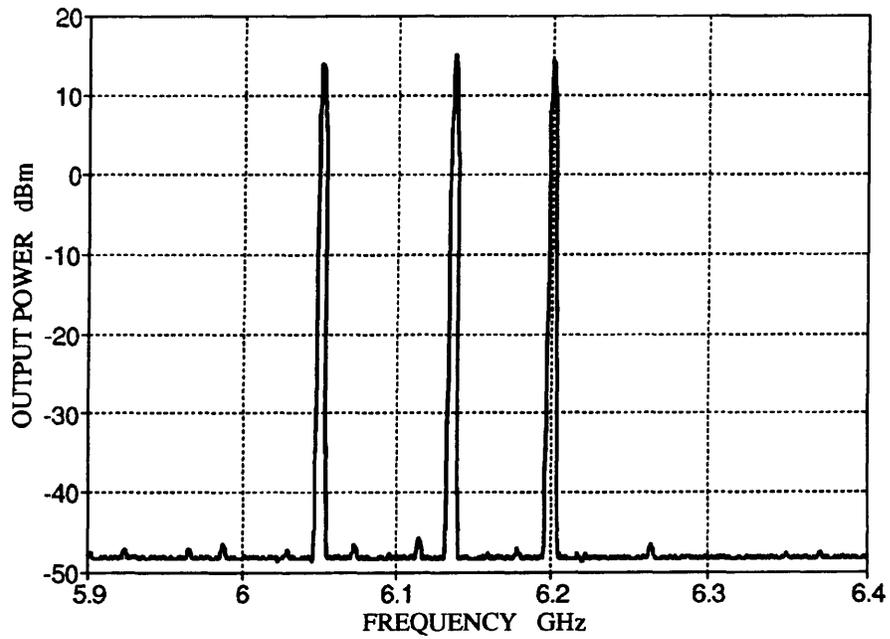
Fig.8.9 Output power with and without linearization F_1=6.05, F_2=6.135, F_3=6.2 GHz
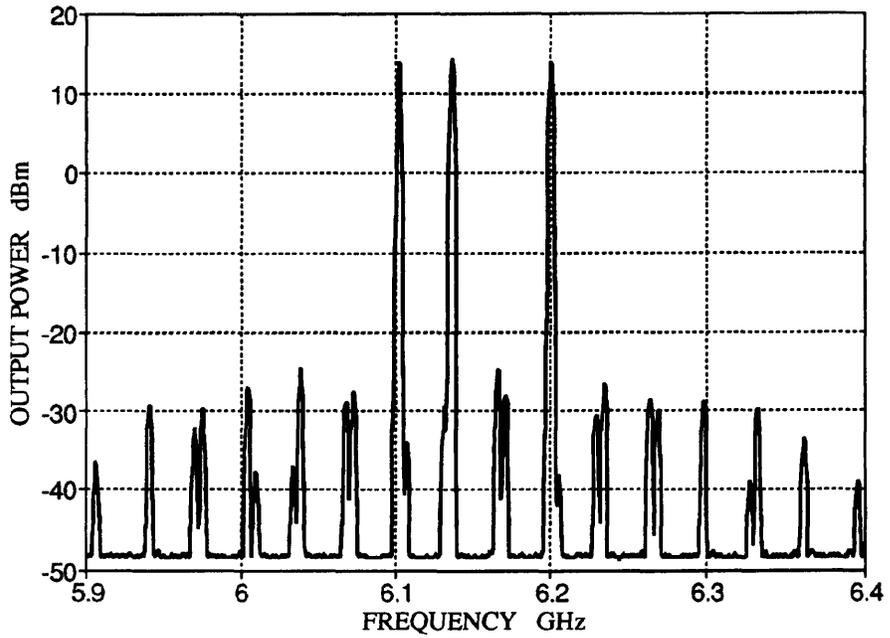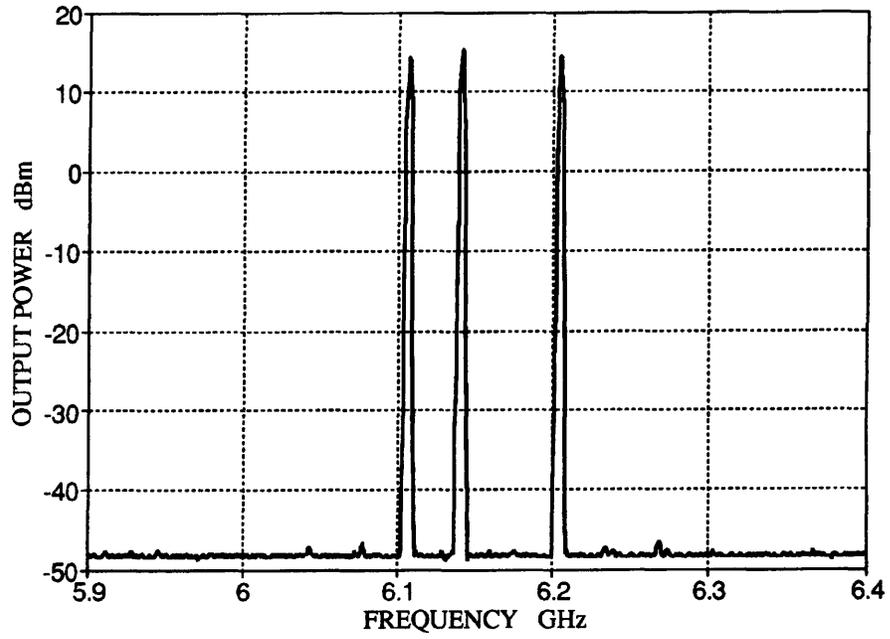
Fig.8.10 Output power with and without linearization $F_1=6.1$, $F_2=6.135$, $F_3=6.2$ GHz
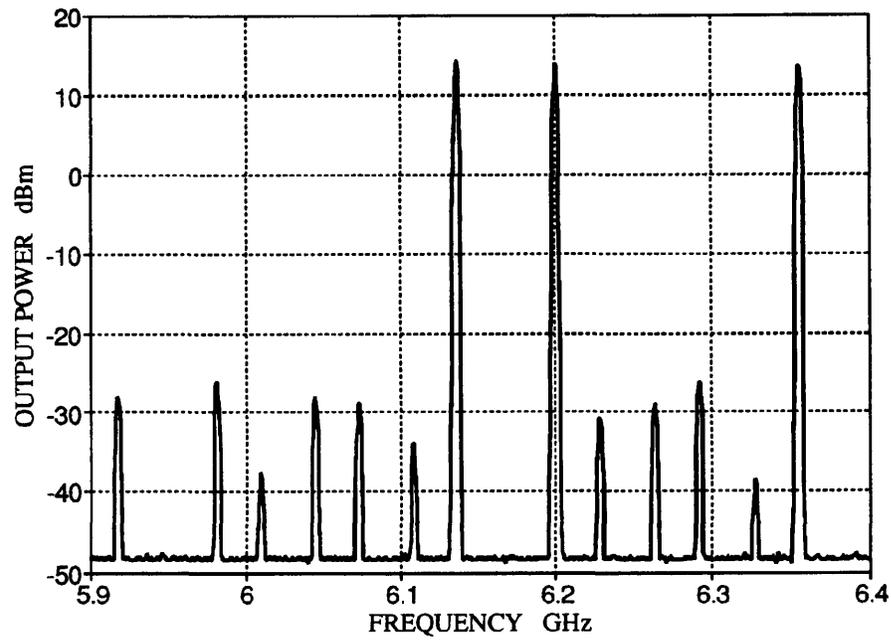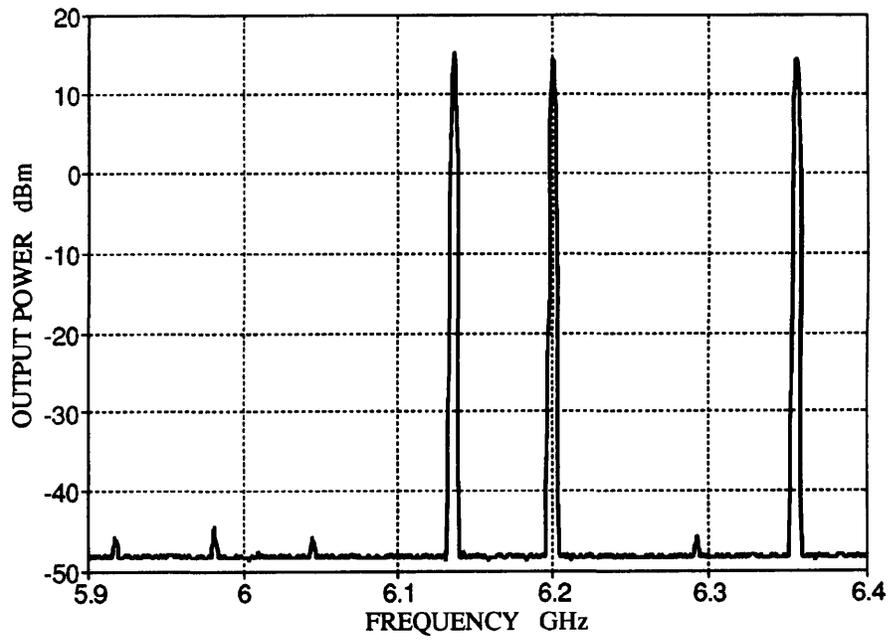
Fig.8.11 Output power with and without linearization F_1=6.135, F_2=6.2, F_3=6.35 GHz
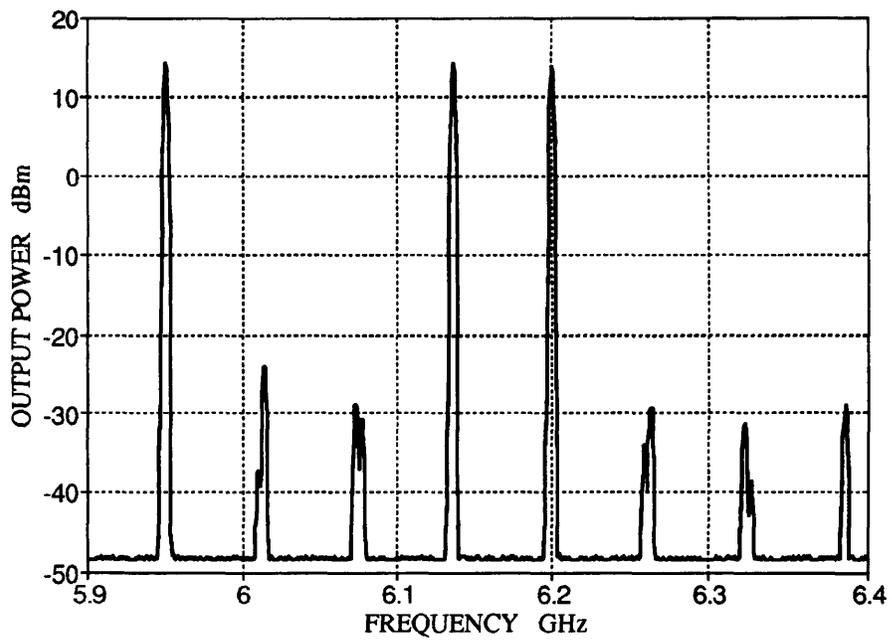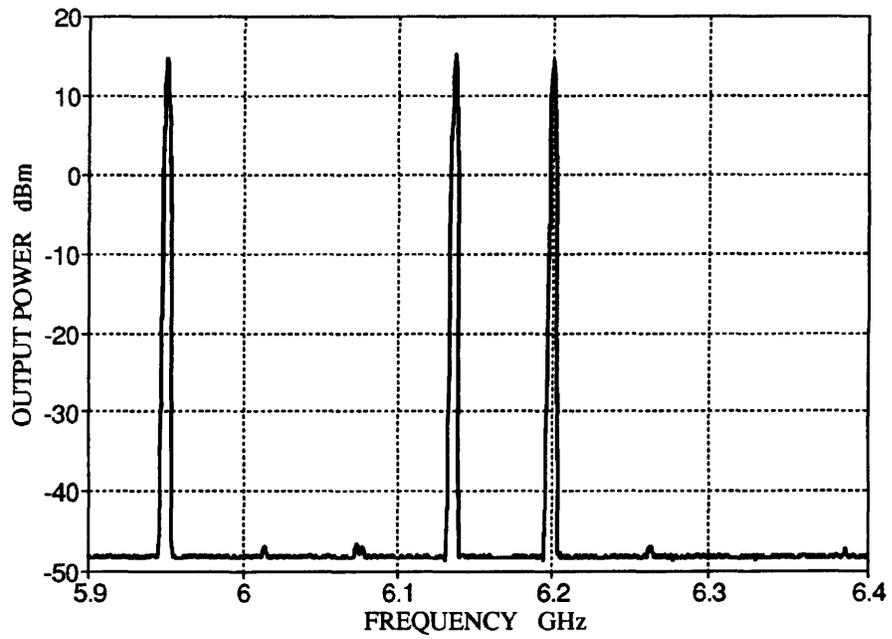
Fig.8.12 Output power with and without linearization F_1=5.95, F_2=6.135, F_3=6.2 GHz

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8.3.3 Power Characteristics of the Linearized Amplifier

In the initial set-up of the experimental linearizer the HP 85107A vector analyzer was used because it offers the facility of phase measurements. However, the signal sources of this equipment do not provide high enough power to drive the main amplifier into saturation. Therefore, for the optimization of the linearizer circuit at elevated output powers, the scalar analyzer Marconi 6000 was employed. Adjustments of the vector modulators in each loop resulted in a minimum output for the appropriate set-up described in section 8.2 and allowed the optimization of the circuit for various output power levels. Only small adjustments were required to obtain the same level of cancellation given in Figs 8.2 and 8.3 for small signal operation of the amplifiers.
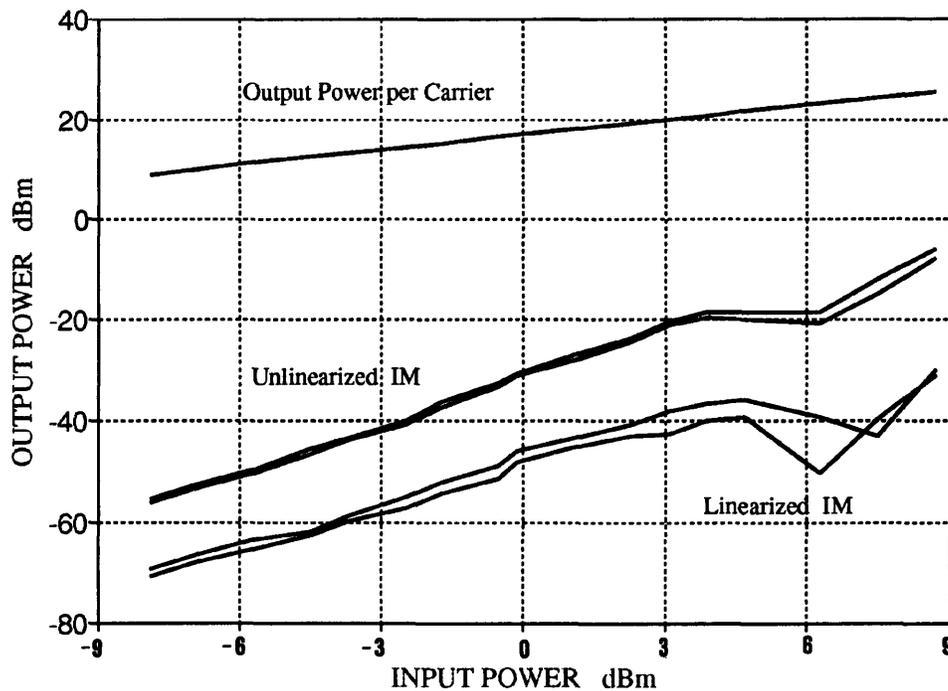
Fig.8.13 Third order intermodulation distortion with and without linearization

The intermodulation suppression for two different optimization power levels is shown in Figs 8.13 and 8.14 for a range of input power levels for two tone input signals at frequencies F_1 = 6.1 GHz and F_2 = 6.2 GHz. These figures clearly demonstrate that the feedforward circuit can be practically optimized for various operating conditions resulting in an further improvement in the performance of the order of 5 dB around the optimum point of operation.
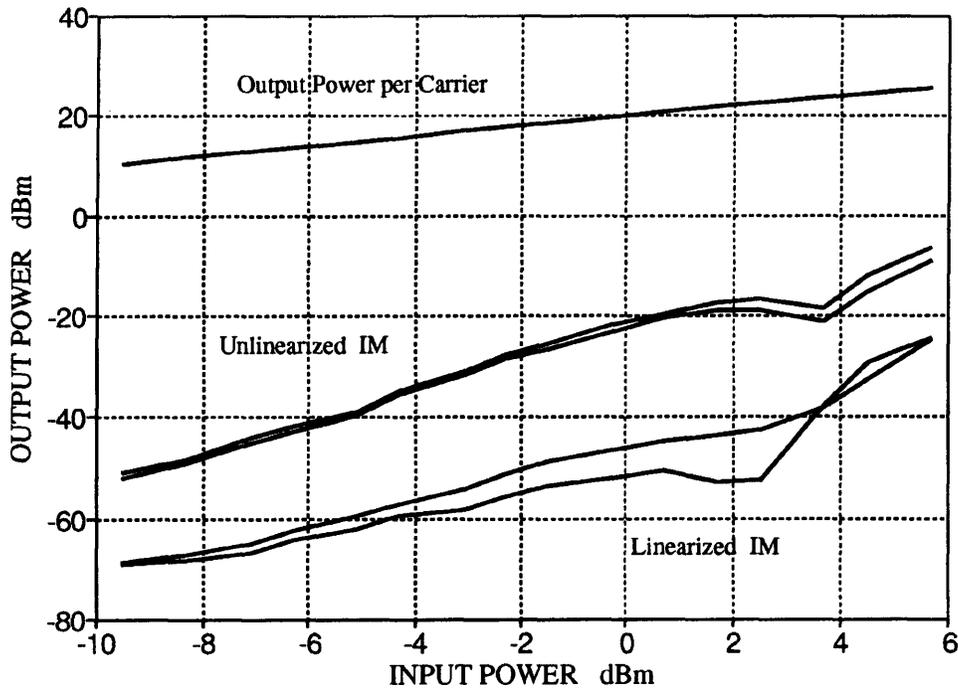
Fig.8.14 Third order intermodulation products with and without linearization

The power characteristics of the main amplifier with and without linearization were measured for a single tone input. The results are shown in Fig.8.15 for an input signal at 6 GHz and for the linearizer optimized for optimum performance at the saturation level. The sharper knee of the characteristic indicates that the linearity of the main amplifier has been improved with the feedforward correction. Furthermore, the saturation power of the main amplifier has been increased 1 dB with the linearizer circuit. This is because the circuit was optimized for operation at saturation level. However, this

comparison is misleading since feedforward linearizers are designed to improve the nonlinear distortion and not the power rating of the main amplifier. The output power of the feedforward amplifier when the second feedforward loop is open, is 28.3 dB. However, the measured output power of the main amplifier alone is 30.5 dB (Fig.5.12) indicating a loss of 2 dB in the output path microstrip delay line. This is in agreement with results obtained with the CAD analysis and presented in section 7.2.2.

The loss of linearized output power due to the second path delay reduces the system efficiency. However, this parameter it is not a prohibiting factor for the use of feedforward amplifiers because of the excellent linearization results obtained by the feedforward circuit. Evaluation of the overall system efficiency is attempted in the next section.
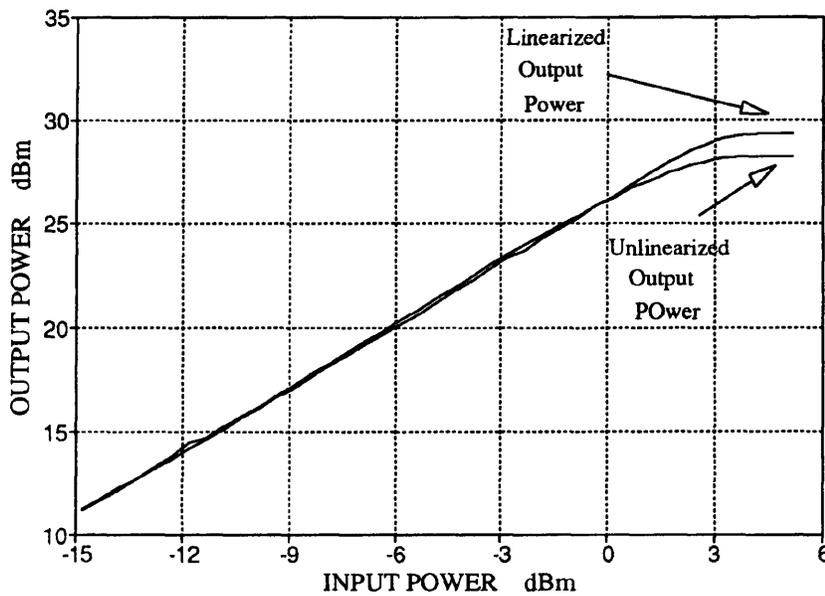
Fig.8.15 Output power with and without linearization

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8.3.4 Efficiency Calculations

The advantages of feedforward linearization are better appreciated if high linearity is required for the power amplifier. To evaluate the efficiency improvement due to the feedforward linearizer, the carrier to third order intermodulation ratio was calculated for two tone input signals at frequencies $F_1 = 6.1$ GHz and $F_2 = 6.2$ GHz. Two cases were investigated. Firstly, the linearized amplifier was optimized for operation 0.6 dB below saturation level as shown in Fig.8.16 and secondly, the linearizer was adjusted for optimum performance 4 dB below saturation level, as shown in Fig.8.17. The measured results presented in Figs 8.16 and 8.17 clearly demonstrate that, when high carrier to intermodulation ratios are required, the linearized amplifier can be operated at much higher output power levels than the main amplifier alone.
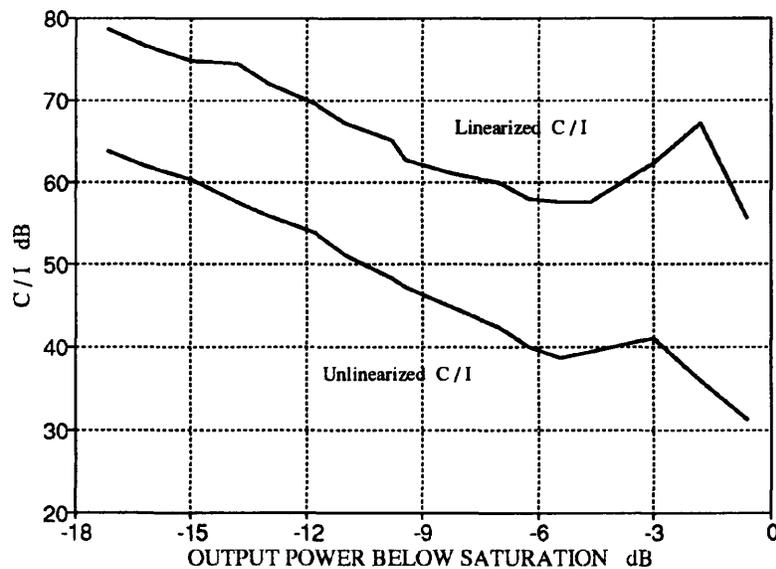
Fig.8.16 Carrier to intermodulation ratio with and without linearization

The results shown in Fig.8.16 were obtained for the linearizer being optimized for operation 0.6 dB below saturation level. The lower value for the C/I ratio for this case is 55 dB. To obtain the same level of linearity without linearization, it would be

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necessary to back-off the main amplifier by 12 dB from saturation.

The RF to DC efficiency of the main amplifier for operation at saturation level is 17%. As discussed previously in section 1.5.2 the efficiency of class A microwave amplifiers is generally low due to active devices limitations. The auxiliary amplifier was designed for output power rating 3 dB lower than the main amplifier. However, 10 dB higher gain was required for this amplifier resulting in a 4 stages configuration. Consequently, the DC power consumption of the auxiliary amplifier is 83% of the DC power required for the main amplifier.

For a C/I of at least 55 dB the linearized amplifier can be operated up to 0.6 dB below saturation level. This corresponds in 6% system efficiency. In comparison, the main amplifier has to be backed off from saturation 12 dB, resulting in an efficiency of only 1%.
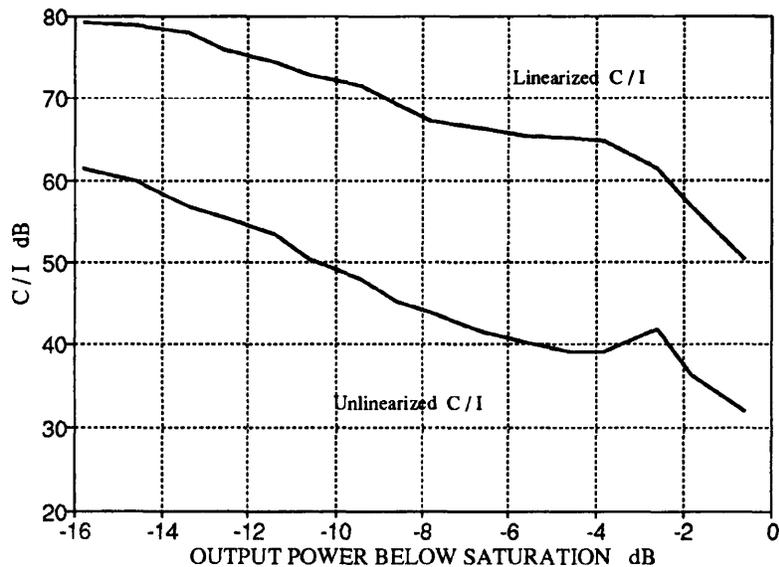
Fig.8.17 Carrier to intermodulation ratio with and without linearization

For higher C/I the unlinearized amplifier has to operate at even lower output power levels, resulting in a dramatic reduction of the system efficiency. For a required 65 dB C/I ratio, which is often the case in modern communication systems, the unlinearized amplifier has to operate 17 dB below saturation level, while the linearized amplifier has to be backed off only 3.8 dB from saturation level, as seen in Fig.8.17. Thus, for an 83% increase of the DC power consumption an increase of 13.2 dB in the output power is achieved with the feedforward linearizer circuit.

The excellent performance of the feedforward linearizer cannot be matched with that of a balance amplifier either. Power combining of two amplifiers results in only 6 dB improvement of the C/I for 100% increase in the DC power consumption of the unlinearized amplifier.

CHAPTER 9

Conclusions

9.1 Summary

The work presented in this thesis describes a research program undertaken to investigate the feedforward linearization technique, to develop design techniques and to overcome the special problems arising in the implementation of the method to the microwave frequency range.

An initial assessment of the feedforward technique was attempted through the simulation of the proposed design of the 6 GHz feedforward linearizer. Fundamental design criteria were established and a novel systematic method of optimizing feedforward systems was developed[93]. The performance evaluation of this linearizer clearly demonstrated the potential advantages of microwave feedforward linearizers in applications where high linearity is essential[106].

The encouraging results of this design initiated further analytical and CAD study of the feedforward linearization technique. The theoretical analysis of the technique resulted in the identification of the significant performance parameters and in the quantification of their relevant importance for the overall system performance. Design equations and graphs were produced to permit the calculation of feedforward linearizer distortion suppression for specific circuit parameters.

The CAD analysis of specific designs of interest verified the theoretical predictions and evaluated the viability of high efficiency configurations[100]. Furthermore, the CAD

analysis allowed the comparison of feedforward linearization with conventional power combining techniques[99].

Based on the results of the above study, an experimental linearizer was designed, constructed and evaluated for operation at the commercial satellite band 5.9-6.4 GHz. Before the final design and assembly of the feedforward system an investigation has been carried out on the evaluation and development of amplitude and phase control circuits suitable for use in the feedforward system. Schiffman and quadrature phase shifters were assessed.

The linearizer was designed employing linear CAD techniques which required the development of a new method to allow a linear approach to the optimization of feedforward linearizers[94]. This method, also, permits the use of commertialy available amplifier modules and active devices characterized by small signal measurements. The technique was, also, applied during the set-up procedure of the practical linearizer to allow the adjustment of the circuit for various operating conditions.

The experimental linearizer performance was evaluated for two and three tone tests and for various operating conditions. The linearizer achieved a 20 dB improvement of the intermodulation products which is, to the best of the author's knowledge, the most promising result so far reported for microwave feedforward amplifiers.

9.2 Conclusions

9.2.1 Effect of Phase and Amplitude Imbalance on the Linearizer Performance

The operation of the feedforward linearizer is based on the subtraction of two vectors at the output of each feedforward loop. As a result, amplitude and phase imbalance leads

to the deterioration of the system performance. Theoretical analysis of the effect of imbalance upon the performance of the linearizer showed that the effective cancellation of the overall system is dependant on the cancellation achieved in each feedforward loop. However, not the same level of imbalance is required in both loops in order to achieve a specific performance. The linearizer is much more sensitive to imbalances in the first loop than imbalances in the second loop. This arises from the third order intermodulation products properties. The important parameters in this effect are the auxiliary amplifier power rating and the coupling ratio of the output coupler. Thus, the effect of these two parameters was further investigated and the theoretical predictions were verified by the CAD analysis of some feedforward linearizer configurations. The CAD results indicate that the auxiliary amplifier power rating has a dramatic effect on the performance of the system.

9.2.2 Auxiliary Amplifier Power Rating

The auxiliary amplifier power rating is of particular importance for the overall performance of a feedforward linearized amplifier because it determines the efficiency of the system, affecting, at the same time, the distortion correcting capability of the linearizer. The design graphs presented in this thesis enable to quantify this effect and permit selection of the appropriate amplifier depending on the desired performance.

The performance of the feedforward linearizer employing auxiliary amplifiers with various power ratings has been investigated using CAD techniques. Alternative solutions to the classic feedforward configurations which employ two equal power rating amplifiers, were investigated in order to improve the system efficiency. The viability of these high efficiency configurations has been evaluated by inserting extra phase and amplitude imbalance in the feedforward loops to simulate changes in the operating conditions such as temperature, output power or aging of the components used.The results indicate that lower power auxiliary amplifier configurations can be a practical solution provided that the imbalances in the first feedforward loop remain below the limits discussed in chapter 4 of this thesis.

One important result from the CAD study of high efficiency linearizer configurations is that, if the power rating of the auxiliary amplifier is too low or/and the imbalances in the first loop too high, feedforward linearization could deteriorate rather than improve the performance of the power amplifier. This could be the case if the auxiliary amplifier saturates before the main amplifier does. To avoid this and ensure safe operation of the circuit the relevant equations of section 4.4 must always be satisfied. The restriction imposed by these equations is more severe if the linearizer is indented to operate near saturation.

9.2.3 Output Coupler Specification

The other important parameter for the correct and efficient operation of the feedforward linearizer is the coupling ratio of the output coupler. Low coupling ratios for this coupler require higher gain and higher output power auxiliary amplifiers requiring more gain stages configurations resulting in larger delays. To compensate this it would be necessary to use longer and, therefore, more lossy delay elements in the second loop and thereby reduce the system efficiency. Furthermore, low coupling ratios deteriorate the effective cancellation of the overall circuit. However, high coupling ratios increase the loss through this coupler and, hence, reduce the output power delivered by the feedforward linearizer. The importance of the output coupling ratio for the overall system efficiency has been investigated based on the analysis reported in [25]. A more realistic approach for the case of class A amplifiers has been developed in this thesis. The results, though indicative and not precise, give an insight into the problem and should be consulted in the design of a feedforward linearizer,

9.2.4 Optimization Techniques

The systematic technique developed to optimize feedforward linearizers was proved to be an effective way of designing the final linearizer circuit. The method allows the optimization of the system performance across the frequency band of interest. This is achieved by properly adjusting the gain and phase response of certain components to permit each path of the feedforward loops to tailor the response of the other. This way,

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phase and amplitude ripple of the various components may be compensated by the other path and lead to the optimum phase and amplitude balance. A further advantage of the method is that it can be modified to optimize the linearizer using linear CAD techniques. This allows the use of any transistor in the design of the linearizer circuit irrespective of the availability of nonlinear data for the device. It, also, allows the use of commercial amplifiers in feedforward linearizers built in a modular form. Furthermore, the method can be applied to the practical circuit and allow the optimum set-up for the desired operating conditions. The particular significance of this method in the development of an adaptive linearizer system will be further discussed in the next section where recommendations for further work are included.

9.2.5 Amplitude and Phase Control Circuits for Feedforward Linearizers

The sensitivity of the feedforward linearizer to phase and amplitude imbalance forces the use of amplitude and phase control circuits. Vector modulators employing the quadrature phase shifter principle of operation have been assessed for use in the feedforward linearizer. The use of both PIN diodes and GaAs single gate FETs as the active devices controlling the phase was investigated. The high insertion loss and considerable nonlinearity of the PIN diode phase shifter proved to be significant disadvantages for use in a feedforward linearizer.

The GaAs FET quadrature phase shifter, however, appears to be the ideal amplitude and phase control circuit for feedforward systems. The nonlinearity of this element is determined by the nonlinearity of the amplifiers employed and its inherent gain allows its use at the input of the system amplifiers with a similar degree of nonlinearity. A further advantage of this phase shifter is that it could be integrated in the main and the auxiliary amplifier circuits as one of the first stages.

The performance of a microstrip 90° Schiffman phase shifter was, also, practically evaluated. The results indicate that the particular structure employed in the design could

lead to improved performance of this element. However, further work should be carried out to evaluate and quantify the effect of the extra capacitance inherent in the layout of the structure upon the performance of the phase shifter.

9.2.5 Feedforward Systems Performance Evaluation

The feedforward circuits developed and assessed in this thesis indicate that the feedforward linearization method can be successfully employed to suppress effectively the intermodulation distortion of microwave power amplifiers. The method was first assessed with the nonlinear simulation of a feedforward linearizer employing the AT8151 GaAs FET chip devices. An experimental linearizer employing the Fujitsu FLC family packaged devices was, also, designed and constructed. Both the simulated and the experimental linearizer were designed to operate over the commercial satellite band 5.9-6.4 GHz. The simulation and measured results showed that feedforward linearization can achieve 20 dB reduction in the intermodulation distortion of the power amplifier over the 500 MHz bandwidth of operation. Furthermore, it was shown that the distortion cancellation does not depend either on the frequency of the input signal or on the carrier separation. This is an important advantage over the predistortion techniques which often require a set-up adjustment for each particular carrier combination[66].

The advantages of the feedforward linearization technique are better appreciated for systems requiring high level of linearity. The computer aided design of the 6 GHz feedforward linearizer was compared with the conventional balanced combining techniques and it was shown that the linearizer was the most efficient configuration. Furthermore, basic calculations of the measured results for the experimental linearizer indicate that feedforward linearization is an efficient approach for obtaining highly linear performance.

9.3 Recommendations for Future Work

The analytical and CAD study of the feedforward linearization method indicated that the distortion suppression obtained with the feedforward correction method is dependant upon the phase and amplitude imbalance that can be achieved in the circuit. In practice, additional imbalance in either of the two loops may occur for a number of reasons including manufacturing tolerances, temperature drift and component aging. Quadrature phase shifters were employed in the experimental linearizer to compensate for component tolerances. Further measurements on the temperature and component aging effect would, also, be necessary to evaluate the required adjustable phase and amplitude range of a feedforward linearizer used in a practical system with strict specifications. In systems where temperature and time stability is essential, built-in test features to allow adjustment of the feedforward linearizer setting to compensate for aging or drift would be necessary.

One possible solution is suggested here, based on the linear design procedures developed in this thesis. In this design procedure the output of each loop is monitored for a minimum in the signal strength. The inclusion of switching elements in the circuit would enable the cancellation in each loop to be monitored with periodic test signals. The results of these tests could be used by an electronic control loop controlling phase shifters and attenuators in the appropriate loop of the linearizer. This would permit compensation for loop imbalance in situ.

Such a control system could be easily incorporated in the circuit to monitor the first loop balance, since access to both the loop input and output signals is readily available. The loop input should be the linearizer input with the loop output signal indicating the state of the loop balance available at the unused fourth port of the output coupler of the linearizer.

In the second loop two additional couplers would be required, one between the output of the main amplifier and the second coupler and the second at the linearizer output. The first coupler is required to inject the test signal, the second to monitor the state of the loop balance. The advantage of this approach is that the detector monitoring the loop balance may be relatively simple, since only a measure of the magnitude of the output test signal is required.

In satellite communication systems the small size and the efficiency of the components is fundamental. The use of an electronic control system for the compensation of amplitude and phase imbalance in the feedforward loops allows the use of low power rating auxiliary amplifiers improving, thus, the efficiency of a feedforward linearized amplifier. The size of the system, however, resulting from the need for three couplers and two amplifiers, may preclude its use in satellite systems. An obvious solution would be a MMIC implementation of the system.

MMIC realization of the feedforward system suffers from two main disadvantages, namely the size of the conventional couplers resulting in high cost and the limited power output capabilities of MMIC amplifiers currently available. If the whole linearizer is to be implemented in MMIc technology, it would be necessary to develop suitable novel techniques for MMIC integration of reduced size passive components. Another solution would be to employ MIC technology where the couplers are built in conventional microstrip whilst the amplifiers and the required phase and amplitude control circuits are implemented in MMIC form.

Amplifiers produced using the currently available MMIC process are limited to power outputs of the order of 1 W or less. This is not sufficient for satellite transponders where output powers of 10 W are required. Nevertheless, reported results on experimental HEMT and HBT transistors[17,22]indicate that higher power devices should be expected to become available in the very near future.

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APPENDIX 1

Manufacturers' Data Sheets for Active Devices

Avantek AT-8151 GaAs FET

Fujitsu C-Band Power GaAs FETs:

FLC 053WG

FLC 091WF

FLC 161WF

Avantek ATF-13136 GaAs FET

Hewlet Packard HPND-4050 PIN diode

Features

- **High Output Power:**
  29.0 dBm typical $P_{1 dB}$ at 4 GHz
- **High Gain at 1 dB Compression:**
  11.0 dB typical $G_{1 dB}$ at 4 GHz
- **High Power Efficiency:**
  38% typical at 4 GHz

Description

The ATF-45100 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 12 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 2.5 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device. All metal surfaces are gold plated for ease of bonding and die attach.

The recommended mounting procedure is to die attach temperature of 300°C using a gold-tin preform under forming gas. Assembly should be performed with wedge bonding using either 0.7 mil of 1.0 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Avantek Chip Outline

POWER OUTPUT @ 1 dB GAIN COMPRESSION and 1 dB COMPRESSED GAIN vs. FREQUENCY
$V_{DS} = 9$ V, $I_{DS} = 250$ mA
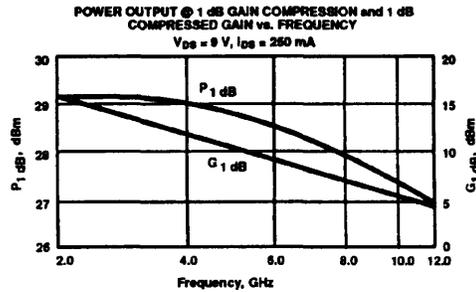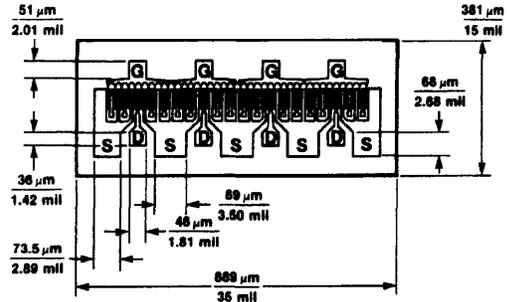
Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$P_{1 dB}$	Output Power @ 1 dB Gain Compression: $V_{DS} = 9$ V, $I_{DS} = 250$ mA	f = 4.0 GHz f = 8.0 GHz f = 12.0 GHz	dBm	28.0	29.0 28.0 27.0	
$G_{1 dB}$	1 dB Compressed Gain: $V_{DS} = 9$ V, $I_{DS} = 250$ mA	f = 4.0 GHz f = 8.0 GHz f = 12.0 GHz	dB	10.0	11.0 6.5 4.5	
η_{add}	Efficiency @ $P_{1 dB}$: $V_{DS} = 9$ V, $I_{DS} = 250$ mA	f = 4.0 GHz	%		38	
g_m	Transconductance: $V_{DS} = 2.5$ V, $I_{DS} = 250$ mA		mmho		200	
I_{DSS}	Saturated Drain Current: $V_{DS} = 1.75$ V, $V_{GS} = 0$ V		mA	400	600	800
V_p	Pinchoff Voltage: $V_{DS} = 2.5$ V, $I_{DS} = 5$ mA		V	–5.4	–4.0	–2.0

Note: 1. RF Performance is determined by packaging and testing 10 samples per wafer.

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Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	-7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	4.0 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	-65°C to +175°C

Thermal Resistance: $\theta_{jc} = 38°C/W$; $T_{CH} = 150°C$ Liquid Crystal Measurement; 1 μm Spot Size[4]	

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 26 mW/°C for $T_{MOUNTING SURFACE} > 23°C$.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Tray
ATF-45100-GP1	5
ATF-45100-GP3	50
ATF-45100-GP6	up to 300

Typical Performance, $T_A = 25°C$
(unless otherwise noted)

OUTPUT POWER AND POWER ADDED EFFICIENCY
vs. INPUT POWER
$V_{DS} = 9 V$, $I_{DS} = 250 mA$, f = 4.0 GHz

INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN
AND MAXIMUM STABLE GAIN vs. FREQUENCY
$V_{DS} = 9 V$, $I_{DS} = 250 mA$
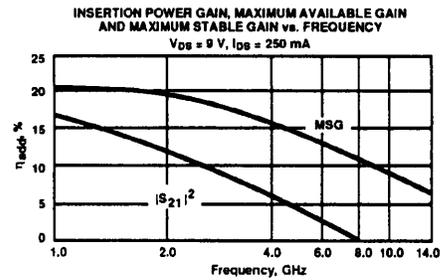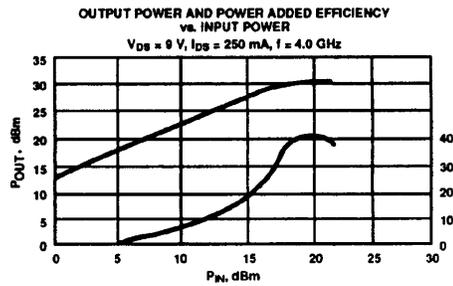
Typical Scattering Parameters: Common Source, $Z_O = 50 \Omega$ $T_A = 25°C$, $V_{DS} = 9 V$, $I_{DS} = 250 mA$

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
1.0	.92	-88	16.1	6.41	124	-27.3	.043	36	.32	-45
2.0	.85	-127	12.1	4.01	96	-26.0	.050	38	.29	-68
3.0	.84	-147	9.3	2.93	78	-25.4	.054	40	.29	-87
4.0	.85	-159	6.8	2.19	64	-24.9	.057	43	.31	-102
5.0	.87	-169	4.8	1.74	51	-24.3	.061	48	.37	-118
6.0	.88	-177	3.1	1.43	38	-23.9	.064	53	.43	-130
7.0	.88	177	1.3	1.17	27	-23.5	.067	57	.50	-139
8.0	.89	173	0.0	1.00	19	-22.4	.076	60	.57	-149
9.0	.90	167	-1.3	.86	8	-21.7	.082	63	.63	-157
10.0	.90	162	-2.6	.74	1	-21.2	.087	60	.68	-162
11.0	.91	157	-4.0	.63	-9	-20.4	.096	57	.72	-169
12.0	.91	148	-5.4	.54	-18	-19.9	.101	54	.75	-171
13.0	.90	145	-6.0	.50	-25	-19.6	.105	48	.79	-175
14.0	.90	135	-6.9	.45	-35	-19.7	.104	41	.82	-179

A model for this device is available in the DEVICE MODELS section

FUJITSU C-BAND POWER GaAs FETs

FLC SERIES

C-BAND POWER GaAs FETs

FEATURES

- High Efficiency
- High Power Output
- High Gain
- High Linearity
- Hermetic Metal/Ceramic Package
- Proven Reliability
- Space Qualified Parts Abailable

SELECTION TABLE

Part No.	P_{1dB} (typ.)	G_{1dB} (typ.)	Freq.
FLC053WG	27 dBm	9 dB	8 GHz
FLC091WF	28.8dBm	8.5dB	6 GHz
FLC103WG	30 dBm	8 dB	8 GHz
FLC161WF	31.8dBm	7.5dB	6 GHz
FLC253MH-6*	34.0dBm	9 dB	6.4GHz
FLC253MH-8*	34 dBm	8 dB	8 GHz
FLC311MG-4*	34.8dBm	9.5dB	4.2GHz

*Internally matched input

The FLC series are N-channel GaAs FETs with a Schottky-barrier gate structure designed for high efficiency high reliability applications in C-band. These transistors are assembled in hermetic metal/ceramic package. The FLC311MG-4 and FLC253MH-6, 8 have an internally matched input. Fujitsu's stringent Quality Assurance assures high performance and reliability by 100% testing of important parameters such as drain/source breakdown voltage and thermal resistance (Rth).

Case Style WG	Case Style WF	Case Style MH	Case Style MG

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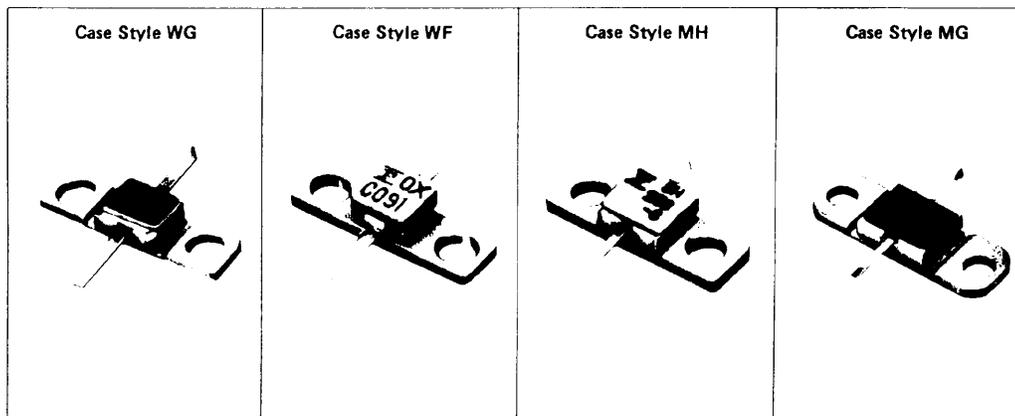
FUJITSU **FLC 053WG**

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta = 25°C)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_T	$T_C = 25°C$	3.75	W
Storage Temperature	T_{stg}		-65 ~ +175	°C
Channel Temperature	T_{ch}		+175	°C

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta = 25°C)

Item	Symbol	Test Conditions	Limit Min.	Limit Typ.	Limit Max.	Unit
Drain Current	I_{DSS}	$V_{DS} = 5V$, $V_{GS} = 0V$	–	200	300	mA
Transconductance	g_m	$V_{DS} = 5V$, $I_{DS} = 125mA$	–	100	–	mS
Pinch-off Voltage	V_P	$V_{DS} = 5V$, $I_{DS} = 10mA$	-1	-2	-3.5	V
Gate-Source Breakdown Voltage	V_{GSO}	$I_{GS} = -10\mu A$	-5	–	–	V
Output Power at 1dB G.C.P.	P_{1dB}	$V_{DS} = 10V$ $I_{DS} \cong 0.6 I_{DSS}$ $f = 8GHz$	25.5	27	–	dBm
Power Gain at 1dB G.C.P.	G_{1dB}		8	9	–	dB
Power-added Efficiency	η_{add}		–	38	–	%
Thermal Resistance	R_{th}	Channel to Case	–	27	40	°C/W

G.C.P.: Gain Compression Point

POWER DERATING CURVE

DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE

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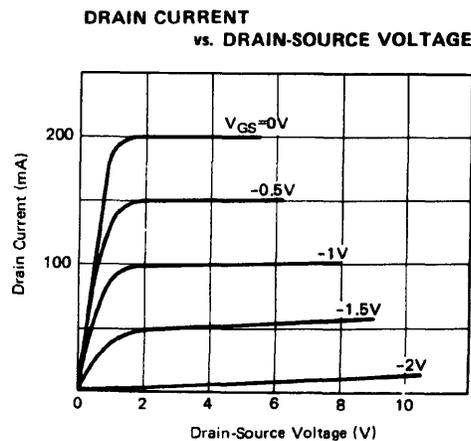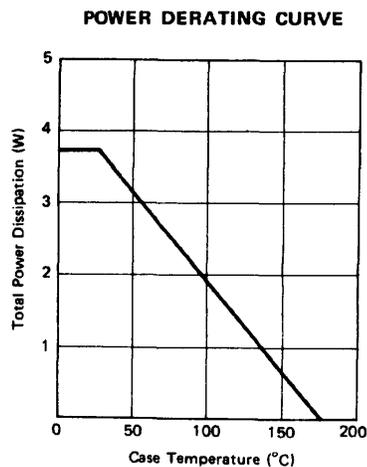
OUTPUT POWER vs. INPUT POWER
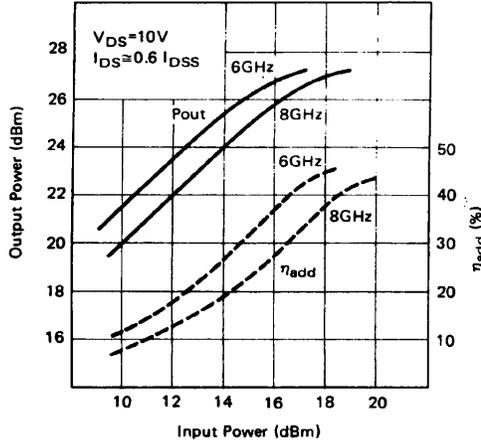
P_{1dB} & η_{add} vs. V_{DS}
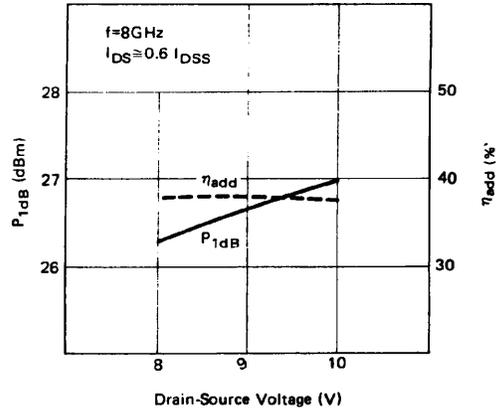
S-PARAMETERS
$V_{DS} = 10V$, $I_{DS} = 125mA$

| FREQUENCY | S_{11} | | S_{21} | | S_{12} | | S_{22} | |
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
500	.958	−40.5	5.659	152.0	.016	62.4	.437	−22.4
1000	.939	−73.5	4.938	128.9	.027	44.8	.428	−40.5
2000	.910	−118.1	3.544	93.9	.037	19.9	.429	−68.6
3000	.892	−144.5	2.619	69.2	.038	3.8	.462	−90.0
4000	.878	−163.3	2.034	47.9	.037	−6.4	.509	−108.7
5000	.863	−177.2	1.646	30.0	.034	−12.0	.555	−124.7
6000	.856	171.7	1.392	14.2	.032	−14.8	.601	−138.3
7000	.847	163.0	1.228	.3	.031	−15.8	.643	−149.1
8000	.841	154.6	1.140	−13.6	.030	−11.0	.693	−157.8
9000	.810	145.1	1.083	−28.7	.034	−9.4	.733	−167.2
10000	.756	135.1	1.068	−43.9	.039	−15.3	.753	−175.7
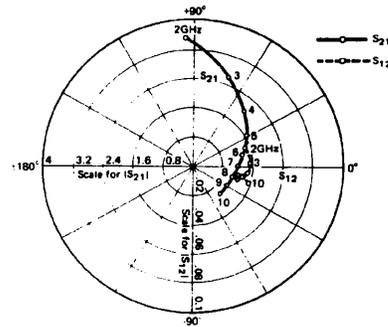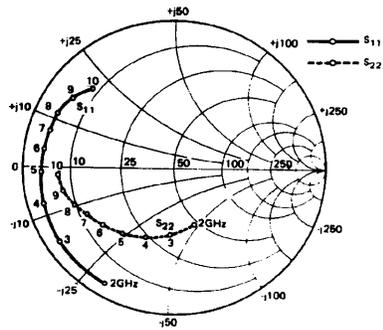
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FUJITSU FLC 091WF

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta = 25°C)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		–5	V
Total Power Dissipation	P_T	$T_C = 25°C$	4.16	W
Storage Temperature	T_{stg}		–65 ~ +175	°C
Channel Temperature	T_{ch}		+175	°C

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta = 25°C)

Item	Symbol	Test Conditions	Limit Min.	Limit Typ.	Limit Max.	Unit
Drain Current	I_{DSS}	$V_{DS} = 5V$, $V_{GS} = 0V$	–	300	450	mA
Transconductance	g_m	$V_{DS} = 5V$, $I_{DS} = 200mA$	–	150	–	mS
Pinch-off Voltage	V_P	$V_{DS} = 5V$, $I_{DS} = 15mA$	–1	–2	–3.5	V
Gate-Source Breakdown Voltage	V_{GSO}	$I_{GS} = -15\mu A$	–5	–	–	V
Output Power at 1dB G.C.P.	P_{1dB}	$V_{DS} = 10V$ $I_{DS} \approx 0.6 I_{DSS}$ $f = 6GHz$	27.5	28.8	–	dBm
Power Gain at 1dB G.C.P.	G_{1dB}		7.5	8.5	–	dB
Power-added Efficiency	η_{add}		–	35	–	%
Thermal Resistance	R_{th}	Channel to Case	–	25	36	°C/W

G.C.P.: Gain Compression Point

POWER DERATING CURVE

DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE

OUTPUT POWER & IM₃ vs. INPUT POWER

S.C.L.: Single Carrier Level
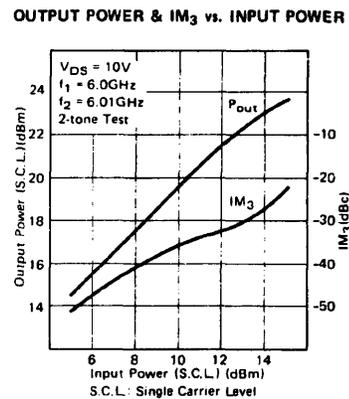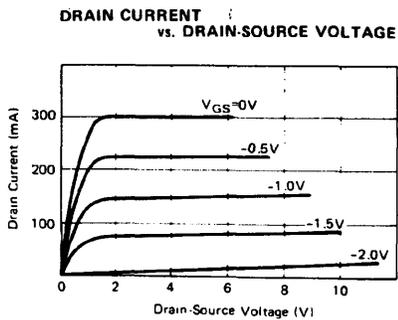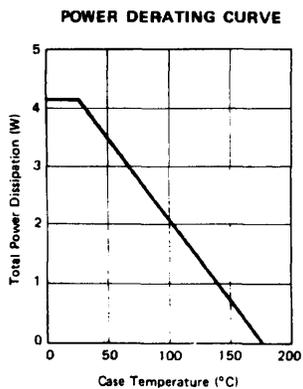
OUTPUT POWER vs. INPUT POWER
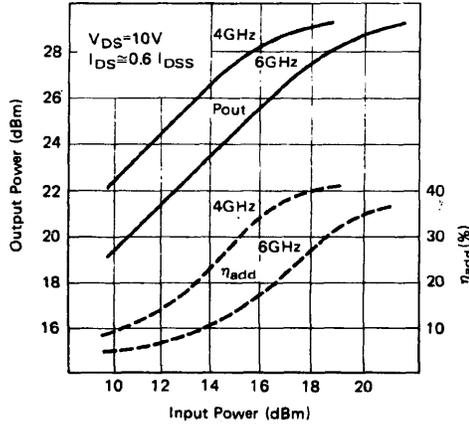
P_{1dB} & η_{add} vs. V_{DS}
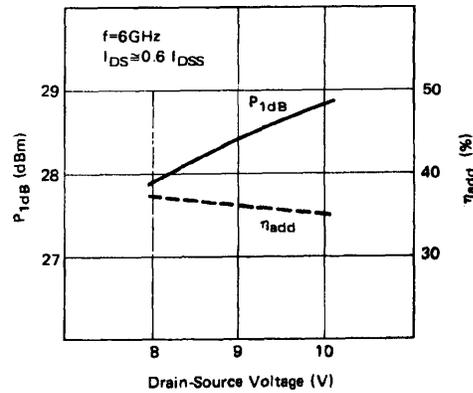
S-PARAMETERS

V_{DS} = 10V, I_{DS} = 180mA

FREQUENCY (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
500	.917	-58.1	8.230	142.7	.029	53.9	.342	-37.2
2000	.858	-148.7	4.080	78.2	.055	7.8	.264	-99.6
3000	.846	-175.8	2.860	52.8	.056	-6.6	.280	-123.5
4000	.840	164.0	2.163	30.5	.053	-16.3	.317	-144.6
5000	.841	148.2	1.730	10.8	.050	-23.7	.367	-162.7
6000	.850	134.3	1.440	-7.7	.048	-27.7	.425	-178.7
7000	.853	122.0	1.237	-24.9	.048	-31.6	.479	167.8
8000	.855	109.7	1.094	-42.3	.049	-34.2	.531	155.1
9000	.845	96.4	.972	-59.8	.053	-40.0	.570	141.9
10000	.839	82.5	.883	-76.8	.058	-46.1	.593	128.2
11000	.843	68.4	.823	-93.6	.065	-53.9	.621	114.9
12000	.849	52.5	.789	-111.8	.075	-63.2	.645	101.3

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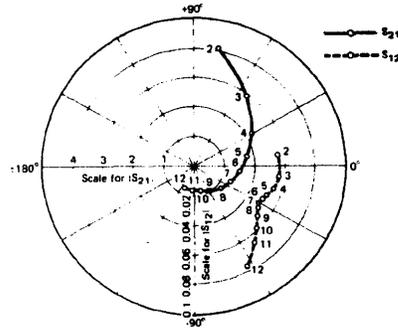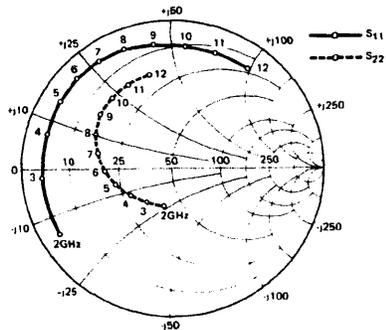
FUJITSU FLC 161WF

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta = 25°C)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		–5	V
Total Power Dissipation	P_T	$T_C = 25°C$	7.5	W
Storage Temperature	T_{stg}		–65 ~ +175	°C
Channel Temperature	T_{ch}		+175	°C

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta = 25°C)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain Current	I_{DSS}	$V_{DS} = 5V$, $V_{GS} = 0V$	–	600	900	mA
Transconductance	g_m	$V_{DS} = 5V$, $I_{DS} = 400mA$	–	300	–	mS
Pinch-off Voltage	V_P	$V_{DS} = 5V$, $I_{DS} = 30mA$	–1	–2	–3.5	V
Gate-Source Breakdown Voltage	V_{GSO}	$I_{GS} = -30\mu A$	–5	–	–	V
Output Power at 1dB G.C.P.	P_{1dB}	$V_{DS} = 10V$ $I_{DS} \approx 0.6\ I_{DSS}$ $f = 6GHz$	30.5	31.8	–	dBm
Power Gain at 1dB G.C.P.	G_{1dB}		6.5	7.5	–	dB
Power-added Efficiency	η_{add}		–	35	–	%
Thermal Resistance	R_{th}	Channel to Case	–	15	20	°C/W

G.C.P.: Gain Compression Point

POWER DERATING CURVE

DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE

OUTPUT POWER & IM₃ vs. INPUT POWER
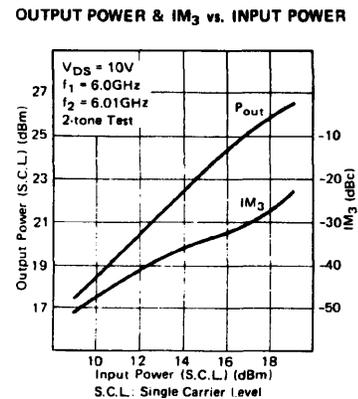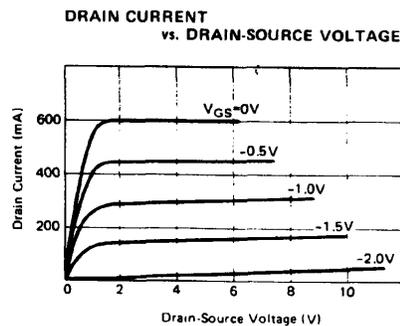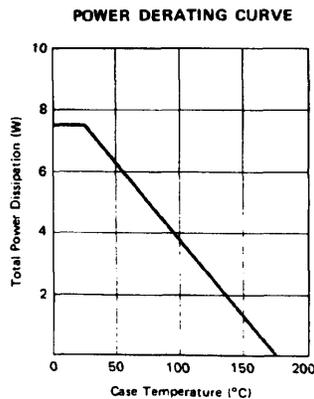
OUTPUT POWER vs. INPUT POWER
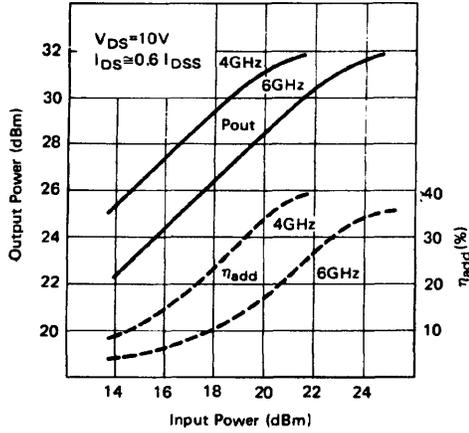
P_{1dB} & η_{add} vs. V_{DS}
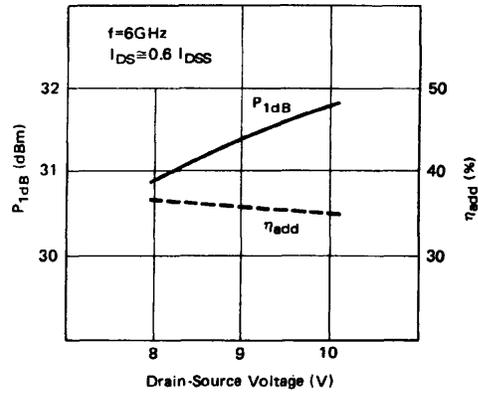
S-PARAMETERS

V_{DS} = 10V, I_{DS} = 360mA

FREQUENCY (MHz)	S_{11} MAG	S_{11} ANG	S_{21} MAG	S_{21} ANG	S_{12} MAG	S_{12} ANG	S_{22} MAG	S_{22} ANG
500	.852	-94.3	9.235	125.6	.033	37.0	.222	-116.9
2000	.859	-173.6	3.086	65.5	.043	1.7	.343	-159.2
3000	.861	167.9	2.045	43.9	.041	-5.1	.399	-167.3
4000	.863	153.5	1.489	24.3	.039	-7.7	.459	-176.2
5000	.873	141.8	1.154	7.2	.038	-6.7	.518	174.9
6000	.887	131.5	.936	-8.7	.039	-4.8	.575	166.1
7000	.894	122.4	.783	-23.0	.041	-3.6	.626	158.0
8000	.900	113.5	.676	-37.3	.046	-2.4	.671	149.4
9000	.895	104.1	.586	-51.3	.052	-6.3	.700	139.8
10000	.891	94.6	.521	-64.5	.059	-11.1	.716	129.8
11000	.898	85.4	.476	-76.5	.067	-17.0	.736	120.0
12000	.909	75.6	.449	-89.5	.079	-24.3	.761	109.8

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AVANTEK

ATF-13136
2-16 GHz Low Noise
Gallium Arsenide FET
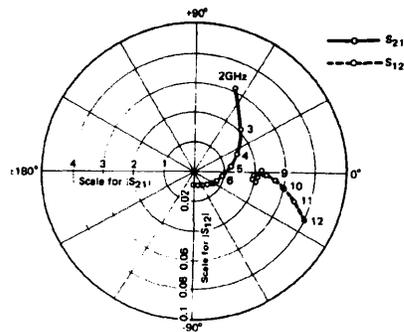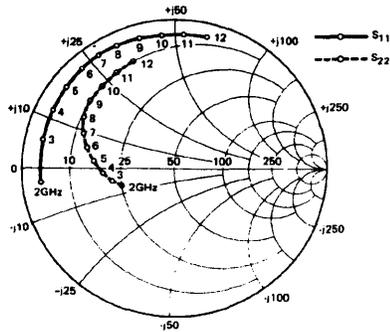
Features

- **Low Noise Figure: 1.2 dB typical at 12 GHz**
- **High Associated Gain: 9.5 dB typical at 12 GHz**
- **High Output Power: 17.5 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

Description

Avantek's ATF-13136 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

Avantek 36 micro-X Package[1]

Notes:
(unless otherwise specified)
1. Dimensions are $\frac{in}{mm}$
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13
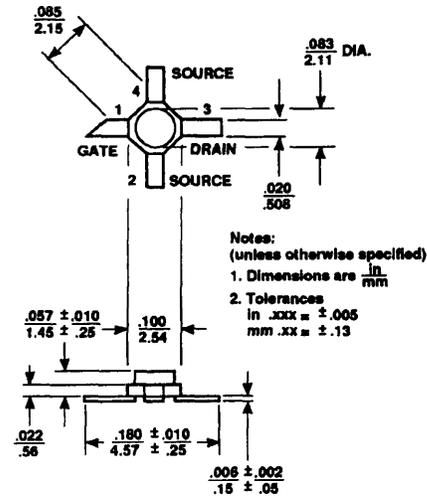
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
$V_{DS} = 2.5\ V$, $I_{DS} = 20\ mA$, $T_A = 25°C$
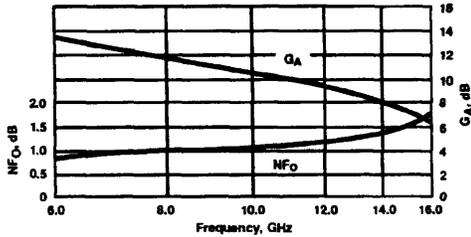
Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NF$_O$ dB	Gamma Opt Mag	Gamma Opt Ang	R$_N$/50
4.0	0.5	.58	87	.22
6.0	0.8	.47	130	.18
8.0	1.0	.37	−163	.17
12.0	1.2	.47	−65	.80
14.0	1.4	.52	−15	1.20

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF$_O$	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB		1.0 1.2 1.4	1.4
G$_A$	Gain @ NF$_O$: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB	8.5	11.5 9.5 8.0	
P$_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
G$_{1\,dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
gm	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
I$_{DSS}$	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	20	50	100
Vp	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	−4.0	−1.5	−0.5

Notes: 1. Long leaded 35 package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

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ATF-13136, 2-16 GHz
Low Noise Gallium Arsenide FET

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	-4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	-65°C to +175°C

Thermal Resistance: θ_{jc} = 400°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm Spot Size[5]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.5 mW/°C for T_{CASE} > 85°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-13136-TR1	1000	7"
ATF-13136-TR2	4000	13"
ATF-13136-STR	1	STRIP

Typical Performance, T_A = 25°C

(unless otherwise noted)

OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. I_{DS}
V_{DS} = 2.5 V, f = 12.0 GHz

INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 2.5 V, I_{DS} = 20 mA
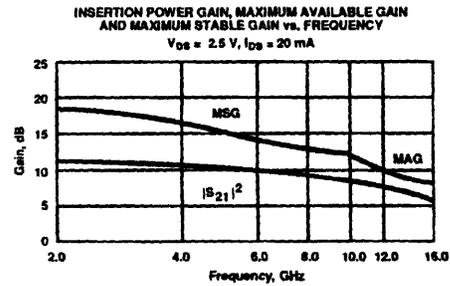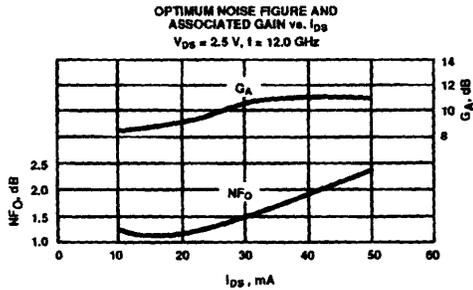
Typical Scattering Parameters: Common Source, Z_0 = 50 Ω T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
2.0	.95	-42	11.2	3.65	134	-26.7	.046	62	.56	-37
3.0	.87	-65	10.7	3.43	112	-24.2	.062	40	.53	-47
4.0	.84	-85	10.3	3.28	93	-22.3	.077	31	.53	-54
5.0	.78	-104	10.1	3.21	73	-20.3	.097	18	.48	-62
6.0	.69	-128	10.4	3.30	52	-18.6	.117	7	.43	-76
7.0	.59	-163	10.4	3.32	27	-17.3	.137	-12	.35	-95
8.0	.54	157	9.8	3.10	2	-17.0	.142	-27	.26	-110
9.0	.55	121	9.2	2.89	-19	-16.3	.153	-43	.15	-119
10.0	.54	93	8.7	2.71	-41	-16.0	.159	-58	.07	-142
11.0	.56	64	8.1	2.54	-61	-16.2	.155	-73	.06	92
12.0	.61	37	7.4	2.34	-84	-16.8	.144	-89	.15	46
13.0	.65	19	6.8	2.18	-102	-17.6	.132	-100	.18	23
14.0	.65	7	6.4	2.09	-120	-18.0	.126	-114	.19	-2
15.0	.67	-6	5.9	1.98	-139	-18.2	.123	-119	.16	-27
16.0	.68	-25	5.3	1.84	-170	-18.4	.120	-134	.13	-30

A model for this device is available in the DEVICE MODELS section.

Features

LOW SERIES RESISTANCE
1.3 Ω Typical

LOW CAPACITANCE
0.07 pF Typical

FAST SWITCHING
2 ns Typical

RUGGED CONSTRUCTION
4 Grams Minimum Lead Pull

Description

The HPND-4001 and -4050 are beam lead PIN diodes designed specifically for low capacitance, low series resistance and rugged construction. The new HP mesa process allows the fabrication of beam lead PINs with a very low RC product. A nitride passivation layer provides immunity from contaminants which would otherwise lead to I_R drift. A polyimide layer provides scratch protection.

Maximum Ratings

Operating Temperature .... -65°C to +175°C
Storage Temperature .... -65°C to +200°C
Power Dissipation at T_{CASE} = 25°C .... 250 mW
Derate linearly to zero at 175°C
Minimum Lead Strength .... 4 grams pull on either lead

Outline 07
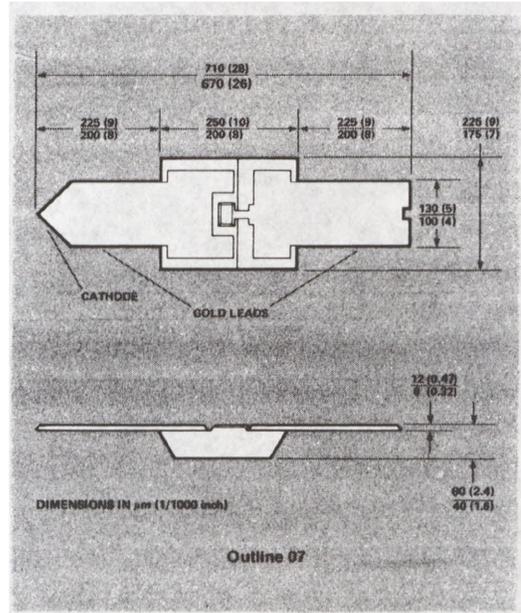
Applications

The HPND-4001 and -4050 beam lead PIN diodes are designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting and modulating at microwave frequencies. The low capacitance and low series resistance at low current make these devices ideal for applications in the shunt configuration.

Bonding and Handling Procedures

See page 6-24

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Electrical Specifications at $T_A = 25°C$

Part Number	Breakdown Voltage V_{BR} (V)		Series Resistance R_S (Ω)		Capacitance C_T (pF)		Minority Carrier Lifetime τ (ns)	Reverse Recovery Time t_{rr} (ns)
	Min.	Typ.	Typ.	Max.	Typ.	Max.	Typ.	Typ.
HPND-4001	50	80	1.8	2.2	0.07*	0.08*	30	3
HPND-4050	30	40	1.3	1.7	0.12	0.15	25	2
Test Conditions	$V_R = V_{BR}$ Measure $I_R \leq 10 \mu A$		$I_F = 10$ mA $f = 100$ MHz		$V_R = 10$ V *$V_R = 30$V $f = 1$ MHz		$I_F = 10$ mA $I_R = 6$ mA	$I_F = 10$ mA $V_R = 10$V

Typical Parameters
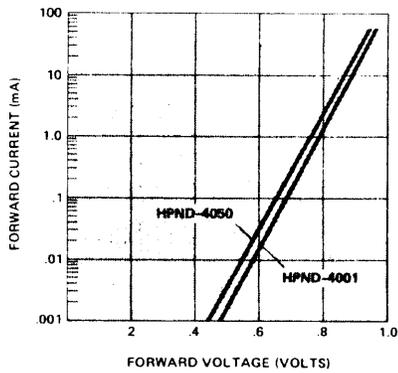
Figure 1 Typical Forward Characteristics.
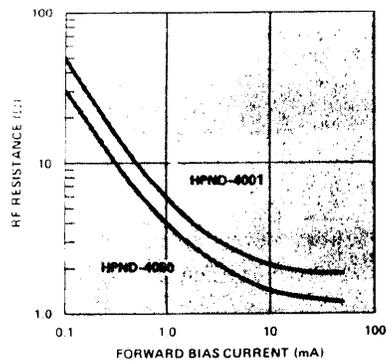
Figure 2 Typical RF Resistance vs. Forward Bias Current.
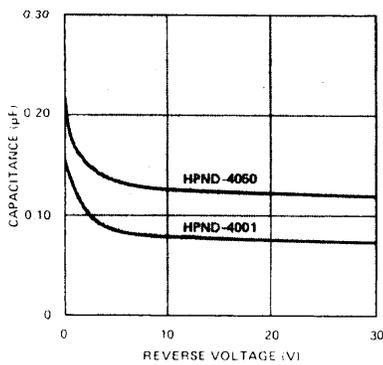
Figure 3 Typical Capacitance vs Reverse Voltage
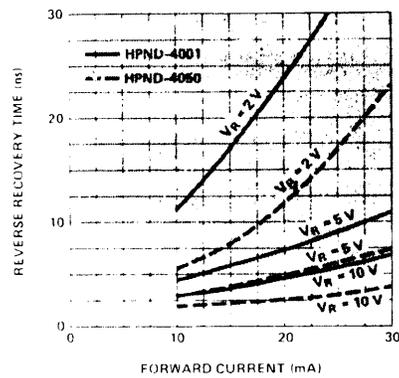
Figure 4 Typical Reverse Recovery Time vs Forward Current Shunt Configuration

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APPENDIX 2

Scattering Parameters Data Files Employed in the

Simulated Designs

AT8151A.s2p

Scattering parameters file for the Avantek AT8151 GaAs FET with Bias conditions:
V_{ds} = 9 V I_{ds} = 313 mA.

FREQ MHz	S11 Real	S11 Im	S21 Real	S21 Im	S12 Real	S12 Im	S22 Real	S22 Im
1000.00	-0.33884	-0.83197	-2.08235	4.27808	0.09519	0.05449	-0.10086	-0.34694
2000.00	-0.69111	-0.52864	-0.23833	2.65403	0.11909	0.02698	-0.23935	-0.27160
3000.00	-0.77790	-0.37627	0.20232	1.81084	0.12354	0001081	-0.28325	-0.25035
4000.00	-0.81156	-0.29360	0.35780	1.33403	0.12364	0.00003	-0.31122	-0.25254
5000.00	-0.82879	-0.24306	0.42229	1.02892	0.12211	-0.00799	-0.33630	-0.26367
6000.00	-0.83948	-0.20930	0.44876	0.81646	0.11974	-0.01431	-0.36148	-0.27772
7000.00	-0.84709	-0.18548	0.45649	0.65989	0.11688	-0.01940	-0.38733	-0.29190
8000.00	-0.85306	-0.16764	0.45400	0.53994	0.11374	-0.02354	-0.41371	-0.30481
9000.00	-0.85806	-0.15379	0.44561	0.44552	0.11045	-0.02689	-0.44029	-0.31582
10000.0	-0.86243	-0.14266	0.43381	0.36975	0.10710	-0.02958	-0.46666	-0.32466
11000.0	-0.86633	-0.13346	0.42009	0.30810	0.10378	-0.03170	-0.49250	-0.33133
12000.0	-0.86987	-0.12567	0.40542	0.25741	0.10053	-0.03335	-0.51751	-0.33595

AT8151B.s2p

Scattering parameters file for the Avantek AT8151 GaAs FET with Bias conditions:
V_{ds} = 4 V I_{ds} = 512 mA.

FREQ MHz	S11 Real	S11 Im	S21 Real	S21 Im	S12 Real	S12 Im	S22 Real	S22 Im
1000.00	-0.25502	-0.87794	-2.29071	4.19351	0.07447	0.04808	-0.08609	-0.29903
2000.00	-0.66460	-0.58661	-0.29960	2.72036	0.09769	0.02555	-0.21440	-0.55905
3000.00	-0.77158	-0.42007	0.20318	1.86692	0.10238	0.01124	-0.66089	-0.25335
4000.00	-0.81351	-0.32809	0.38104	1.36995	0.10269	0.00170	-0.29349	-0.26493

```
5000.00 -0.83484 -0.27098  0.55292  1.04798  0.10136 -0.00529 -0.32406 -0.28223
6000.00 -0.84782 -0.23248  0.48022  0.82270  0.09925 -0.01066 -0.35502 -0.30017
7000.00 -0.85683 -0.20487  0.48567  0.65668  0.09671 -0.01487 -0.38660 -0.31646
8000.00 -0.86366 -0.18408  0.47942  0.5299   0.09395 -0.01817 -0.41838 -0.33008
9000.00 -0.86920 -0.16780  0.46674  0.43091  0.09111 -0.02075 -0.44981 -0.34070
10000.0 -0.87366 -0.15463  0.45057  0.35213  0.08828 -0.02273 -0.48042 -0.34834
11100.0 -0.87790 -0.14370  0.43270  0.28871  0.08553 -0.02422 -0.50981 -0.35324
12000.0 -0.88145 -0.13442  0.41425  0.23718  0.08288 -0.02530 -0.53772 -0.35572
```

Isolator.s2p

Scattering parameters file for the simulation of a microstrip isolator.

FREQ GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.00001	0.10000	0.00000	0.94400	0.00000	0.10000	0.00000	0.10000	0.00000
1.10000	0.10000	0.00000	0.94400	0.00000	0.10000	0.00000	0.10000	0.00000
5.10000	0.10000	0.00000	0.94400	0.00000	0.10000	0.00000	0.10000	0.00000
6.10000	0.10000	0.00000	0.94440	0.00000	0.10000	0.00000	0.10000	0.00000
7.10000	0.10000	0.00000	0.94400	0.00000	0.10000	0.00000	0.10000	0.00000
20.1000	0.10000	0.00000	0.94400	0.00000	0.10000	0.00000	0.10000	0.00000

Bandfilt.s2p

Scattering parameters file for the simulation of a circuit having the same amplitude and phase response as the band pass filter described in section 3.4.3 within the 5.9-6.4 GHz band, but allowing signals at other frequencies to pass through.

FREQ GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang
5.00000	0.011	-168.413	0.995	-83.507
5.90000	0.011	-168.413	0.995	-83.507
6.00000	0.001	-149.584	0.995	-86.912
6.10000	0.005	-4.090	0.995	-90.277
6.20000	0.009	-4.046	0.995	-93.611
6.30000	0.011	-5.794	0.995	-96.920
6.40000	0.010	-7.325	0.995	-100.212
7.00000	0.010	-7.325	0.995	-100.212

APPENDIX 3

Measured and Modeled Scattering Parameters of the PIN diode HPND4510

The measured scattering parameters presented here were obtained with the measurements employing the TRL calibration technique as described in chapter 6. The modelled scattering parameters correspond to the optimized equivalent circuit for the PIN diode also described in chapter 6. Data for various bias conditions are provided. The optimized element values for the PIN diode are, also, included.

Forward Biased Current 2 mA

$R_2 = 7.63 \ \Omega$

FREQ GHz	Modeled S11 Mag	S11 Ang	S21 Mag	S21 Ang	Measured S11 Mag	S11 Ang	S21 Mag	S21 Ang
5.0	0.096	25.812	0.926	-44.900	0.151	28.100	0.916	-42.800
5.1	0.097	24.164	0.926	-45.800	0.161	27.760	0.914	-43.560
5.2	0.098	24.525	0.925	-46.701	0.170	27.420	0.913	-44.320
5.3	0.099	23.896	0.925	-47.602	0.180	27.080	0.911	-45.080
5.4	0.099	23.277	0.925	-48.503	0.189	26.740	0.910	-45.840
5.5	0.100	22.667	0.925	-49.404	0.199	26.400	0.908	-46.600
5.6	0.101	22.066	0.925	-50.306	0.192	25.220	0.909	-47.280
5.7	0.102	21.475	0.925	-51.207	0.185	24.040	0.910	-47.960
5.8	0.103	20.892	0.925	-52.109	0.178	22.860	0.910	-48.640
5.9	0.104	19.318	0.925	-53.010	0.171	21.680	0.911	-49.320
6.0	0.105	18.752	0.924	-53.912	0.164	20.500	0.912	-50.000
6.1	0.106	17.195	0.924	-54.814	0.167	20.600	0.910	-50.920
6.2	0.107	16.646	0.924	-55.716	0.170	20.700	0.908	-51.840
6.3	0.108	16.105	0.924	-56.619	0.174	20.800	0.906	-52.760
6.4	0.109	15.572	0.924	-57.521	0.177	20.900	0.904	-53.680
6.5	0.109	15.047	0.924	-58.424	0.180	21.000	0.902	-54.600

6.6	0.110	14.530	0.924	-59.326	0.188	17.900	0.902	-55.000
6.7	0.111	13.020	0.924	-60.229	0.196	14.800	0.901	-55.400
6.8	0.112	12.517	0.923	-61.132	0.203	11.700	0.901	-55.800
6.9	0.113	11.021	0.923	-62.035	0.211	8.600	0.900	-56.200
7.0	0.114	10.533	0.923	-62.939	0.219	5.500	0.900	-56.600

Forward Biased Current 1 mA

$R_2 = 7.91 \ \Omega$

	Modeled				Measured			
FREQ	S11	S11	S21	S21	S11	S11	S21	S21
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
5.0	0.098	24.819	0.923	-44.889	0.149	27.800	0.913	-42.500
5.1	0.098	25.173	0.923	-45.789	0.159	28.040	0.911	-43.300
5.2	0.099	25.537	0.923	-46.690	0.168	28.280	0.910	-44.100
5.3	0.100	24.910	0.923	-47.590	0.178	28.520	0.908	-44.900
5.4	0.101	24.222	0.923	-48.491	0.187	28.760	0.906	-45.700
5.5	0.102	23.683	0.923	-49.392	0.197	99.000	0.905	-46.500
5.6	0.103	23.083	0.923	-50.293	0.191	27.120	0.906	-47.200
5.7	0.104	22.491	0.922	-51.194	0.185	25.240	0.907	-47.900
5.8	0.105	21.909	0.922	-52.096	0.179	23.360	0.907	-48.600
5.9	0.105	21.334	0.922	-52.997	0.173	21.480	0.908	-49.300
6.0	0.106	20.768	0.922	-53.899	0.167	19.600	0.909	-50.000
6.1	0.107	20.210	0.922	-54.801	0.171	19.780	0.907	-50.900
6.2	0.108	19.660	0.922	-55.703	0.173	19.960	0.005	-51.800
6.3	0.109	19.118	0.922	--56.605	0.175	20.140	0.903	-52.700
6.4	0.110	18.584	0.922	-57.507	0.178	20.320	0.901	-53.600
6.5	0.111	17.057	0.921	-58.409	0.181	20.500	0.899	-54.500
6.6	0.112	16.537	0.921	-59.312	0.189	17.660	0.898	-54.880
6.7	0.113	16.025	0.921	-60.214	0.197	14.820	0.898	-55.260
6.8	0.114	15.520	0.921	-61.117	0.204	11.980	0.897	-55.640
6.9	0.115	12.022	0.921	-62.020	0.212	9.140	0.897	-56.020
7.0	0.116	10.531	0.921	-62.923	0.220	6.300	0.896	-56.400

Forward Biased Current 0.3 mA

$R_2 = 9.36 \ \Omega$

	Modeled				Measured		
FREQ GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S11 Mag	S11 Ang	S21 Mag	S21 Ang
5.0	0.107	24.429	0.911	-44.831	0.169	27.000	0.897	-41.633
5.1	0.108	23.803	0.911	-45.730	0.169	25.800	0.897	-42.420
5.2	0.108	22.185	0.911	-46.630	0.169	24.600	0.897	-43.207
5.3	0.109	21.575	0.911	-47.529	0.168	23.400	0.898	-43.993
5.4	0.110	20.971	0.911	-48.429	0.168	22.200	0.898	-44.780
5.5	0.111	20.376	0.910	-49.329	0.168	21.000	0.898	-45.567
5.6	0.111	19.787	0.910	-50.229	0.167	19.800	0.898	-46.353
5.7	0.112	18.205	0.910	-51.129	0.167	18.600	0.898	-47.140
5.8	0.113	17.631	0.910	-52.029	0.167	17.400	0.898	-47.927
5.9	0.114	16.063	0.910	-52.929	0.166	16.200	0.898	-48.713
6.0	0.115	15.503	0.910	-53.830	0.166	15.000	0.898	-49.500
6.1	0.115	14.949	0.910	-54.731	0.168	15.140	0.896	-50.380
6.2	0.116	14.402	0.910	-55.631	0.171	15.280	0.894	-51.260
6.3	0.117	13.861	0.909	-56.532	0.173	15.420	0.892	-52.140
6.4	0.118	12.327	0.909	-57.433	0.176	15.560	0.890	-53.020
6.5	0.119	11.800	0.909	-58.334	0.178	15.700	0.888	-53.900
6.6	0.120	11.278	0.909	-59.236	0.186	12.960	0.887	-54.380
6.7	0.120	10.744	0.909	-60.137	0.195	10.220	0.887	-54.860
6.8	0.121	9.255	0.909	-61.039	0.203	7.480	0.886	-55.340
6.9	0.122	8.752	0.909	-61.940	0.212	4.740	0.886	-55.820
7.0	0.123	7.256	0.908	-62.842	0.220	2.000	0.885	-56.300

Forward Biased Current 0.1 mA

$R_2 = 12.70 \ \Omega$

	Modeled				Measured		
FREQ GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S11 Mag	S11 Ang	S21 Mag	S21 Ang
5.0	0.229	10.125	0.884	-44.699	0.148	13.400	0.873	-40.880
5.1	0.129	9.565	0.884	-45.596	0.156	13.880	0.872	-41.580
5.2	0.130	9.008	0.884	-46.493	0.165	14.360	0.871	-42.360
5.3	0.130	8.456	0.884	-47.390	0.173	14.840	0.869	-43.140
5.4	0.131	7.909	0.884	-48.287	0.182	15.320	0.868	-43.920

5.5	0.132	6.366	0.884	-49.184	0.190	15.800	0.867	-44.700
5.6	0.132	5.827	0.883	-50.081	0.185	13.700	0.868	-45.500
5.7	0.133	5.293	0.883	-50.978	0.180	11.600	0.869	-46.300
5.8	0.134	4.763	0.883	-51.876	0.175	9.500	0.870	-47.100
5.9	0.134	3.237	0.883	-52.774	0.170	7.400	0.871	-47.900
6.0	0.135	2.716	0.883	-53.671	0.165	5.300	0.872	-48.700
6.1	0.136	1.199	0.883	-54.569	0.167	5.380	0.870	-49.540
6.2	0.136	0.686	0.883	-55.467	0.168	5.460	0.869	-50.380
6.3	0.137	-0.178	0.882	-56.366	0.170	5.540	0.867	-51.220
6.4	0.138	-0.674	0.882	-57.264	0.171	5.620	0.866	-52.060
6.5	0.138	-1.174	0.882	-58.162	0.173	5.700	0.864	-52.900
6.6	0.139	-2.679	0.882	-59.061	0.183	3.580	0.864	-53.280
6.7	0.140	-2.188	0.882	-59.960	0.193	1.460	0.863	-53.660
6.8	0.140	-3.701	0.882	-60.859	0.202	-0.660	0.863	-54.040
6.9	0.141	-4.218	0.882	-61.758	0.212	-2.780	0.862	-54.420
7.0	0.142	-5.739	0.882	-62.657	0.222	-4.900	0.862	-54.800

Forward Biased Current 0.03 mA

$R_2 = 18.80\ \Omega$

	Modeled				Measured			
FREQ	S11	S11	S21	S21	S11	S11	S21	S21
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
5.0	0.169	-15.379	0.838	-44.455	0.154	-13.600	0.830	-38.300
5.1	0.170	-14.925	0.838	-45.347	0.160	-11.820	0.829	-39.000
5.2	0.170	-14.474	0.838	-46.239	0.165	-10.040	0.828	-39.860
5.3	0.171	-14.024	0.838	-47.131	0.171	-8.260	0.828	-40.640
5.4	0.171	-13.576	0.838	-48.023	0.176	-6.480	0.827	-41.420
5.5	0.171	-12.131	0.838	-48.915	0.182	-4.700	0.826	-42.200
5.6	0.172	-10.687	0.838	-49.807	0.179	-6.420	0.828	-43.000
5.7	0.172	-11.245	0.838	-50.700	0.176	-8.140	0.829	-43.800
5.8	0.173	-12.805	0.837	-51.592	0.172	-9.860	0.831	-44.600
5.9	0.173	-13.367	0.837	-52.485	0.169	-11.580	0.832	-45.400
6.0	0.174	-14.932	0.837	-53.378	0.166	-13.300	0.834	-46.200
6.1	0.174	-15.498	0.837	-54.271	0.166	-13.040	0.832	-47.020
6.2	0.175	-16.066	0.837	-55.164	0.165	-12.780	0.830	-47.840
6.3	0.175	-16.636	0.837	-56.057	0.165	-12.520	0.829	-48.660
6.4	0.176	-17.209	0.837	-56.950	0.164	-12.260	0.827	-49.480
6.5	0.176	-18.783	0.837	-57.844	0.164	-12.000	0.825	-50.300
6.6	0.176	-19.359	0.836	-58.737	0.175	-13.040	0.825	-50.700
6.7	0.177	-20.938	0.836	-59.631	0.186	-14.080	0.825	-51.100

6.8	0.178	-21.519	0.836	-60.525	0.198	-15.120	0.825	-51.500
6.9	0.178	-22.101	0.836	-61.419	0.209	-16.160	0.825	-51.900
7.0	0.179	-22.686	0.836	-62.313	0.220	-17.200	0.825	-52.300

Forward Biased Current 0.01 mA

$R_2 = 26.76 \ \Omega$

	Modeled				Measured			
FREQ GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S11 Mag	S11 Ang	S21 Mag	S21 Ang
5.00000	0.219	-30.987	0.786	-44.136	0.182	-46.900	0.793	-32.000
5.1	0.219	-49.625	0.786	-35.021	0.181	-44.500	0.794	-32.880
5.2	0.219	-49.263	0.785	-35.907	0.180	-42.100	0.794	-33.760
5.3	0.220	-43.903	0.785	-36.792	0.180	-39.700	0.795	-34.640
5.4	0.220	-42.543	0.785	-37.678	0.179	-37.300	0.795	-35.520
5.5	0.220	-42.184	0.785	-38.563	0.178	-34.900	0.796	-36.400
5.6	0.220	-42.826	0.785	-39.449	0.177	-36.380	0.798	-37.200
5.7	0.221	-42.469	0.785	-40.335	0.176	-37.860	0.799	-38.000
5.8	0.221	-44.113	0.785	-41.221	0.174	-39.340	0.801	-38.800
5.9	0.221	-44.758	0.785	-42.107	0.173	-40.820	0.802	-39.600
6.0	0.222	-44.403	0.785	-42.994	0.172	-42.300	0.804	-40.400
6.1	0.222	-43.050	0.784	-43.880	0.182	-41.560	0.803	-41.320
6.2	0.222	-42.698	0.784	-44.767	0.192	-40.820	0.802	-42.240
6.3	0.223	-42.346	0.784	-45.653	0.203	-40.080	0.800	-43.160
6.4	0.223	-41.996	0.784	-46.540	0.213	-39.340	0.799	-44.080
6.5	0.223	-40.646	0.784	-47.427	0.223	-38.600	0.798	-45.000
6.6	0.224	-40.298	0.784	-48.314	0.220	-37.840	0.799	-45.600
6.7	0.224	-39.951	0.784	-49.201	0.216	-37.080	0.799	-46.200
6.8	0.224	-39.604	0.783	-50.089	0.213	-36.320	0.800	-46.800
6.9	0.225	-39.259	0.783	-50.976	0.209	-35.560	0.800	-47.400
7.0	0.225	-38.914	0.783	-51.864	0.206	-34.800	0.801	-48.000

Reverse Biased Voltage 0 V

$C_1 = 0.27$ pF

$R_1 = 14.11$ Ω

	Modeled			Measured			
FREQ GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S11 Mag	S11 Ang	S21 Mag	S21 Ang
5.0	0.772	-76.151	0.574	9.019	0.746	-74.800	0.607	14.200
5.1	0.765	-77.481	0.581	7.583	0.734	-76.020	0.617	13.140
5.2	0.759	-78.802	0.588	6.155	0.722	-77.240	0.627	12.080
5.3	0.752	-80.115	0.595	4.734	0.709	-78.460	0.636	11.020
5.4	0.745	-81.420	0.602	3.321	0.697	-79.680	0.646	9.960
5.5	0.739	-82.717	0.608	1.916	0.685	-80.900	0.656	8.900
5.6	0.735	-84.006	0.615	0.517	0.678	-82.420	0.664	7.200
5.7	0.725	-85.287	0.621	-0.874	0.671	-83.940	0.671	5.500
5.8	0.719	-86.561	0.628	-2.258	0.664	-85.460	0.679	3.800
5.9	0.712	-87.826	0.634	-3.635	0.657	-86.980	0.686	2.100
6.0	0.705	-89.084	0.640	-5.005	0.650	-88.500	0.694	0.400
6.1	0.699	-90.334	0.645	-6.368	0.642	-90.320	0.998	-0.800
6.2	0.692	-91.577	0.651	-7.724	0.635	-92.140	0.702	-2.000
6.3	0.686	-92.813	0.657	-9.074	0.627	-93.960	0.707	-3.200
6.4	0.679	-94.041	0.662	-10.417	0.620	-95.780	0.711	-4.400
6.5	0.673	-95.261	0.667	-11.753	0.612	-97.600	0.715	-5.600
6.6	0.667	-96.475	0.672	-13.083	0.598	-97.580	0.722	-6.980
6.7	0.660	-97.681	0.677	-14.407	0.583	-97.560	0.729	-8.360
6.8	0.654	-98.880	0.682	-15.725	0.569	-97.540	0.736	-9.740
6.9	0.648	-100.073	0.687	-17.036	0.554	-97.520	0.743	-11.120
7.0	0.641	-101.258	0.692	-18.341	0.540	-97.500	0.750	-12.500

Reverse Biased Voltage 1 V

$C_1 = 0.20$ pF

$R_1 = 12.7$ Ω

	Modeled			Measured			
FREQ GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S11 Mag	S11 Ang	S21 Mag	S21 Ang
5.0	0.772	-76.151	0.574	9.019	0.746	-74.800	0.607	14.200
5.1	0.765	-77.481	0.581	7.583	0.734	-76.020	0.617	13.140

5.2	0.759	-78.802	0.588	6.155	0.722	-77.240	0.627	12.080
5.3	0.752	-80.115	0.595	4.734	0.709	-78.460	0.636	11.020
5.4	0.745	-81.420	0.602	3.321	0.697	-79.680	0.646	9.960
5.5	0.739	-82.717	0.608	1.916	0.685	-80.900	0.656	8.900
5.6	0.735	-84.006	0.615	0.517	0.678	-82.420	0.664	7.200
5.7	0.725	-85.287	0.621	-0.874	0.671	-83.940	0.671	5.500
5.8	0.719	-86.561	0.628	-2.258	0.664	-85.460	0.679	3.800
5.9	0.712	-87.826	0.634	-3.635	0.657	-86.980	0.686	2.100
6.0	0.705	-89.084	0.640	-5.005	0.650	-88.500	0.694	0.400
6.1	0.699	-90.334	0.645	-6.368	0.642	-90.320	0.998	-0.800
6.2	0.692	-91.577	0.651	-7.724	0.635	-92.140	0.702	-2.000
6.3	0.686	-92.813	0.657	-9.074	0.627	-93.960	0.707	-3.200
6.4	0.679	-94.041	0.662	-10.417	0.620	-95.780	0.711	-4.400
6.5	0.673	-95.261	0.667	-11.753	0.612	-97.600	0.715	-5.600
6.6	0.667	-96.475	0.672	-13.083	0.598	-97.580	0.722	-6.980
6.7	0.660	-97.681	0.677	-14.407	0.583	-97.560	0.729	-8.360
6.8	0.654	-98.880	0.682	-15.725	0.569	-97.540	0.736	-9.740
6.9	0.648	-100.073	0.687	-17.036	0.554	-97.520	0.743	-11.120
7.0	0.641	-101.258	0.692	-18.341	0.540	-97.500	0.750	-12.500

Reverse Biased Voltage 3 V

$C_1 = 0.15$ pF

$R_1 = 0.20$ Ω

FREQ GHz	Modeled				Measured			
	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S11 Mag	S11 Ang	S21 Mag	S21 Ang
5.0	0.848	-73.215	0.529	16.728	0.800	-70.500	0.549	19.100
5.1	0.843	-74.590	0.537	15.351	0.790	-71.680	0.559	18.180
5.2	0.838	-75.960	0.545	13.979	0.780	-72.860	0.569	17.260
5.3	0.833	-77.327	0.553	12.611	0.769	-74.040	0.578	16.340
5.4	0.827	-78.689	0.560	11.247	0.759	-75.220	0.588	15.420
5.5	0.822	-80.047	0.568	9.888	0.749	-76.400	0.598	14.500
5.6	0.817	-81.400	0.576	8.532	0.743	-77.920	0.607	12.760
5.7	0.812	-82.749	0.583	7.181	0.737	-79.440	0.616	11.020
5.8	0.806	-84.094	0.590	5.835	0.732	-80.960	0.624	9.280
5.9	0.801	-85.435	0.597	4.493	0.726	-82.480	0.633	7.540
6.0	0.796	-86.771	0.604	3.154	0.720	-84.000	0.642	5.800
6.1	0.790	-88.103	0.611	1.821	0.713	-85.800	0.646	4.620
6.2	0.785	-89.431	0.618	0.491	0.706	-87.600	0.651	3.440
6.3	0.780	-90.755	0.625	-0.835	0.700	-89.400	0.655	2.260

6.4	0.774	-92.075	0.632	-2.156	0.693	-91.200	0.660	1.080
6.5	0.769	-93.390	0.638	-3.473	0.686	-93.000	0.664	-0.100
6.6	0.763	-94.701	0.645	-4.786	0.672	-93.200	0.672	-1.420
6.7	0.758	-96.008	0.651	-6.095	0.658	-93.400	0.681	-2.740
6.8	0.753	-97.311	0.657	-7.399	0.643	-93.600	0.689	-4.060
6.9	0.747	-98.610	0.663	-8.700	0.629	-93.800	0.698	-5.380
7.0	0.742	-99.905	0.669	-9.997	0.615	-94.000	0.706	-6.700

APPENDIX 4

Equivalent Circuit Model of Avantek
GaAs FET ATF13136

The element values for the equivalent circuit model described in chapter 6 are listed below in Table II. The scattering parameters of this model are listed in Table III.

TABLE II

Parameter	Value
l_g	0.5354 nH
l_{gp}	0.1631 nH
l_d	0.7153 nH
l_{dp}	0.4265 nH
l_s	0.1650 nH
l_{sp}	0.1582 nH
c_{ds}	0.0847 pF
r_{ds}	218.5 Ω
g_m	0.061 mA/V
c_{gd}	0.0420 pF
c_{gs}	0.2546 pF

t	0.002 s
r_s	0.59 Ω
r_g	0.10 Ω
c_{gsp}	0.0500 pF
Parameter	Value
c_{dsp}	0.050 pF
c_{gdp}	0.005 pF
Z_1	65 Ω
l_1	35 mil
k_1	7
Z_2	30 Ω
l_2	15 mil
k_2	7
Z_3	65 Ω
l_3	35 mil
k_3	7
r_c	0.011 Ω
r_d	0 Ω

TABLE III

FREQ GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S11 Mag	S11 Ang	S21 Mag	S21 Ang
2.00	0.943	-40.786	3.996	137.322	0.042	70.312	0.382	-17.297
3.00	0.879	-61.751	3.879	116.291	0.064	60.123	0.362	-26.180
4.00	0.799	-83.498	3.724	95.623	0.086	49.610	0.334	-35.194
5.00	0.714	-106.422	3.540	75.424	0.107	38.774	0.295	-44.144
6.00	0.635	-130.918	3.335	55.778	0.128	27.661	0.248	-52.604
7.00	0.573	-157.115	3.117	36.749	0.148	16.337	0.192	-59.609
8.00	0.536	175.560	2.895	18.379	0.167	4.875	0.131	-62.437
9.00	0.529	148.524	2.676	0.687	0.183	-6.651	0.075	-50.134
10.0	0.447	123.327	2.464	-16.322	0.197	-18.179	0.061	1.944
11.0	0.580	100.783	2.264	-32.659	0.209	-29.658	0.111	27.673
12.0	0.622	808875	2.078	-48.353	0.218	-41.052	0.175	28.102

APPENDIX 5

Details of the Element Syntax and Models Used in the Computer Aided Design Work

This Appendix contains details of the syntax used in describing microwave circuit elements for analysis with the Eesof program Academy[103]. The details have been reproduced from the Eesof element catalogue[111].

Symbol:

$$1 \text{---} | \quad | \text{---} 2$$
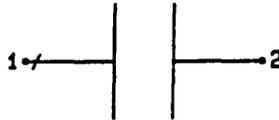
Syntax:

$CAP\text{-}xxx$ $n1$ $n2$ $C=x1$

Parameters:

_xxx   =   optional identifier tag
C   =   capacitance

Netlist Example:

CAP_C2   11   0   C=12

ACADEMY/jOMEGA Notes:

Requires an artwork replacement with Layout Option.

Element Type: Lumped
capacitor

Model Basis: Ideal
Originator -- EEsof

Range of Usage:

Frequency ≥ 0

Frequency = simulation frequency

Notes/Equations/References:

N/A
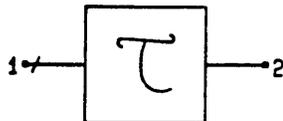
Symbol: **Illustration:**
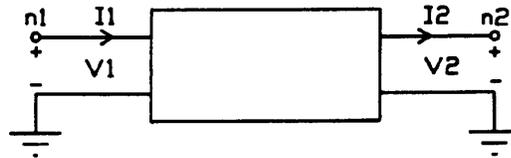
Syntax:

> *DELAY_xxx   n1   n2   T=x1*

Parameter:

> _xxx   =   optional identifier tag
> T   =   time delay

Netlist Example:

> DELAY_G3   1   2   T=10

ACADEMY/jOMEGA Notes:

> Requires an artwork replacement with Layout Option.

Element Type: Universal
time-delay

Model Basis: Mathematical
Originator -- EEsof

Range of Usage:

Frequency ≥ 0

Frequency = simulation frequency

Notes/Equations/References:

$$\frac{V2}{V1} = \frac{I2}{I1} = e^{-(j\,2\,\pi\,f\,T)}$$

$$s11 = s22 = 0$$

$$s21 = e^{-(j\,2\,\pi\,f\,T)}$$

$$s12 = e^{(j\,2\,\pi\,f\,T)}$$

where

f = Simulation frequency

Symbol:
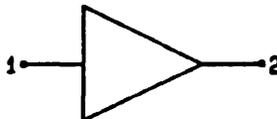
Syntax:

GAIN_xxx   *n1*   *n2*   *A=x1*   *S=x2*   *F=x3*

Parameters:

_xxx	=	optional identifier tag
A	=	constant gain (loss) in dB
S	=	gain (loss) slope in db/octave
F	=	frequency at which slope starts

Netlist Example:

GAIN_G3   1   2   A=6   S=-6   F=1.5

ACADEMY/jOMEGA Notes:

Requires an artwork replacement with Layout Option.

Element Type: Universal
ideal gain or loss element

Model Basis: Mathematical, ideal
Originator -- EEsof

Range of Usage:

Frequency ≥ 0

$A(f) = A$ for $f \leq F$ or $F = 0$ or $S = 0$

$A(f) = A + S * \log_2 (f/F)$ for $f > F$, $S > 0$ and $F > 0$

f = simulation frequency

F = reference frequency

Equivalent Circuit:
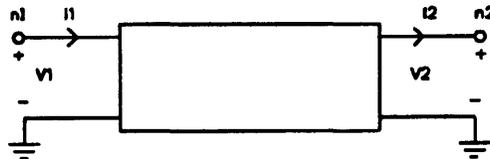
Notes/Equations/References:

Any number of gain elements can be cascaded to obtain an arbitrary shape as a function of frequency.

If $F = 0$, S is ignored.

$$\frac{V2}{V1} = \frac{I2}{I1} = A(f)$$

$s11 = s22 = 0$

$s21 = A(f)$

$$s12 = \frac{1}{A(f)}$$

Symbol:

Syntax:

IND_xxx   *n1*   *n2*   *L=x1*

Parameter:

_xxx	=	optional identifier tag
L	=	inductance

Netlist Example:

IND_L5   1   2   L=1.3

ACADEMY/jOMEGA Notes:

Requires an artwork replacement with Layout Option.

Element Type: Lumped
Ideal inductor

Model Basis: Ideal
Originator -- Ideal

Range of Usage:

     Frequency ≥ 0

         Frequency = simulation frequency

Notes/Equations/References:

     N/A

Symbol: **Illustration:**

"SMALL" MITERS   "LARGE" MITERS

$$M < M_s \qquad\qquad M \geq M_s$$

$$M = \frac{X}{D}$$

$$M_s = Sin^2\left(\frac{Angle}{2}\right)$$
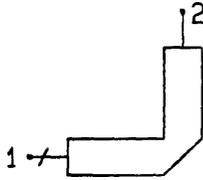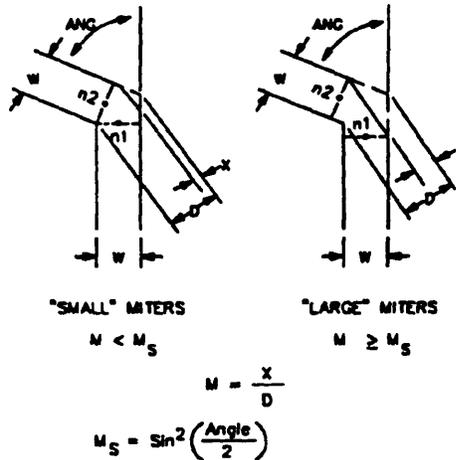
Syntax:

    MBEND_xxx   n1   n2   W=x1   ANG=x2   M=x3

Parameters:

_xxx	=	optional identifier tag
W	=	conductor width
ANG	=	angle of bend
M	=	miter (M=X/D)

Netlist Example:

    MBEND_T6   1   2   W=25   ANG=90   M=0.5

ACADEMY/jOMEGA Notes:

Be sure to review *Using Global Material Specifications* in the front section of this manual.

A positive value for ANG specifies a bend to the left from n1 to n2 as shown in the illustration. A negative value for ANG specifies a bend to the right.

Element Type: Microstrip
                      bend with arbitrary angle and miter

Model Basis: Mathematical
                      Originator -- reference

Range of Usage:

Frequency $\geq$ 0

$1 \leq$ Er $\leq$ 128

$-90° \leq$ ANG $\leq$ 90°

$.01 \leq \dfrac{W}{H} \leq 100$

Frequency	=	simulation frequency
Er	=	dielectric constant
H	=	substrate height

Notes/Equations/References:

For right angle bends, it is recommended you use MBEND2, MBEND3, or MCORN.

Be sure to review *Using Global Material Specifications* in the front section of this manual.

Requires an MSUB symbol on the same design sheet.

There are two possible reference plane locations available:

■   Small miters where the reference planes line up with the inner corner of the bend, or

■   Large miters where the reference planes line up with the corner between the connecting strip and the mitered section.

Improved modeling for this element in Version 3.0 may result in improved data differing from previous program versions. For more details, refer to *Element Performance Changes by Program Version* in the front section of this manual.

Kirschning, M., Jansen, R.H., and Koster, N.H.L.,"Measurement and Computer-Aided Modeling of Microstrip Discontinuities by an Improved Resonator Method," *1983 IEEE MTT-S International Microwave Symposium Digest*, May 1983, pp. 495-497.

Symbol:
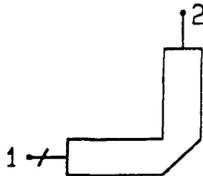
Illustration:
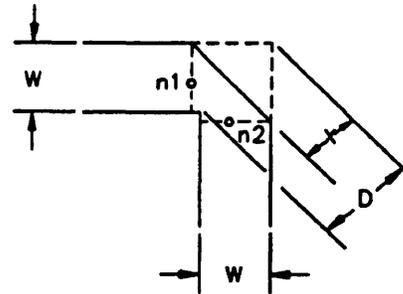
Syntax:

MBEND3_xxx   *n1*   *n2*   *W=x1*

Parameters:

_xxx	=	optional identifier tag
W	=	conductor width

Netlist Example:

MBEND3_T5   1   2   W=24.1

ACADEMY/jOMEGA Notes:

Be sure to review *Using Global Material Specifications* in the front section of this manual.

The shape of the layout artwork is dependent on the substrate height given in the MSUB element.

Element Type: Microstrip
bend with optimal mitered 90° bend

Model Basis: Mathematical
Originator -- reference

Range of Usage:

Frequency $\leq \dfrac{15}{H \,(mm)}$ (GHz)

$2.5 \leq E_r \leq 25$

Angle = 90°

$0.5 \leq \dfrac{W}{H} \leq 2.75$

Frequency	=	simulation frequency
E_r	=	substrate dielectric constant
H	=	substrate height

Notes/Equations/References:

Be sure to review *Using Global Material Specifications* in the front section of this manual.

Requires an MSUB symbol on the same design sheet.

Improved modeling for this element in Version 3.0 may result in improved data differing from previous program versions. For more details, refer to *Element Performance Changes by Program Version* in the front section of this manual.

Optimum miter is given by

$$\frac{X}{D} = 0.52 + 0.65 * e^{-1.35 \cdot \frac{W}{H}}$$

where H = substrate height

Douville, R.J.P., and James, D.S., "Experimental Characterization of Microstrip Bends and Their Frequency Dependent Behavior," *1973 IEEE Conference Digest*, October 1973, pp. 24-25.

Douville, R.J.P., and James, D.S., "Experimental Study of Symmetric Microstrip Bends and Their Compensation," *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-26, March 1978, pp. 175-181.
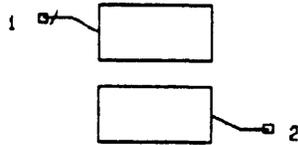
Symbol: **Illustration:**
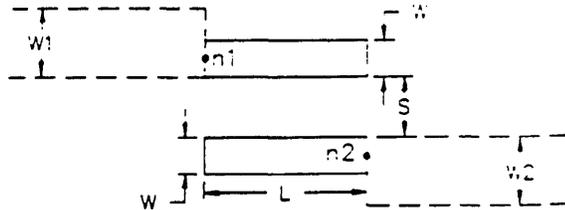
Syntax:

MCFIL_xxx   n1   n2   W=x1   S=x2   L=x3   W1=x4   W2=x5

Parameters:

_xxx	=	optional identifier tag
W	=	width
S	=	spacing
L	=	length
W1	=	width of line that connects to node 1 (for generating a layout)
W2	=	width of line that connects to node 2 (for generating a layout)

Netlist Example:

MCFIL_T6   1   2   W=20   S=5   L=130   W1=25   W2=50

Layout Notes:

In generating a layout, Layout lines up the inner edges of the conductor strips unless the connecting transmission lines are narrower than the coupled lines. The program then centers the transmission lines on the coupled lines.

W1 and W2 are required only for generating a layout and do not affect the results of simulation.

If there is no input strip, specify a zero width.

Element Type: Microstrip
coupled line filter section
with built-in open-end effect

Model Basis: Mathematical
Originator -- EEsof

Range of Usage:

Frequency $\leq \dfrac{25}{H \ (mm)}$ (GHz)

$1 \leq E_r \leq 18$

$0.1 \leq \dfrac{W}{H} \leq 10$

$0.1 \leq \dfrac{S}{H} \leq 10$

Frequency   =   simulation frequency
E_r =   dielectric constant
H =   substrate height

Notes/Equations/References:

Requires an MSUB symbol on the same design sheet.

Garg, R., and Bahl, I.J.,"Characteristics of Coupled Microstriplines," *MTT-27*, July 1979.

Kirschning, M., and Jansen, R.H., "Accurate Wide-Range Design Equations for the Frequency-Dependent Characteristic of Parallel Coupled Microstrip Lines," *MTT-32*, January 1984 (with corrections by EEsof).

The use of impedance dispersion with this model can be selected (on or off) with EECONFIG as follows:

Setting in EECONFIG	Impedance Dispersion Used?
Getsinger	No
Kirschning & Jansen	Yes
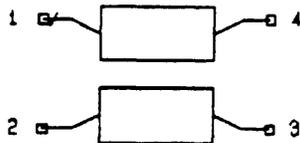
Symbol: Illustrations:
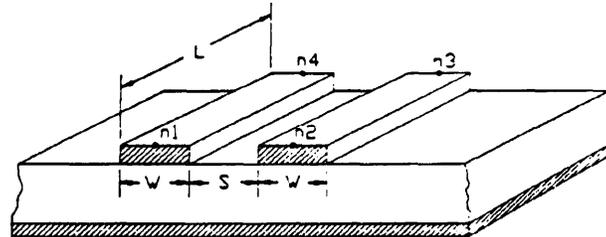
Syntax:

MCLIN_xxx   n1 n2 n3 n4 =x1 S=x2 L=x3 W1=x4 W2=x5 W3=x6 W4=x7

Parameters:

_xxx	=	optional identifier tag
W	=	width of microstrip coupled lines
S	=	space between coupled lines
L	=	length of coupled lines
W1	=	width of line that connects to node 1 (for generating a layout)
W2	=	width of line that connects to node 2 (for generating a layout)
W3	=	width of line that connects to node 3 (for generating a layout)
W4	=	width of line that connects to node 4 (for generating a layout)

Netlist Example:

MCLIN_S6   1 2 3 4 W=23.2 S=2 L=85 W1=25 W2=30 W3=40 W4=25

Layout Notes:

In generating a layout, Layout aligns the inner edges of the conductor strips unless the connecting transmission lines are narrower than the couples lines. The program then centers the connecting transmission lines on the coupled lines.

If there is no input strip, specify a zero width.

Element Type: Microstrip
coupled lines

Model Basis: Mathematical
Originator -- reference

Range of Usage:

Frequency $\leq \dfrac{25}{H \text{ (mm)}}$ (GHz)

$1 \leq E_r \leq 18$

$T \geq 0$

$0.1 * H \leq W \leq 10.0 * H$

$0.1 * H \leq S \leq 10.0 * H$

Frequency	=	simulation frequency
E_r	=	dielectric constant
H	=	substrate height

Notes/Equations/References:

Requires an MSUB symbol on the same design sheet.

The use of impedance dispersion with this model can be selected (on or off) with EECONFIG as follows:

Setting in EECONFIG	Impedance Dispersion Used?
Getsinger	No
Kirschning & Jansen	Yes

Kirschning, M., and Jansen, R.H., "Accurate Wide-Range Design Equations for the Frequency-Dependent Characteristic of Parallel Coupled Microstrip Lines," *MTT-32*, January 1984 (with corrections by EEsof).

Garg, R., and Bahl, I.J.,"Characteristics of Coupled Microstriplines," *MTT-27*, July 1979.

Symbol:
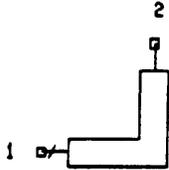
Illustration:
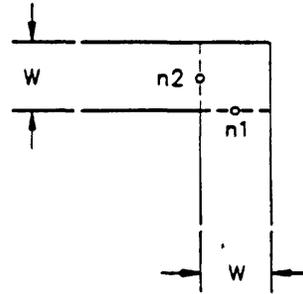
Syntax:

    MCORN_xxx   *n1 n2 W=x1*

Parameter:

    _xxx   =   optional identifier tag
    W   =   conductor width

Netlist Example:

    MCORN_T4   21 22 W=25

Layout Notes:

    N/A

Element Type: Microstrip
bend with 90° fixed angle and no miter

Model Basis: Mathematical
Originator -- reference

Range of Usage:

Frequency $\leq \dfrac{12}{H\ (mm)}$ (GHz)

$2.36 \leq E_r \leq 10.4$

$0.2 \leq \dfrac{W}{H} \leq 6.0$

Frequency	=	simulation frequency
E_r	=	dielectric constant
H	=	substrate height

Notes/Equations/References:

Requires an MSUB symbol on the same design sheet.

Kirschning, M., Jansen, R.H., and Koster, N.H.L., "Measurement and Computer-Aided Modeling of Microstrip Discontinuities by an Improved Resonator Method," *1983 IEEE MTT-S International Microwave Symposium Digest*, May 1983, pp. 495-497.

Marcuvitz, N., *Waveguide Handbook*, McGraw-Hill, New York, 1951, pp. 312-313.

Symbol:
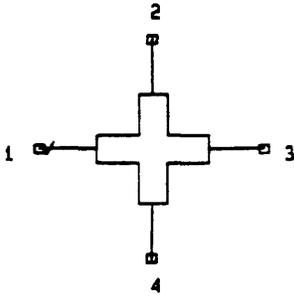
Illustration:
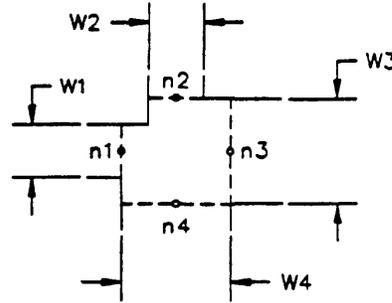
Syntax:

MCROS_xxx   *n1*   *n2*   *n3*   *n4*   *W1=x1*   *W2=x2*   *W3=x3*   *W4=x4*

Parameters:

_xxx	=	optional identifier tag
W1	=	width of line that connects to node 1
W2	=	width of line that connects to node 2
W3	=	width of line that connects to node 3
W4	=	width of line that connects to node 4

Netlist Example:

MCROS_T8   23 24 25 26 W1=24 W2=30 W3=24 W4=30

Layout Notes:

In generating a layout, Layout aligns the centerlines of the transmission lines connected to nodes 1 and 3 and the centerlines of the transmission lines connected to nodes 2 and 4.

Element Type: Microstrip
                     cross discontinuity

Model Basis: Mathematical
                     Originator -- EEsof - modified reference

Range of Usage:

Frequency $\geq$ 0

$$0.4 \leq \frac{W_i}{H} \leq 2.5$$

Frequency   =   simulation frequency
H   =   substrate height

Notes/Equations/References:

Requires an MSUB symbol on the same design sheet.

Gupta, K.C., Garg, R., and Chadha, R., "Computer-Aided Design of Microwave Circuits," Artech House, 1981, pp. 197-199.

Improved modeling for MCROS in Touchstone Version 3.0 and Libra Version 3.0 may result in improved data differing from previous program versions.

Symbol:
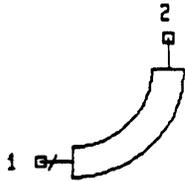
Illustration:
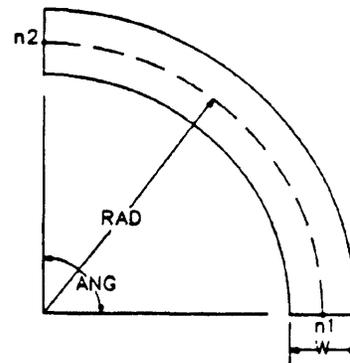
Syntax:

MCURVE_xxx   n1   n2   W=x1   ANG=x2   RAD=x3

Parameters:

_xxx	=	optional identifier tag
W	=	width of the microstrip transmission line
ANG	=	angle of the bend
RAD	=	radius of the bend measured to the center of the microstrip transmission line

Netlist Example:

MCURVE_T6   10   11   W=24   ANG=-90   RAD=100

Layout Notes:

A positive value for ANG specifies curvature to the left from n1 to n2 as shown in the illustration. A negative value for ANG specifies curvature to the right.

Element Type: Microstrip
                      curved bend with arbitrary angle

Model Basis: Mathematical
                      Originator – EEsof

Range of Usage:

Frequency ≥ 0

$0.01 * H \leq W \leq 100 * H$

$RAD \geq W/2$

$-180° \leq ANG \leq 180°$

Frequency	=	simulation frequency
H	=	substrate height

Notes/Equations/References:

Requires an MSUB symbol on the same design sheet.

Improved modeling for MCURVE in Touchstone Version 3.0 and Libra Version 3.0 may result in improved data different from previous program versions.

The use of impedance dispersion with this model can be selected (on or off) with EECONFIG as follows:

Setting in EECONFIG	Impedance Dispersion Used?
Getsinger	No
Kirschning & Jansen	Yes

Symbol: **Illustration:**
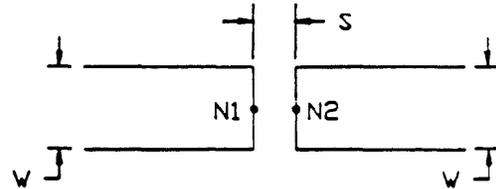
Syntax:

> *MGAP_xx*   *n1*   *n2*   *W=x1*   *S=x2*

Parameters:

_xxx	=	optional identifier tag
W	=	conductor width
S	=	gap spacing

Netlist Example:

> MGAP_T3   1   2   W=25   S=2.5

Layout Notes:

> N/A

Element Type: Microstrip
                    gap

Model Basis: Mathematical
                    Originator -- reference

Range of Usage:

Frequency $\geq$ 0

$1 \leq E_r \leq 15$

$0.5 \leq \dfrac{W}{H} \leq 2.0$

$0.1 \leq \dfrac{S}{H} \leq 2.0$

Frequency	=	simulation frequency
E_r	=	dielectric constant
H	=	substrate height

If $S/H \leq 10^{-7}$, then S = 0 is used.

Notes/Equations/References:

Requires an MSUB symbol on the same design sheet.

Hammerstad, E., "Computer Aided Design of Microstrip Couplers with Accurate Discontinuity Models," *IEEE MTT-S International Microwave Symposium Digest*, June 1981, pp. 54-56 (with modifications).
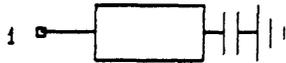
Symbol: **Illustration:**
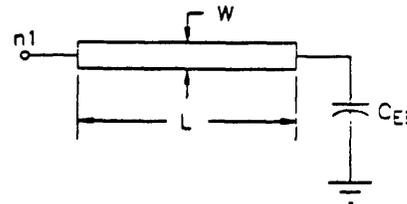
Syntax:

> *MLEF_xxx   n1   W=x1   L=x2*

Parameters:

_xxx	=	optional identifier tag
W	=	microstrip line width
L	=	microstrip line length

Netlist Example:

> MLEF_T2   1   W=35   L=180

Layout Notes:

> N/A

Element Type: Microstrip
open-end transmission line
with end effect included

Model Basis: Mathematical
Originator -- reference

Range of Usage:

Frequency ≥ 0

$2 \leq E_r \leq 50$

$\dfrac{W}{H} \geq 0.2$

Frequency	=	simulation frequency
E_r	=	dielectric constant
H	=	substrate height

Notes/Equations/References:

Fringing at the open end of the line is calculated and included in the model.

Requires an MSUB symbol on the same design sheet.

Kirschning, M., Jansen, R.H., and Koster, N.H.L., "Accurate Model for Open-End Effect of Microstrip Lines," *Electronics Letters*, Vol. 17, No. 3, pp. 123-125, February 5, 1981.

Improved modeling for MLEF in Touchstone Version 3.0 and Libra Version 3.0 may result in improved data differing from previous program versions.

The use of impedance dispersion with this model can be selected (on or off) with EECONFIG as follows:

Setting in EECONFIG	Impedance Dispersion Used?
Getsinger	No
Kirschning & Jansen	Yes
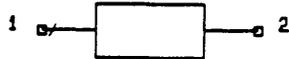
**Symbol:**   **Illustration:**
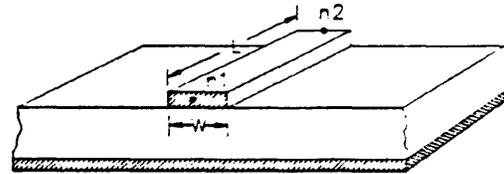
Syntax:

> *MLIN_xxx   n1   n2   W=x1   L=x2*

Parameters:

> _xxx   =   optional identifier tag
> W   =   microstrip line width
> L   =   microstrip line length

Netlist Example:

> MLIN_T3   1   2   W=24   L=110

Layout Notes:

> N/A

Element Type: Microstrip
transmission line

Model Basis: Mathematical
Originator -- reference

Range of Usage:

Frequency ≥ 0

$1 \leq E_r \leq 128$

$0.01 \leq \dfrac{W}{H} \leq 100$

Frequency	=	simulation frequency
E_r	=	dielectric constant
H	=	substrate height

Notes/Equations/References:

Requires an MSUB symbol on the same design sheet.

Getsinger, W.J., "Measurement and Modeling of the Apparent Characteristic Impedance of Microstrip," *MTT-31*, August 1983.

Hammerstad, E. and Bekkadal, F., *Microstrip Handbook*, ELAB Report STF44 A74169, February 1975.

Hammerstad, E. and Jensen, O., "Accurate Models for Microstrip Computer-Aided Design," *MTT Symposium Digest*, 1980.

Kirschning, M. and Jansen, R.H., *Electronics Letters*, January 18, 1982.

Improved modeling for MLIN in Touchstone Version 3.0 and Libra Version 3.0 may result in improved data differing from previous program versions.
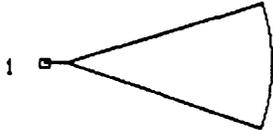
Symbol: Illustration:
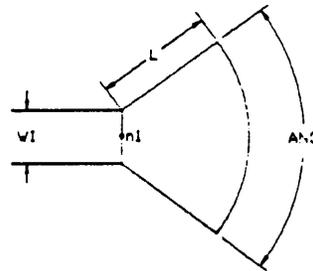
Syntax:

> *MRSTUB_xxx   n1   WI=x1   L=x2   ANG=x3*

Parameters:

_xxx	=	optional identifier tag
WI	=	conductor width at input
L	=	length
ANG	=	angle

Netlist Example:

> MRSTUB_T3   1   WI=25   L=175   ANG=70

Layout Notes:

> N/A

Element Type: Microstrip
                      radial line stub

Model Basis: Mathematical
                      Originator -- EEsof

Range of Usage:

Frequency $\geq$ 0

E_r $\leq$ 128

$10° \leq$ ANG $\leq 170°$

$.01 \leq \dfrac{WI}{H} \leq 100$

L * ANG(radians) ≤ 100 * H

|		
Frequency	=	simulation frequency
H	=	substrate height
Er	=	dielectric constant

Notes/Equations/References:

MRSTUB should be used with MTEE or MCROS when used as a stub in shunt with a transmission line.

A lossless model is used in computing the values for MRSTUB.

Requires an MSUB symbol on the same design sheet.

Illustration:
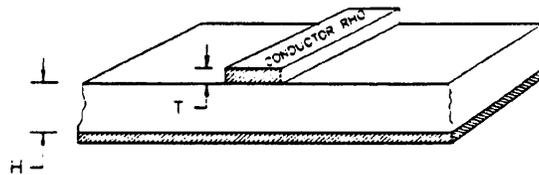
Syntax:

MSUB_xxx   ER=x1   H=x2   T=x3   RHO=x4   RGH=x5

Parameters:

_xxx	=	optional identifier tag
ER	=	substrate relative dielectric constant
H	=	substrate thickness
T	=	metal thickness
RHO	=	metal bulk resistivity normalized to that of gold
RGH	=	rms surface roughness, in units of length

Netlist Example:

MSUB_P2   ER=3.78   H=15   T=.1   RHO=1   RGH=0

Layout Notes:

N/A

Element Type: Microstrip
                      substrate specification

Model Basis: Mathematical
                      Originator -- EEsof

Range of Usage:

Frequency $\geq$ 0

This specification must precede any microstrip element or coplanar waveguide.

Frequency = simulation frequency

Notes/Equations/References:

Bulk resistivity references 2.44 microhm - cm (gold)
Circuit resistivity = RHO * 2.44 microhm - cm

Losses are accounted for when RHO > 0 and T > 0. The RGH parameter modifies the loss calculations.

An MSUB symbol is required for all microstrip elements and coplanar waveguides.
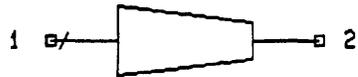
Symbol: **Illustration:**
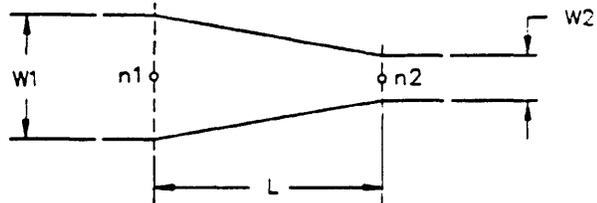
Syntax:

MTAPER_xxx   n1   n2   W1=x1   W2=x2   L=x3

Parameters:

_xxx	=	optional identifier tag
W1	=	conductor width
W2	=	conductor width
L	=	taper length

Netlist Example:

MTAPER_T3   1   2   W1=25   W2=50   L=100

Layout Notes:

N/A

Element Type: Microstrip
                    linear width taper

Model Basis: Mathematical
                    Originator – EEsof

Range of Usage:

Frequency $\geq$ 0

$E_T \leq 128$

$0.01 * H \leq (W1, W2) \leq 100 * H$

Frequency	=	simulation frequency
E_T	=	dielectric constant
H	=	substrate height

Notes/Equations/References:

Requires an MSUB symbol on the same design sheet.

Improved modeling for MTAPER in Touchstone Version 3.0 and Libra Version 3.0 may result in improved data differing from previous program versions.

Symbol:

Illustration:

Syntax:

MTEE_xxx   *n1*   *n2*   *n3*   *W1=x1*   *W2=x2*   *W3=x3*

Parameters:

_xxx	=	optional identifier tag
W1	=	line width at node 1
W2	=	line width at node 2
W3	=	line width at node 3

Netlist Example:

MTEE_T4   27   25   28   W1=25   W2=20   W3=10

Layout Notes:

N/A

Element Type: Microstrip
T-junction

Model Basis: Mathematical
Originator -- EEsof-modified reference

Range of Usage:

Frequency ≥ 0

$E_r \leq 128$

$W1 + W3 \leq 0.5\ \lambda$

$W2 + W3 \leq 0.5\ \lambda$

$.01 \leq \dfrac{W1}{H} \leq 100$

$.01 \leq \dfrac{W2}{H} \leq 100$

$.01 \leq \dfrac{W3}{H} \leq 100$

Frequency	=	simulation frequency
H	=	substrate height
λ	=	wavelength in the dielectric

Notes/Equations/References:

The center lines of the strips connected to n1 and n2 are assumed to be aligned.

Requires an MSUB symbol on the same design sheet.

Hammerstad, E., "Computer-Aided Design of Microstrip Couplers Using Accurate Discontinuity Models," *MTT Symposium Digest*, 1981.

Improved modeling for MTEE in Touchstone Version 3.0 and Libra Version 3.0 may result in improved data differing from previous program versions.
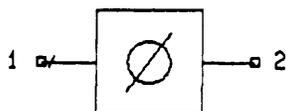

Symbol: **Illustration:**
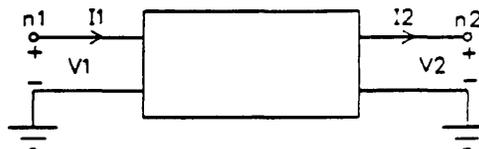
Syntax:

$PHASE\_xxx$ nl $n2$ $A=x1$ $S=x2$ $F=x3$

Parameters:

_xxx	=	optional identifier tag
A	=	constant phase (for frequency < F)
S	=	slope in angle units per octave
F	=	frequency at which slope starts, F > 0

Netlist Example:

PHASE_G3   1   2   A=45   S=−30   F=1.5

Layout Notes:

Requires an artwork replacement in Layout.

Element Type: Universal
                     phase shift element

Model Basis: Mathematical, ideal
                     Originator -- EEsof

Range of Usage:

$f \geq 0$

$\theta(f) = A$ $(f < F)$

$\theta(f) = A + S * LOG_2(f/F)$ $(f \geq F)$

If F = 0, then phase slope is zero regardless of the setting of S.

      f = simulation frequency

Notes/Equations/References:

$$\frac{V2}{V1} = \frac{I2}{I1} = e^{j\theta(f)}$$

$$s_{11} = s_{22} = 0$$

$$s_{21} = e^{j\theta(f)}$$

$$s_{12} = e^{-j\theta(f)}$$

Symbol:

1 o—/\/\/\/\—o 2

Syntax:

RES_xxx   *n1   n2   R=x1*

Parameters:

_xxx   =   optional identifier tag
R   =   resistance

Netlist Example:

RES_R4   1   25   R=25

Layout Notes:

Requires an artwork replacement in Layout.

Element Type: Lumped
resistor

Model Basis: Ideal
Originator -- EEsof

Range of Usage:

Frequency > 0

Frequency = simulation frequency

Notes/Equations/References:

N/A

Symbol:
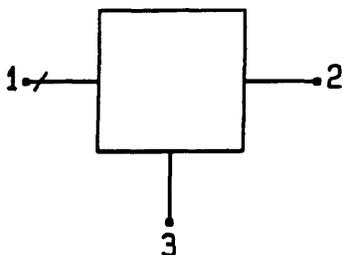
Syntax:

S2P_xxx   *nl*   *n2*   *n3*   *dataFile*

S2P_xxx   *nl*   *n2*   *n3*   *filename [varl=xl var2=_RANDOM var3^x3....varm=xm]*

Parameters:

_xxx	=	optional identifier tag
dataFile	=	a file containing 2-port S-, Y-, Z-, G-, or H-parameters for this element
filename	=	name of the parametric MDIF file
varm	=	MDIF variable up to 8 characters long. Can be an arbitrary name since an MDIF file can have variables with arbitrary names. Typical examples: TEMP, BIAS, SAMPLE, etc.
=, ^	=	equal and variable assignments allowed
_RANDOM	=	optional. For statistical analysis purposes, it generates a "truth model" for that element. The MDIF variable to which _RANDOM is assigned is randomized.

Netlist Examples:

S2P_S6   11   10   0   NEC70000.S2P

S2P_S8   2   3   0   NE045.MDF   [DATE=Fri Dec 21 1989   TEMP=30 &
                                   BIAS^VDD   LOTID=NEC 045 Lot 45G]

ACADEMY/jOMEGA Notes:

Requires an artwork replacement with Layout Option.

Element Type: Universal
                     2-port data file

Model Basis: Mathematical
                     Originator -- EEsof

Range of Usage:

Frequency ≥ 0

S-, Y-, Z-, G-, or H-parameters only

Noise parameters may be included at the end of the file.

Frequency = simulation frequency

Notes/Equations/References:

In order to use the network analyzer for this element, refer to the appendix, *Network Analyzer Setup*, in your simulator manual.

The parameters specified in the data file are assumed to correspond to the following configuration:

Node n1	Input
Node n2	Output
Node n3	Common

General Use of the MDIF File

If there are one or more MDIF variable names given in square brackets after the filename, it is an MDIF file. If there are no square brackets after the filename, it is a standard S-parameter file.

The file extension must be specified. There is no default extension.

Square brackets are necessary if one or more MDIF variables are to be specified.

A maximum of 10 MDIF variables can be specified in any order.

The S-parameter data set within the MDIF file is selected based on its existence at the specified values (x1, x2, etc.) of the specified MDIF variable names (var1, var2, etc.).
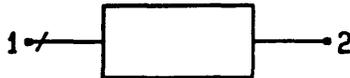

Symbol: Illustration:
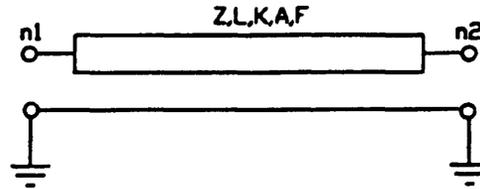
Syntax:

TLINP_xxx   n1   n2   Z=x1   L=x2   K=x3   A=x4   F=x5

Parameters:

_xxx	=	optional identifier tag
Z	=	characteristic impedance
L	=	physical length
K	=	effective dielectric constant
A	=	attenuation [dB / unit length]
F	=	frequency for scaling attenuation

Netlist Example:

TLINP_T4   11   15   Z=35   L=85   K=6.62   A=0.00035   F=1

ACADEMY/jOMEGA Notes:

Be sure to review *Using Global Material Specifications* in the front section of this manual.

Requires an artwork replacement with Layout Option.

Element Type: Universal
                    physical 2-node transmission line

Model Basis: Mathematical
                    Originator -- EEsof

Range of Usage:

Frequency $\geq$ 0

Frequency = simulation frequency

Notes/Equations/References:

Be sure to review *Using Global Material Specifications* in the front section of this manual.

$$A(f) = A \qquad\qquad \text{for } F = 0$$

$$A(f) = A(F) * \sqrt{\frac{f}{F}} \qquad \text{for } F \neq 0$$

f   =   simulation frequency
F   =   reference frequency

Symbol:
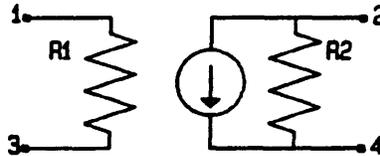
Syntax:

VCCS_xxx   *n1* *n2* *n3* *n4*   *M=x1*   *A=x2*   *R1=x3*   *R2=x4*   *F=x5*   *T=x6*

Parameters:

_xxx	=	optional identifier tag
M	=	I G(0) I; magnitude of transconductance at dc
A	=	phase offset of transconductance in angle units
R1	=	input resistance
R2	=	output resistance
F	=	frequency at which transconductance magnitude is down by 3dB
T	=	time delay associated with transconductance

Netlist Example:

VCCS_I8   22 28 29   M=0.05   A=30   R1=1E6   R2=0   F=20   T=0

ACADEMY/jOMEGA Notes:

Requires an artwork replacement with Layout Option.

Element Type: Controlled source
                    voltage controlled current source

Model Basis: Lumped equivalent circuit
                    Originator -- EEsof

Range of Usage:

Frequency $\geq$ 0

| Setting	Result
F = 0	F = ∞
T = 0	T = 0
R1 = 0	R1 = 0
R2 = 0	R2 = ∞

Frequency = simulation frequency

Equivalent Circuit:
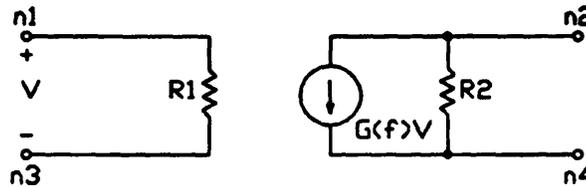
Notes/Equations/References:

$$G(f) = G(0) \;*\; \frac{e^{-(j\,2\,\pi\,f\,T\,-\,A_{radians})}}{1 + j\frac{f}{F}} \qquad (F \neq 0)$$

$$G(f) = G(0) \;*\; e^{-(j\,2\,\pi\,f\,T\,-\,A_{radians})} \quad (F = 0)$$

f = simulation frequency
F = reference frequency

GAASFET_Axxx	Gallium Arsenide Field Effect Transistor	GAASFET_Axxx

Symbol:


```
                              2  drain
                        1
               gate  o─────

                              3  source
```
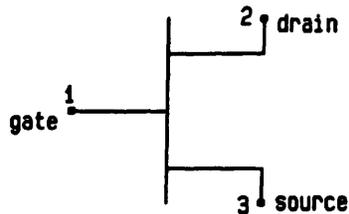
Syntax:

CKT
 GAASFET_Axxx *n1* *n2* *n3* {*dataFile*} [*MODEL* = *modelname* {*AREA=x1*}]

Parameters:

_Axxx	=	required identifier tag
dataFile	=	a 2-port S-parameter file, required only for linear simulation
MODEL	=	a GaAsFET device model name defined in the MODEL block as GaAsFET MODEL 1, 2, or 2.5 and used for nonlinear simulation
AREA	=	an optional factor that scales certain parameter values in the MODEL block
[ ]	=	square brackets are required
{ }	=	braces indicate optional entries

Netlist Example:

CKT
 GAASFET_A12 10 20 0 FETS.S2P [MODEL = MODEL2 AREA=1]

ACADEMY/jOMEGA Notes:

Requires an artwork replacement with Layout Option.

GAASFET_Axxx	Gallium Arsenide Field Effect Transistor	GAASFET_Axxx

---

Element Type: Nonlinear device
                    field effect transistor

Model Basis: Mathematical
                    Originator -- EEsof-modified reference

Range of Usage:

Libra only

Notes/Equations/References:

For nonlinear simulation (including DC bias and DCTR simulations), the data file is
ignored. For linear simulation, entries in the square brackets are ignored.

MODELS 1, 2, and 2.5 are the GaAsFET models defined in the MODEL block.

The AREA parameter permits changes to a specific semiconductor since semiconductors
may share the same model. The following parameters are scaled proportionally to
AREA:

A0, A1, A2, A3, BETA , CGS, CGD, CGSO, CGDO, CDS, IS

while the resistive parameters are scaled inversely proportional to AREA:

RD, RG, RS

For example, MODEL=1 and AREA=3 use the following computations:

RD/3	CGSO*3	BETA*3
RG/3	CGDO*3	
RS/3	CDS*3	

These computations have the same effect as placing three devices in parallel to simulate a
larger device and are much more efficient.

GAASFET_Axxx   **Gallium Arsenide**   **GAASFET_Axxx**
                   Field Effect Transistor

GaAsFET MODEL Block Syntax

modelname GAS parameters

MODEL Block Parameters

modelname	=	the name of the model from the CKT block.
GAS	=	specification that the device is a GaAsFET.
parameters	=	one parameter or more from Table SEL-2; parameters not used are set to the default values shown in the table; note that parameter MODEL=1, MODEL=2, or MODEL=2.5 depends on quadratic, cubic, or improved quadratic fit for ids.

MODEL Block Example:

```
GASMDL2  GAS  MODEL=1  VTO=-2.5  LAMBDA=0.035  ALPHA=1.5  &
         BETA=32.5E-6  TAU=0  RD=0  RS=0  CGSO=6F  &
         CGD=0.3F  CDS=0.0  VBI=0.5  RG=0  FC=0.95
```

References:

Curtice, Walter R. and Ettenberg, M. "A Nonlinear GaAs Fet Model for Use in the Design of Output Circuits for Power Amplifiers," *IEEE Transactions of Microwave Theory and Techniques*, Vol. MTT-33 No. 12, December 1985.

Haus, H. A.; Newman, P.; Pucel, R. A.; Smith, I. W.; and Statz, H., "GaAsFET Device and Circuit Simulation in SPICE," *IEEE Transactions of Microwave Theory and Techniques*, Vol. ED-34, No. 2, Pages 160-169, February 1987, the basis for the Raytheon (MODEL 2.5) model.

See also MODEL Block Notes following Table SEL-4.

Table SEL-4. GaAsFET MODEL Block Parameters

NAME	MEANING	UNIT	DEFAULT VALUE
A5	Coefficient for TAU's VDS dependency, i.e., TAU = A5*VDS (Do not use TAU and A5 together.)	S/V	0.0
AF	Flicker noise exponent (not used)	-	1.0
CDS[1]	Drain-source capacitance	F	0.0
CRF	Used with RC to model frequency dependency of the output conductance	F	0.0
FC	Coefficient for forward bias used in capacitance equation (diode model)	-	0.5
KF	Flicker noise coefficient (not used)	-	0.0
MODEL	Model index, either 1, 2 or 2.5		1
	= 1 : Curtice model (quadradic fit for ids)		
	= 2 : modified Curtice and Ettenberg model (cubic fit for ids)		
	= 2.5: Raytheon model		
RC	Used with CRF to model frequency dependency of the output conductance	ohms	infinity
RD[1]	Drain ohmic resistance	ohms	0.0
RG[1]	Gate ohmic resistance	ohms	0.0
RS[1]	Source ohmic resistance	ohms	0.0
TAU	Transit time under gate (If TAU is used, A5 is ignored.)	S	0.0
TM	ids temperature factor	-	0.0
VBI	Built-in gate potential	V	0.8
VBR	Gate junction reverse bias breakdown voltage or drain gate reverse bias breakdown voltage	V	infinity
	with vds = 0	V	infinity

<u>**Symmetric Curtice Model Parameter Subset**</u>

| NAME	MEANING	UNIT	DEFAULT VALUE
CGDO[1]	Zero bias gate-drain junction capacitance (diode model)	F	0.0
CGSO[1]	Zero bias gate-source junction capacitance (diode model)	F	0.0
EG	Energy gap (diode model)	ev	1.11
IS[1]	Gate junction saturation current (diode model)	I	1.0E-14
N	Gate-drain and gate-source emission coefficient (diode model)		1.0
XTI	Saturation current temperature exponent (diode model)		3.0

[1]This parameter value is scaled with AREA.

Table continues

Table SEL-4. GaAsFET MODEL Block Parameters (continued)

NAME	MEANING	UNIT	DEFAULT VALUE
	**Asymmetric Curtice Model Parameter Subset**		
CGD[1]	Gate-drain capacitance	F	0.0
CGS[1]	Gate-source capacitance	F	0.0
R1	Approximate breakdown resistance	ohms	infinity
R2	Resistance relating breakdown voltage to channel	ohms	0.0
RF	Effective value of forward bias resistance at gate to source	ohms	infinity
RIN	Gate-source resistance	ohms	0.0
	**MODEL=1 Parameter Subset**		
ALPHA	Hyperbolic tangent function parameter	1/V	0.0
BETA[1]	Transconductance parameter	A/V**2	0.0
LAMBDA	Channel length modulation parameter	1/V	0.0
VTO	Threshold voltage	V	-2.0
	**MODEL=2 Parameter Subset**		
A0[1]	Cubic fit ids equation coefficient	A	0.0
A1[1]	Cubic fit ids equation coefficient	A/V	0.0
A2[1]	Cubic fit ids equation coefficient	A/V**2	0.0
A3[1]	Cubic fit ids equation coefficient	A/V**3	0.0
BETA	Coefficient for pinch-off change with respect to vds	1/V	0.0
GAMMA	Hyperbolic tangent function parameter	1/V	0.0
RDSO	Fix drain to source resistance at VDSDC	ohm	infinity
VDSDC	VDS bias point where RDSO, CGD, CGS and CDS are measured		
VDSO	VDS at which A0,A1,A2,A3 were evaluated	V	0.0
VTO	If specified, IDS is set to zero for Vgs less than VTO.	V	0.0
	**MODEL=2.5 Parameter Subset**		
ALPHA	Hyperbolic tangent function parameter	1/V	0.0
BETA[1]	Transconductance parameter	A/V**2	0.0
LAMBDA	Channel length modulation parameter	1/V	0.0
THETA	Transconductance parameter for large Vgs	1/V	0.0
VTO	Threshold voltage	V	-2.0

[1]Parameter value is scaled with AREA.

VS_Dxxx   **DC Voltage Source**   **VS_Dxxx**

Symbol:
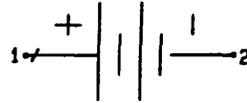
Syntax:

> *SOURCE*
>   *netname VS_Dxxx   n1   n2   DC=x1*

Parameters:

netname	=	the name of the main (last) network in the CKT block
_Dxxx	=	required identifier tag
DC	=	value of dc voltage in DIM block voltage units

Netlist Example:

> SOURCE
>   AMP   VS_D19   20   0   DC= –0.15

ACADEMY/jOMEGA Notes:

None

VS_Dxxx	**DC Voltage Source**	**VS_Dxxx**

Element Type: Source
DC voltage source

Model Basis: Ideal
Originator -- EEsof

Range of Usage:

Libra only

Notes/Equations/References:

ACADEMY name is DCVS. The _D is required.

VS_D must be located in the SOURCE block of circuit file.