TRANSISTORISED PILOT-WIRE FEEDER PROTECTION

ASSOCIATED WITH IRONLESS-CORE CURRENT

TRANSFORMERS

A THESIS SUBMITTED

TO

THE VICTORIAL UNIVERSITY OF MANCHESTER

FOR

THE DEGREE OF DOCTOR OF PHILOSOPHY

BY

EMAD EL-SHARKAWI, B.Sc.

January, 1964

ProQuest Number: 11004494

ProQuest 11004494

SUMMARY

Pilot-wire protection and its applications have been the topic of a good deal of discussion and research recently. It seems, however, that the demand for protecting longer lines and for decreased operating times extends present techniques beyond their limit of applications. Most of the present available pilot-wire schemes operating on G.P.O. circuits are dependent on the pilot-wire circuit, i.e. their overall characteristics are unpredictable.

Ideally, pilot-wire protection schemes should be independent of the pilot-circuit.

A sophisticated pilot-wire scheme using narrow-angle phase-comparison techniques, similar to those used in carrier protection, has been developed in the work described in this thesis.

This work falls into five broad sections. The first deals with the advantages and the future of a new pilot-wire scheme.

The second discusses the analysis of single relaying quantities for feeder protection.

The third describes the design, analysis and testing of segregating circuits associated with ironless-core C.T.s for extracting relaying quantities.

The fourth and the fifth section deal with artificial pilot circuits as well as the design, construction and experimental work carried out on the developed scheme.

In order to protect longer distribution feeders, it is nowadays increasingly realised that developing protection schemes, as the one described in this work, is economically justified.

ERRATA

Page	Line	Error Reading	Correction To Read
42	9	Section (8.5)	Section (8.6)
47	18	be	by
50	13	flux in	flux ϕ in
52	4	eqn (3.3)	eqn (3.4)
	7	is is	it is
62	24	earch	earth
74	19	$(3n + 1)$	$(3n + 3)$
77	13	eqn (4.24)	eqn (4.34)
94	3	$\dfrac{V}{Z_1} \cdot \dfrac{1}{1 + 2K}$	$-\dfrac{V}{Z_1} \cdot \dfrac{1}{1 + 1K}$
97	3	by eqns (5.1)	by (b & c) eqns (5.1)
104	6	eqns (5.13)	eqns (5.15)
111	5	.... evaluates, for $N = \pm 1$, expresses...	...., evaluated for $N = \pm 1$, expressed...
113	3	Exp (4)	Exp (5)
131	3	$\dfrac{(1 - a^2)^2}{\sqrt{3}}$	$\dfrac{(1 - a^2)^2}{3}$
136	5	for for	for
141	7	Fig. (6.3)	Fig. (6.2)
153	10	$a^2\, B_B$	$a^2\, V_D$
158	12	Fig. (6.9D)	Fig. (6.9C)

Page	Line	Error Reading	Correction To Read
165	6	n/R^2 ....)	$n(R^2$ ....)
166	23	Fig. (6.7D)	Fig. (6.7C)
179	1	... $\underline{/\phi_R}$ $V_{o.c.}$	... $\underline{/\phi_R} \simeq V_{o.c.}$
182	4	eqns (6.45, ...	eqns (6.54, ...
194	8	$Z_{s.c.}(1)/Z_{s.c.}(2)$	$Z_{o.c.}(2)/Z_{s.c.}(2)$
196	5	constant " "	constant "γ"
223	5	$\dfrac{-V_{cc}(R_5)}{(R_5 + R_6)}$ V_d	$\dfrac{-V_{cc}(R_5)}{(R_5 + R_6)} \leqslant V_d$
238	1 & 2	T_3	T_2
269	5	anxiliary	auxiliary
271	6	Y_x	Y_s

THE WRITER

The writer graduated in 1954 from the Faculty of Engineering, Cairo University. He then joined the Aswan Dam Hydro-Electric Scheme for three years.

After a further two year's special training course with Messrs. A.S.E.A. of Västerås SWEDEN, and Messrs. A. REYROLLE and Co. Ltd. of Hebburn-on-Tyne, he joined King's College, University of Durham, where he obtained a Post-Graduate Diploma in 1960. Later in the same year he joined the Power Systems Laboratory of the Manchester College of Science and Technology, where he was engaged on a number of research topics, the main of which is the work described in this Thesis.

During the last year he has also been engaged as a Demonstrator in the Electrical Engineering Department in this College.

ACKNOWLEDGEMENTS

CONTENTS

INTRODUCTION

In the past, inverse time relays were adequate to protect simple radial feeders and they gave reasonable clearing times.

As a result of the growth of generating stations and their interconnecting networks, such simple schemes became unsatisfactory due to lack of discrimination. The introduction of the early Merz-Price pilot-wire schemes promised a solution to the problem.

Pilot-wire schemes have been applied in recent years to longer high voltage feeders. The increasing length of the protected section has precluded the use of private pilots and introduced telephone type pilots, privately owned or rented circuits from the G.P.O.

The principle of comparing signals derived from the currents at each end of the protected feeder is still unchanged today. Developments have, so far, been mostly concerned with finding suitable and effective methods to carry comparison over pilot circuits which impose limitations, due to their characteristics, on the application of the comparison principle. These developments have been evolving round the concepts of biassed relays and replica impedance.

In general, most modern pilot-wire differential schemes function satisfactorily within their limitations. Unfortunately, their capabilities and limits are not always clear. This is

possibly due to the simple treatment of pilot-circuit in terms of loop resistance and intercore capacitance. Long G.P.O. pilots are actually composed of different conductor size sections and, in effect, have to be treated as more complex four terminal networks.

It appears, however, that with the progress achieved in telephone techniques, the G.P.O. will eventually tend to reduce the size of conductors below their present practice. In such a case protective pilot-wire schemes must be able to operate satisfactorily over increased pilot-circuit resistances.

Present pilot-wire differential schemes have almost reached their limits of application, and as the pilot-wire resistances increase, less current can be carried over the pilot circuit for a given maximum permissible voltage. This consequently requires the development of more sensitive relays. In the same time the capacitive current of the pilot-circuit increases as the pilot-length increases, and this unfortunately tends to override the differential effect principle.

Ideally, pilot-wire protection schemes should, of course, be independent of the pilot-circuit, but this would appear to be an impossible requirement with the present day schemes unless some fundamentally new technique is evolved.

Conventional iron-cored C.T.s, with their defects, have always been a major obstacle in the progress of many types of

protection including pilot-wire. It was also clear from Nellist's work[26] that further improvements in protective relaying depend to a large extent on finding an alternative current transducer. This fact together with successful application of transistors[8][19][20] and semiconductor techniques in power system protection, have opened the way for further development in the field of pilot-wire protection.

A sophisticated pilot-wire scheme using narrow-angle phase-comparison techniques, similar to those used in carrier protection, has been developed in the work described in this thesis. This work is the result of research and development carried out by the author since the time Nellist published his work[26] on ironless-core C.T.s (linear couplers).

The contents of this thesis falls into five broad sections. The first describes the advantages outlined in introducing a new pilot-wire scheme and gives briefly its basic principle, and future applications.

The second, gives a rather detailed analysis of single relaying quantities, derived from three phase currents, for feeder protection and recommends a certain combination of sequence currents for this purpose.

The third, is the design, testing and analysis of segregating networks to be associated with ironless-core C.T.s for the extraction of relaying quantities.

The fourth section deals with the simulation of G.P.O.
pilot-circuits and their associated problems.

The fifth and last section deals with design, construction,
and experimental work carried-out on the developed scheme. This
section contains some general conclusions and recommendations for
further work.

CHAPTER 1

A SURVEY OF MODERN PILOT-WIRE SCHEMES

1.1 Historical Introduction

In the past, inverse time relays were adequate to protect simple radial feeders and gave reasonable fault clearing times.

As a result of the growth of generating stations and their interconnecting networks, higher fault current levels were experienced. Such simple protective schemes became therefore unsatisfactory due to the lack of discrimination. The introduction of the early Merz-Price pilot-wire schemes promised a ready solution to the problem of high speed discriminative protection.

The principle of comparing currents, or voltages derived from these currents at each end of the protected feeder is still unchanged today. Developments have been so far mostly concerned with finding suitable and effective methods to carry comparison over pilot circuits which impose limitations, due to their characteristics, on the application of the comparison principle.

The early Merz-Price scheme Fig. (1.1A), operated over negligibly short pilots, used air gap transformers to provide a linear current/voltage output, and was connected in a voltage opposition arrangement under through fault conditions. The effect of the capacitive current of the pilot circuit was considered by increasing the relay setting. The scheme operated satisfactorily, within its limits,
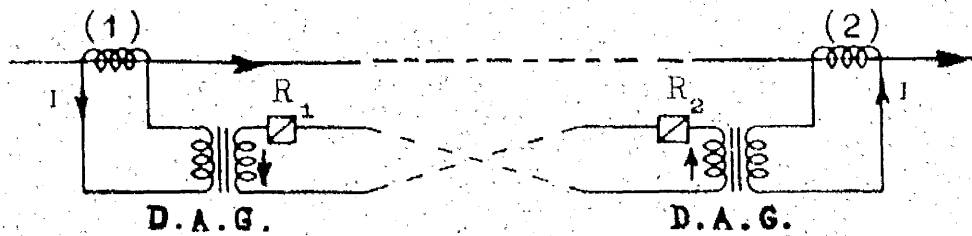
(A) Merz – Price Balanced Scheme.
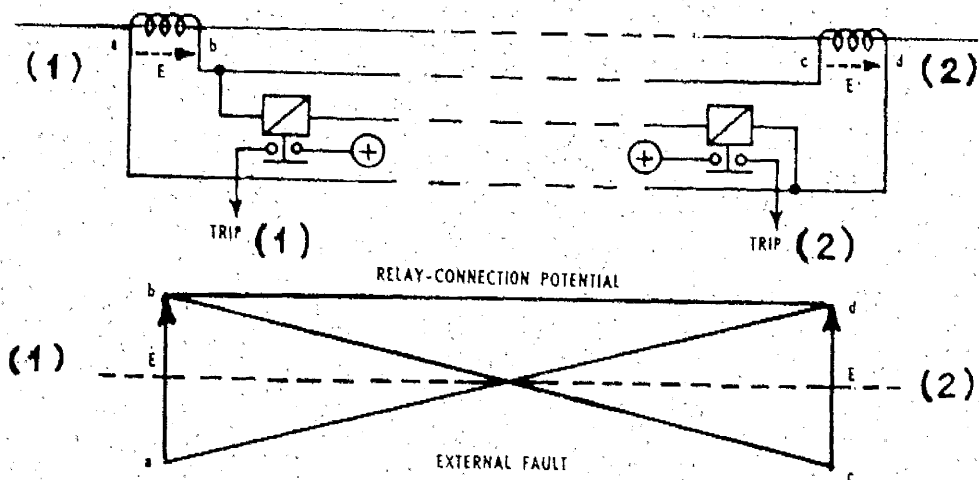
(B) Merz – Price Current Scheme.
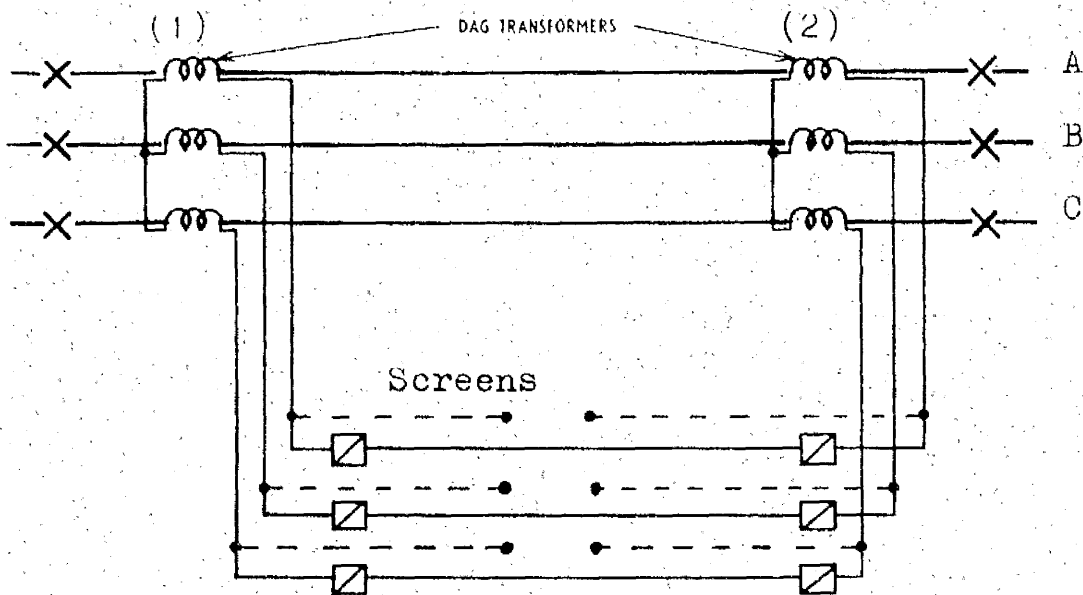
(C) Beard – Hunter Scheme.

FIG. (1.1)

for very short feeders.

The modified Merz-Price circulating current scheme, which overcomes the practical difficulty of inserting the relay at the middle of the protected section by introducing a third pilot wire thus enabling the relays at both ends to be at a zero voltage position on external faults, is shown in Fig. (1.1B). This arrangement reduced also the effect of pilot capacitive current.

Beard-Hunter[1] used screened pilot cables with discontinuous sheath at mid point, to prevent the pilot capacitive current passing into the relay coils. This scheme, Fig. (1.1C), introduced an improvement in setting/stability ratio and was used extensively with reasonable success. The cost of the special pilots cables and D.A.G. transformers made it uneconomical.

Further schemes requiring three core pilots were subsequently introduced mainly to eliminate pilot capacitive currents from the relay coil circuit. The Merz-Hunter split pilot and the self compensated pilot systems are typical of such schemes[1]. In general, all these modified schemes required either special pilot-cable or 3 core pilots and therefore were found to be expensive.

However, it was realised that the capacitive currents of pilots as well as current transformer inequalities, had the greatest effect under heavy external fault conditions. This promoted the idea of employing biassed relays whose pick-up setting increases as the value of through fault current increases.

R_P Pilot Loop Resistance
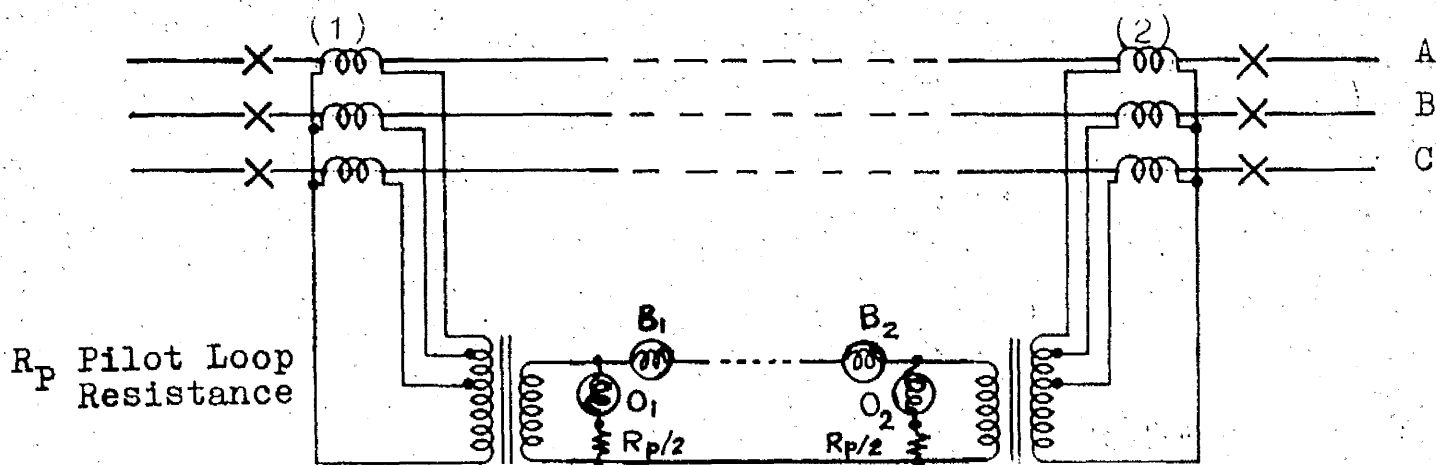
(A) Biassed Relay "Balanced Current" Scheme.

O Relay Operating Coil

B Relay Biasing Coil
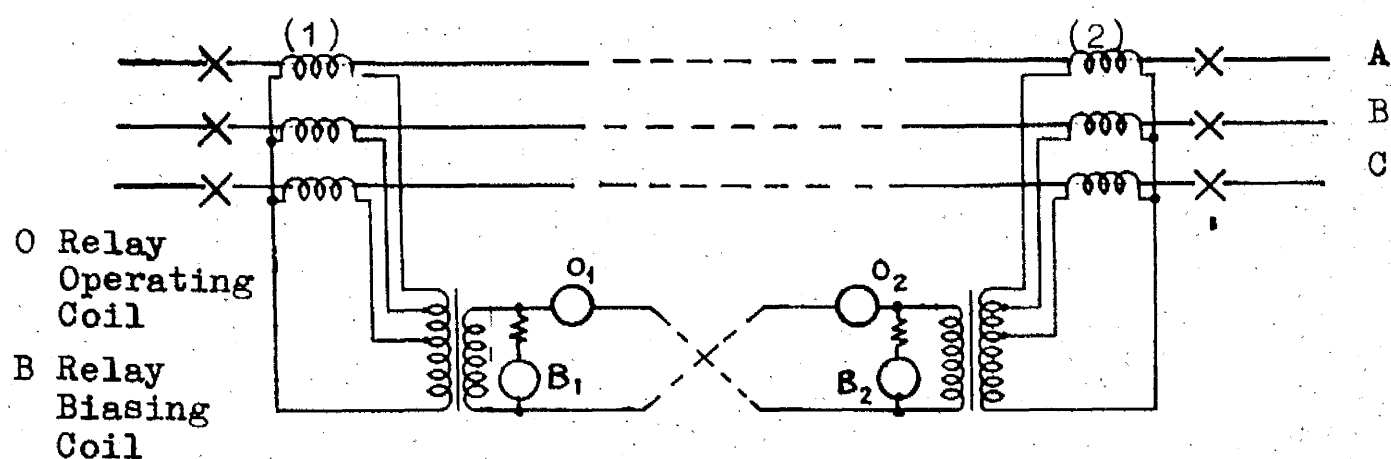
(B) Biassed Relay "Balanced Voltage" Scheme

Rc Pilot Compensating Resistance

(C) Pilot-Wire Scheme Using Replica Impedance

FIG. (1.2) BASIC COMPENSATED SCHEMES.
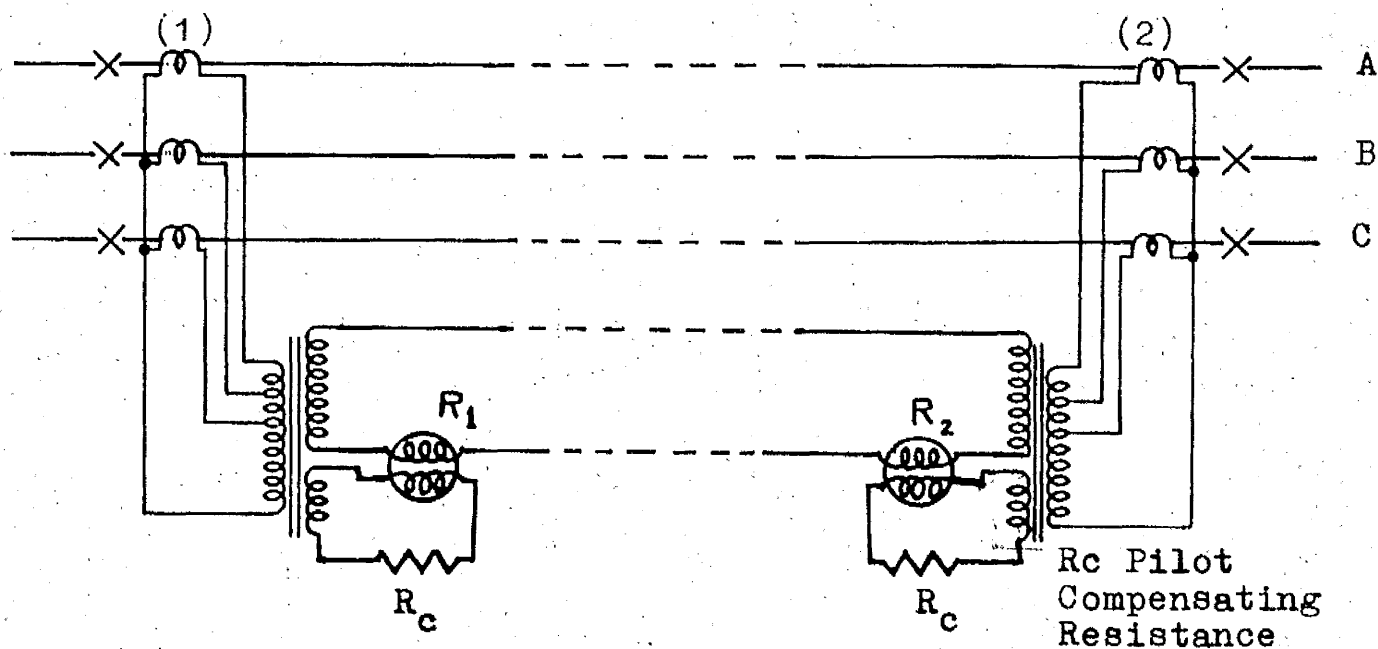
These schemes used two core pilot and were similar to modern schemes in application today, Fig. (1.2A and B). In fact differential protective schemes in common use, both in the U.S.A.[3] and U.K.[10][16], at present differ very little from the basic biassed schemes.

The introduction of the pilot compensation impedance, or replica impedance, was a major step forward in the design of pilot-wire schemes, and a typical scheme is illustrated in Fig. (1.2C). The scheme uses an artifiqial (mimic) impedance having similar characteristics to the pilot-wire circuit and is energised by pilot voltage. The current through it is used to counteract the effect of pilot current, so that the relay operating coil is effectively connected to the electrical mid point of the protected section under external-fault conditions. Early schemes included compensation only for pilot-circuit resistance and they did not give very satisfactory performance.

Most of the modern pilot-wire differential schemes in practice, use either the bias features or replica impedances, or both. It is in the choice of satisfactory bias and/or compensation circuits that progress has been made[10] in providing a protection scheme, which can operate satisfactorily, over any practical lengths of pilot-circuits.

Many methods devised for pilot-wire protection schemes were based on the balanced current principle and two main notable

departures from this approach were D.C. lock-in scheme and the Casson[5] - Last phase comparison scheme.

The former was introduced by Longfield[2][15] and was the first scheme to envisage the use of rented P.O. circuits[2]. The pilot circuits were used only to carry a D.C. signal, i.e. on/off, distinct from a signal representing either the magnitude or the phase of the feeder current. This D.C. signal was used only for blocking associated with a high speed directional relay and a lower speed overcurrent relay at each end of the feeder. Fig.(1.3) shows a schematic illustration of the basic scheme. For external fault conditions one directional relay would indicate the fault power, active or reactive, leaving the protected section and would therefore initiate a D.C. pulse over the pilot circuit to inhibit tripping at both ends by blocking the lower speed o.c. relays. For internal fault conditions neither of the directional relays would indicate outgoing fault power and the o.c. relays would therefore effect tripping at one or both ends where there is fault current infeed. The performance of the scheme was satisfactory but it suffers from the obvious disadvantage of long fault clearing times, since discrimination is provided by time delay.

As a result of further developments, the time delay was reduced to acceptable proportions by a more complicated scheme known as High-Speed D.C. Lock-in System. This system was used extensively with carrier pilot and in a number of cases audio frequency (V.F.)

D Directional Relay
O.C. Over Current Relay
R D.C. Trip Lock-out Relay
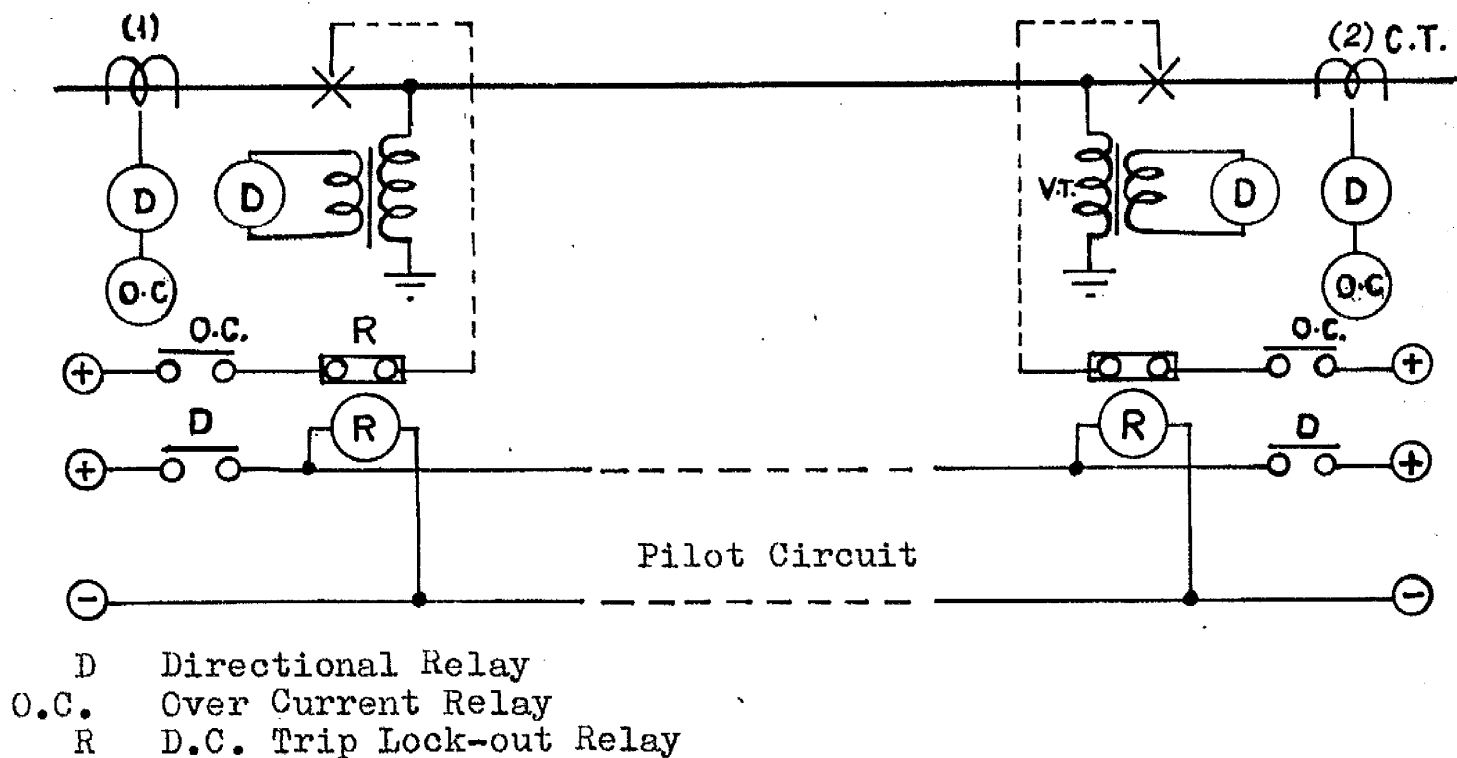
FIG. (1.3) D.C. LOCK-IN PROTECTION (LONGFIELD)

(A) High Speed Fault
  Detecting Relays
(B) H.S. Locking Relay
(T) Tripping Relays

(a) Fundamental Prin-
  ciple shown for
  one Half-Cycle on
  External Fault
(b) Phase Angle
  Characteristics
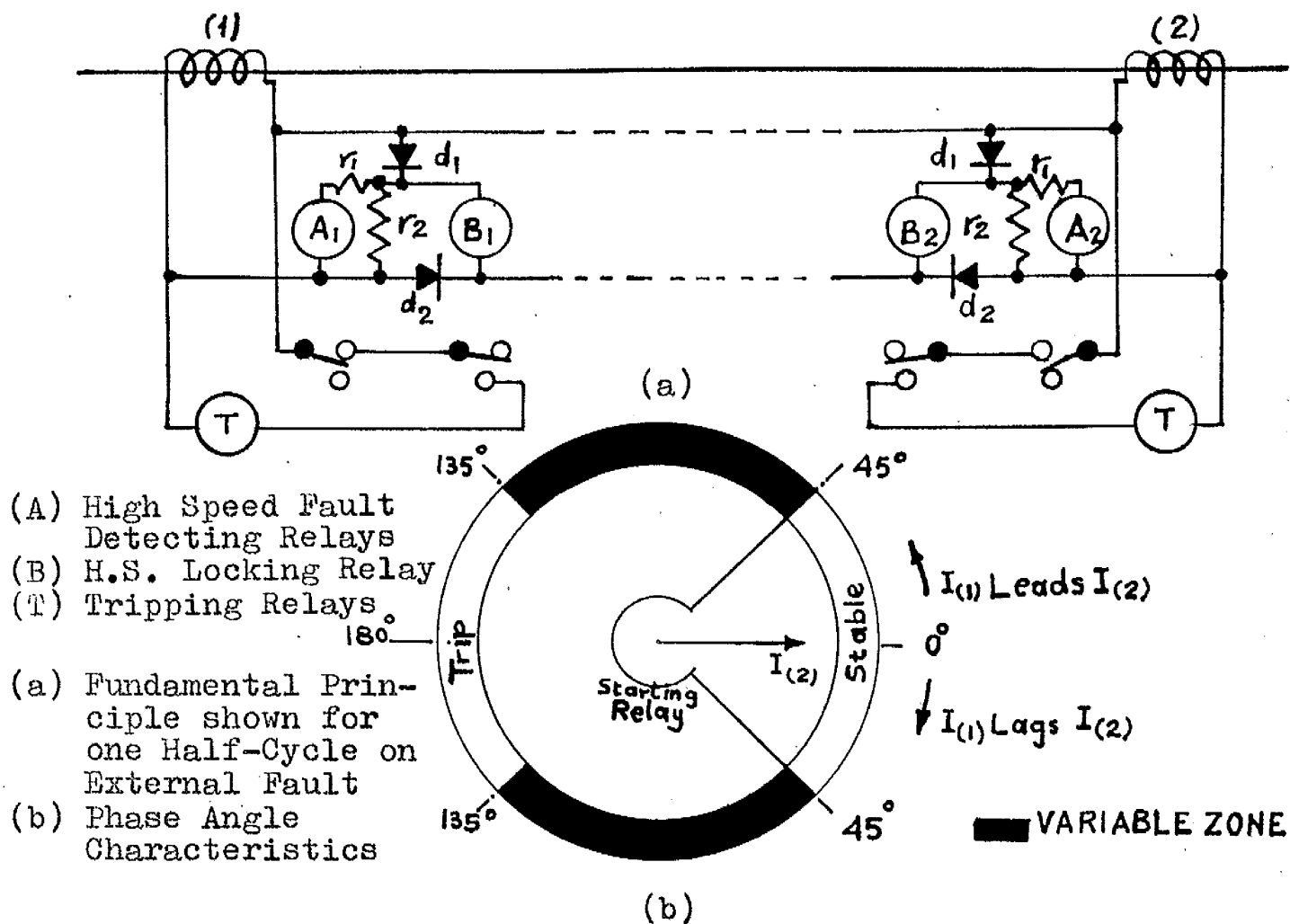
FIG. (1.4) CASSON-LAST SCHEME

or D.C. signalling[4] was used, but with less success, over P.O.
circuits. The over-current starting feature was ultimately replaced
by under-impedance starting and this lead to the idea of providing
D.C. locking impulse to conventional high speed distance protection
in order to reduce last zone clearance time. This method is still
practiced in U.S.A. over carrier pilots. D.C. lock-in schemes
required low set and high set starting features as well as expensive
V.T.s for directional relays. They suffered also from the problems
of directional relay operation under nearby three phase faults.

The outcome of all these schemes was the introduction of
accelerated distance protection by the aid of signals (V.F.) over
pilot circuits. Its basic principle was to initiate a signal (V.F.)
in the pilot circuits when tripping takes place at one end of the
protected section. This signal, on receipt at the remote end,
is arranged to operate an auxiliary relay which in turn short
circuits the time delay contacts of the last zone of the Distance
Scheme. This arrangement has therefore instantly changed the reach
to zone 3.

Such scheme has been successfully operating on feeders,
particularly on teed feeders,[15] and has many advantages, not the least
of which is that a pilot failure does not produce serious consequences.
It is envisaged that its main application will be for long feeders
where present conventional differential schemes may get into
difficulties.

Another method which was a major attempt to deviate from the differential principle was introduced in 1947 by Casson and Last[5]. The basic principle of this scheme is to compare the direction of each half-wave of current with the direction of the half-wave received from the other end of the protected section via the pilot circuit. This scheme was introduced at a time when P.O. pilot circuits were considered unsuitable for differential protection schemes and were used only for lock-in protection purposes.

The Casson-Last scheme guided the thought away from the use of voltage transformers and directional relays to the method of current phase comparison at the two ends of the protected section. In this respect it introduced the present field of longitudenal differential protection over rented G.P.O. pilot circuits. Fig. (1.4A) illustrates the principles of the practical scheme.

Under external fault conditions the secondary currents of the C.T.s are approximately 180° out of phase, so that on one half cycle relay A_1 is operated from the C.T. at end (1) simultaneously with relays B_2 and B_1 in parallel from the C.T. at end (2).

Relay A_2 remains inoperative. Under these conditions no tripping will occur. On the next half cycle the reverse will take place, A_2 and B_2 operating together while B_1 operates alone and again no tripping takes place.

Alternatively for internal faults fed from both ends, on the first half cycle A_1 and A_2 operate simultaneously while B_1

and B_2 remain inoperative. This will result in an impulse given to the tripping relay for a half cycle. On the second half cycle B_1 and B_2 will operate without effect while A_1 and A_2 are inoperative. The tripping relay will therefore be energised on alternate half-cycles.

The series resistor r_1 is equivalent to the pilot loop resistance and resistor r_2 is equal to the resistance of one relay coil. The current setting of relays B_1 and B_2 is lower than relays A_1 and A_2 to provide a low set and high set feature, i.e. to ensure overlap feature.

The scheme, in practice, had unfortunate history because of the unsatisfactory performance of the ultra high speed relays. Difficulties arouse particularly in designing and adjusting the relays so that they would respond to instantaneous reversals of direction at the inception and clearing of faults. Considerable improvement was obtained by the introduction of a slugged telephone type trip auxiliary relay and no doubt improvement would have resulted from the use of Carpenter relay elements.

The principle of the scheme is used in phase comparison carrier relaying but, to the Author's knowledge, is not used nowadays with pilot channels. It was tried in Germany and the U.K.[17] for some years but was not considered practical because of the difficulties mentioned before.

The indefinite performance of the scheme can be seen from the

polar diagram Fig. (1.4B) of the tripping phase angle characteristics.

The scheme was designed to operate over G.P.O. pilot circuits having

a loop resistance of about 2.0 K ohm and intercore capacitance not

more than 2.0 μF. The demand for operation over longer G.P.O.

circuits, together with the unfortunate history of this scheme,

contributed in accelerating the development of the biassed

differential schemes.

1.2 General Considerations for Modern Pilot-Wire Schemes

The historical introduction attempted very briefly to trace

the development from the early Merz-Price scheme to the conceptions

of bias, replica, D.C. or (V.F.) signalling type, and was concluded

with the Casson-Last scheme[5].

A great many pilot-wire schemes for private pilots have been

developed over the years, many of which are similar in principle

if not in detail. Most of these schemes are operating over

7/.029" pilots with a maximum loop resistance of about 800 - 1000 Ω.

These schemes are not given much attention in this work, but are

only mentioned when appropriate. Private pilot-schemes are often

uneconomical for protection of feeder sections[14] of about 25 miles

and over. It is therefore economical to rent pilot circuits from

telephone companies (G.P.O.) for feeders longer than 25 miles where

the cost of distance or carrier protection may not be justifiable.

However it is felt that with the introduction of a super-grid of

400 K.V. in the U.K.[12], many of the lower voltage feeders, in particular 132 K.V. grid, would be merely for distribution purposes, rather than for trunk transmission. This may add another factor not to justify, in principle, distance or carrier protection for these distribution networks.

All these reasons combined together give a greater demand for the development of pilot-wire protection schemes, including the one described in this thesis, suitable for use over G.P.O. rented circuits. Such schemes are more attractive economically than carrier or distance protections on lines of 30 - 40 miles in length. For shorter lines they have also some economic advantages over private pilot-schemes unless a suitable pilot is readily available at low cost.

With the use of G.P.O. rented circuits, additional difficulties exist due to G.P.O. limitations with regard to the maximum permissible voltage and current levels which may be applied to their pilot circuits. In addition, inductive loading coils, to facilitate speech, are often included in G.P.O. circuits which add to the difficulties.

In general, G.P.O. rented circuits are by no means as reliable as private pilot circuits, and in modern protection schemes it is essential to use continuous supervision of pilot circuits. G.P.O. pilot circuits are discussed in more detail in Chapter (7).

These pilot circuits introduce also special problems in the

designing of relaying schemes due to voltage and current limitations,
i.e. limiting the power which can be transmitted, and consequently
reducing the power available for relay operation. Voltage limiting
networks are used as a normal practice and thus greater power is
made available to the relay at setting.

Schemes involving voltage limiters tend, at high current levels,
to become insensitive to amplitude differences between the currents
at the two ends of the protected feeder and can only then operate
on phase difference (i.e. phase comparison).

There are some common features to all pilot-wire schemes
operating over G.P.O. circuits. Most of these features were
introduced to overcome some of the special problems experienced
with the use of G.P.O. rented pilots. The two main features
introduced are pilot supervision equipment and starting relay
arrangement.

1.2.1 Pilot Supervision Equipment

A healthy pilot circuit is essential in a pilot-wire scheme
for correct discrimination. Private pilot circuits of 7/.029 type
are not usually provided with continuous supervision although they
are not completely without fault incidence, at least due to
interference as a result of human activities.

When G.P.O. circuits are used for protection purposes,
continuous supervision is considered essential. Fitting of

"Priority" coloured links on these circuits, by the G.P.O., help to minimise interference. However, interference cannot be completely avoided during fault locations or field testing by G.P.O. personnel. Testing voltages may be applied during maintenance of adjacent circuits.

Pilot supervision equipment is arranged to give a time delayed alarm in the event of pilot failure and fault detector relays (starting relays) ensure that pilot failure does not result in circuit breaker tripping under normal load condition. A through fault coinciding with a pilot failure will produce maloperation, but this is not considered a serious risk.

Most pilot supervision schemes are basically similar. Fig. (1.5) shows two typical cases of these arrangements.

The supervision method usually consists of circulating a small direct current, between 0.5 to 5 mA, around the pilot loop. A polarised pilot supervision relay, at the remote end, is held continuously operating by this D.C. current. Conditions of short-circuit, open-circuit, and reversal of pilot cores cause the supervision relay to reset and give an alarm. The relay at the sending end gives also an alarm for the failure of supervision supply. The supervision current is generally disconnected during fault conditions to prevent any interference with the main protective scheme. A high degree of D.C. smoothing is required by the G.P.O. to prevent interference with adjacent communication circuits.
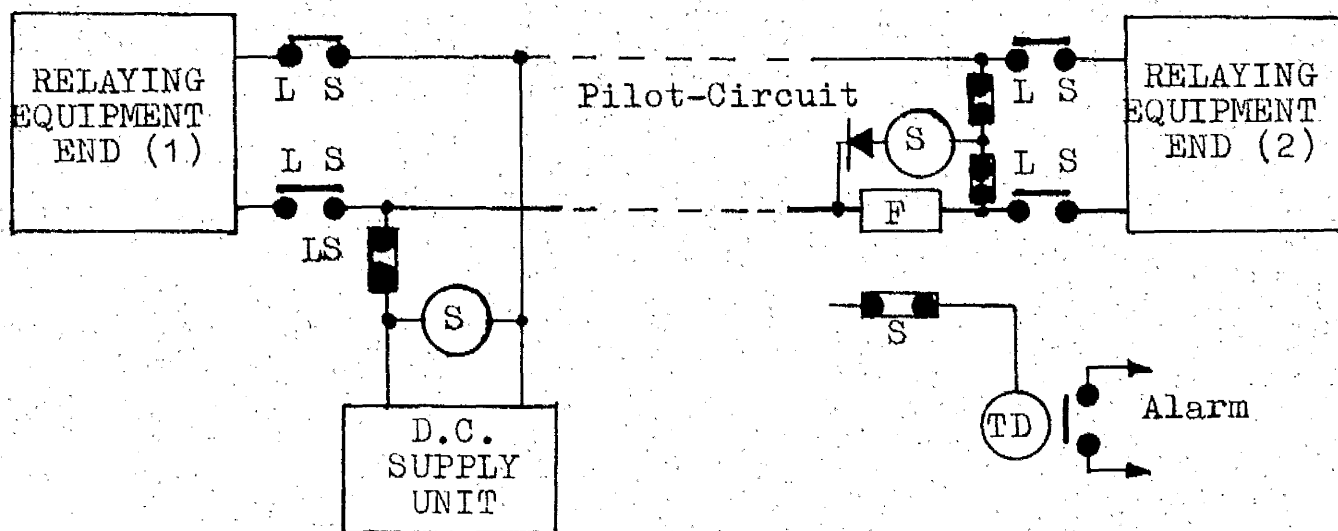
F   50 c/s By-passfilter
LS   Low Set Relay
S   Supervision Relays
TD   Time Delay Relays

(A) Typical Pilot Supervision Scheme with Pilot Switching.

LS₁) Added
LS₂) if
) required
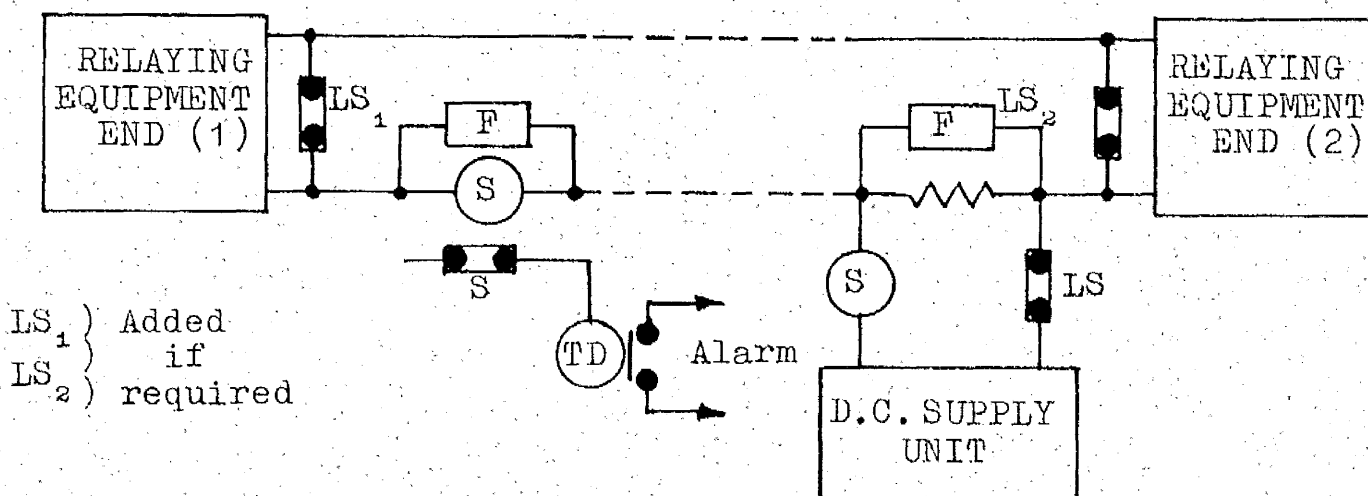
(B) Pilot Supervision Scheme (No Pilot Switching).

FIG. (1.5) PILOT SUPERVISION SCHEMES.

1.2.2 Fault Detectors or Starting Elements

The fault detectors (starting elements) have to fulfil two main requirements when used in conjunction with pilot-wire protective schemes operating over G.P.O. circuits.

(a) To prevent, or rather to eliminate, the possibility of circuit breaker tripping for pilot circuit failures or faults arising from G.P.O. interference. This is usually achieved by arranging for the starting relay contacts to short circuit the main relay operating coil circuit and to control tripping.

(b) The pilot supervisory current should be interrupted before the main protection is brought into operation. This facility is also provided by the starting relay.

Fault detecting elements (starting relays) may respond to overcurrents, negative sequence currents or their rate of change. Generally, where fault settings are greater than maximum loads, as in 3 phase and 2 phase faults, starting feature is provided by two overcurrent and one earth fault elements.

In cases where settings less than maximum loads are encountered on the system, a rate of change element provides starting, phase unbalance or negative sequence current, for phase faults.

1.3 Present Schemes for use over G.P.O. Pilots

In the present section a survey of commercially available schemes is given, with elementary details of operating principles, and also some general criticism.

1.3.1 A.E.I. DSC Protection

This protective scheme uses the opposed voltage principle together with amplitude comparator relays having separate coils energised from separate metal rectifier bridges. This equipment was first installed in 1953.

The basic arrangement is shown schematically in Fig. (1.6). The summation current transformer secondary winding energises a voltage limiting network composed of a resistor/Metrosil (non-linear resistance) parallel combination.

The inherent discrimination available over G.P.O. pilot circuits is limited by their large series loop impedance and the high shunt admittance normally encountered on such circuits. This scheme uses a shunt reactor across the pilot circuit at each end to compensate for (tune) about half the pilot capacitance. Adequate discriminating factor is achieved by the use of tapped pilot tuning choke and the bias resistor setting which is adjustable.

Three starting relays are used, as shown in Fig. (1.6), two connected in the phases and the third in the residual circuit of the C.T.s. The starting relays contacts short circuit the relay
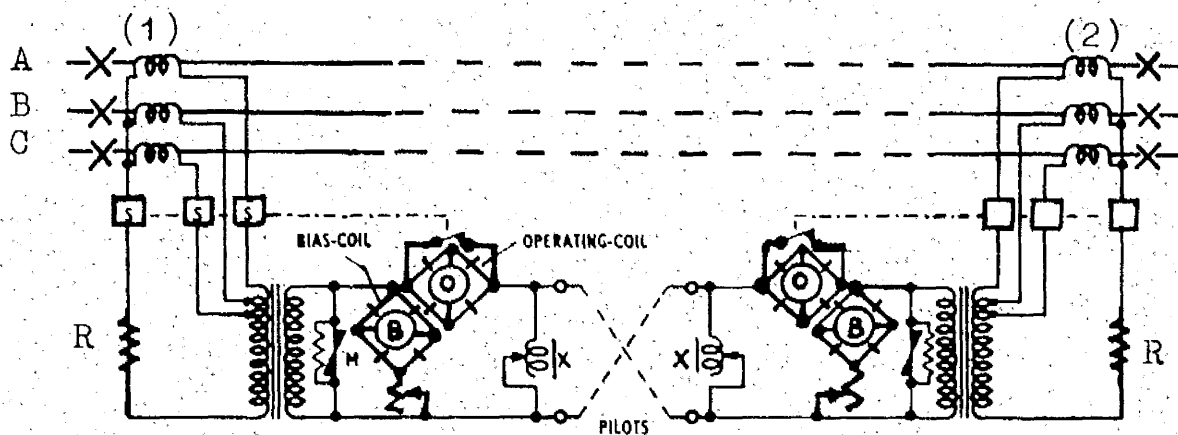
O   Operating Coil
B   Restraining Coil (Bias)
M   Non-Linear Resistor
    (Metrosil)
X   Pilot Tuning Reactor
R   Stabilising Resistor

FIG. (1.6) A.E.I. (DSC) OPPOSED VOLTAGE SCHEME.

operating coil and control tripping.

Comparison over the pilot circuit is continuous but measurement is only carried out during fault conditions, (i.e. when starting relays operate).

Alternative schemes are available using switched pilots, i.e. the pilot circuits are normally free for telephone or supervisory use and are connected to the protective system only under fault conditions.

Pilot supervision is invariably included although it is not shown in Fig. (1.6).

The relay depends entirely upon the settings of the pilot tuning choke and the bias setting resistor for correct operation, particularly on long pilot circuits.

The pilot circuit is not necessarily symmetrical and the tuning reactor may require different settings at each end. High "Q" chokes may introduce system frequency variations as well as severe subsidence transients. Where pilot voltage limiters are also used the compensation effect of the choke is further impaired by harmonics of the pilot voltage waveform, since compensation is only effective at fundamental frequency. All the above causes contribute to impair the discriminating factor of the scheme.

When this scheme was first designed very little was known about the characteristics of the G.P.O. circuits and design specification merely quote 3500 ohms pilot loop resistance and a core/core

capacitance of 2.5 µF.

A recent version of this scheme contains a second harmonic filter unit connected across the bias circuit resistor. This has been included particularly for transformer feeder applications to provide an additional bias under transformer magnetising inrush current during switching operations. Tests carried out on this scheme[10][15] over an actual unsymmetrically loaded G.P.O. circuit of 2750 ohms, have shown that the best obtainable discriminating factor was 4:1. It would therefore seem unwise to extend the use of such schemes on longer pilot circuits.

1.3.2 High Resistance Pilot Wire Protection (Reyrolle)

This scheme[16], referred to occasionally as half-wave comparison scheme[17], uses the series voltage principle with parallel connected relays. Rectifiers are connected in series with the pilot circuit to give an artificial mid-point connection for the relays on alternate half cycles. The basic connections of the scheme are shown in Fig. (1.7A).

At each end the pilot loop contains a half-wave rectifier, shunted by a resistance R_A , so arranged that their conducting directions are in opposition. The relays are connected across the pilot-circuit terminals each in series with another half-wave rectifier.

Fig. (1.7B) shows the condition of an external fault for
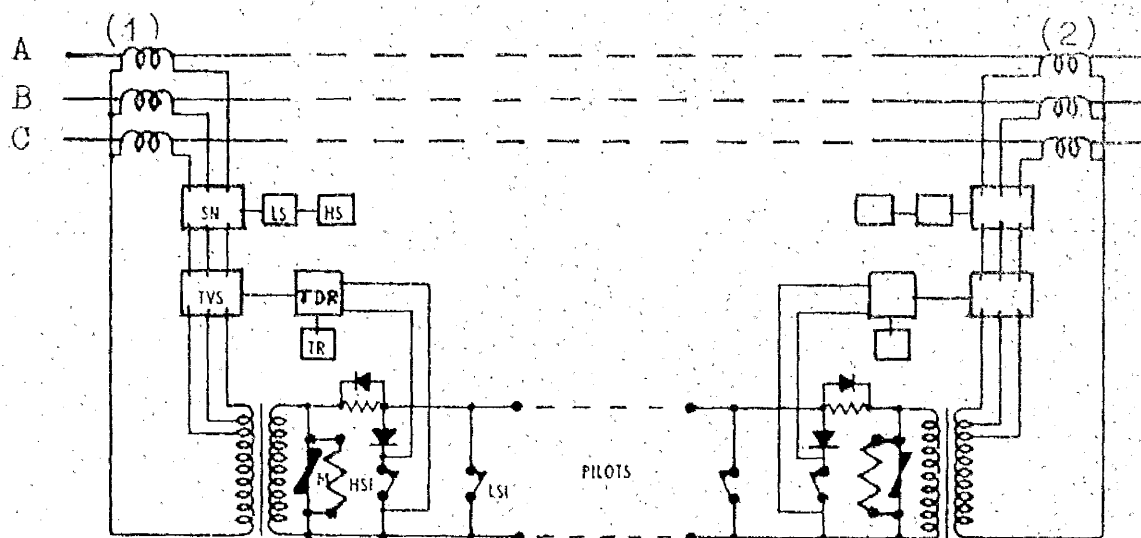
HS. —High-set starting-relay
LS.—Low-set starting-relay.
SN.—Starting network.
TDR—Transductor.
TR.—Trip-relay.
TVS.—Transductor voltage
    supply.

(A) SCHEMATIC DIAGRAM.

1st half-cycle (B) EXTERNAL FAULTS. 2nd half-cycle

1st half-cycle (C) INTERNAL FAULTS. 2nd half-cycle
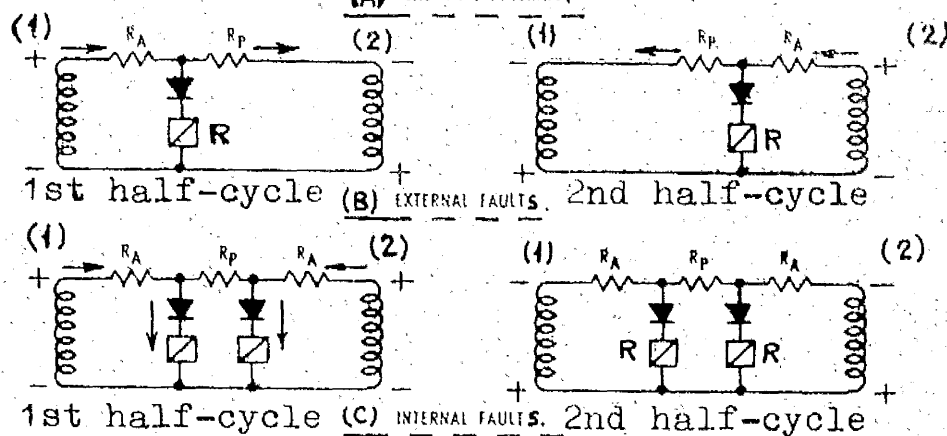
FIG. (1.7) High Resistance Pilot-Wire Scheme. (REYROLLE)

both half cycles of current. It is seen from the figure that if $R_A = R_p$ then the equipotential point alternates between the two ends, each relay R being at the electrical mid-point on alternate half cycles. The rectifier in series with the relay circuit prevents current flowing when the relay is not at the electrical mid-point.

In practice, the resistor R_A is chosen to be greater than the pilot loop resistance so that both relays R are polarised by reverse voltage for both half cycles on external faults. This, in effect, provides the relay with a bias feature by displacing its connection beyond the mid point, in the stable direction.

It is claimed that the pilot replica impedance R_A may be a pure resistor, no capacitance required, because of the uni-directional nature of the pilot voltage, on external faults, which reduces the effects of pilot capacitance currents.

Under internal fault conditions, only the relay at the fault-feeding end is energised. The relay current is unidirectional being a half-wave rectified and is therefore used as control current of a transductor type relay, which obtains its polarising constant voltage supply through a network energised by the secondary fault current.

Another additional half-wave rectifier is connected across each relay coil to perpetuate the coil current during the dead half cycle.

The starting equipment consists of three identical transformers the outputs of which are connected to three rectifiers, the outputs of which in turn are paralleled and connected to the coils of two starting relays in series, low set and high set.

On the occurrence of a fault, contacts of the low set are opened thus removing the short-circuit across the pilots as well as interrupting the supervisory current. At the same time, the high set contact is opened which removes a short circuit from the control winding of the transductor relay. A conventional pilot supervision arrangement (not shown in the diagram) is also included.

The scheme is suitable for pilot circuits of up to 3500 ohms loop resistance and a pilot core capacitance up to about 2.0 µF.

Simple tests carried on this scheme[10][15] gave adequate discriminating factors for pilots up to 3600 ohm loop resistance, but for longer circuits the available discriminating margin is greatly reduced to something in the range of 2 - 5 for a pilot-loop resistance of about 5000 Ω.

It is clear, from the description of operation, of this scheme that the ultimate length of pilot permissible is probably restricted by the basic principle rather than inherent sensitivity of relay elements.

It has been mentioned in section (1.2), that schemes involving voltage limiters tend to operate on phase comparison principles over most of its working range. The scheme under consideration

is one of this type, and it is therefore essential to examine the basic characteristics with particular reference to phase angle response. Reference to the manufacturers confirmed that such characteristics have not been recorded.

It was not until very recently* that such tests were carried out over G.P.O. circuits. From the study of the results it is apparent that this scheme has a very low tripping angle, with short pilots, of about 10°. It is also apparent that the tripping phase angle of the scheme is seriously unsymmetrical, having an angle as high, in the lagging direction, as 90° and over.

Such schemes would give sequential tripping under fault conditions which might limit its use in cases where automatic high speed reclosing is practised. However, the scheme is suitable for many less important feeders, within its limitations of 3500 Ω pilot resistance and 2.0 μF core capacitance, as long as care is taken in setting-up the scheme so that adequate phase comparison angle is obtained particularly with short pilots.

1.3.3 Bridge Comparator Scheme Using Replica Impedance

The scheme was developed in 1954 by C.E.G.B.[10] South Wales Division. The basic principles, of the latest version, of this scheme are shown in Fig. (1.8)

---

* Private correspondence with Mr. J. Rushton of C.E.G.B., South Western Region.
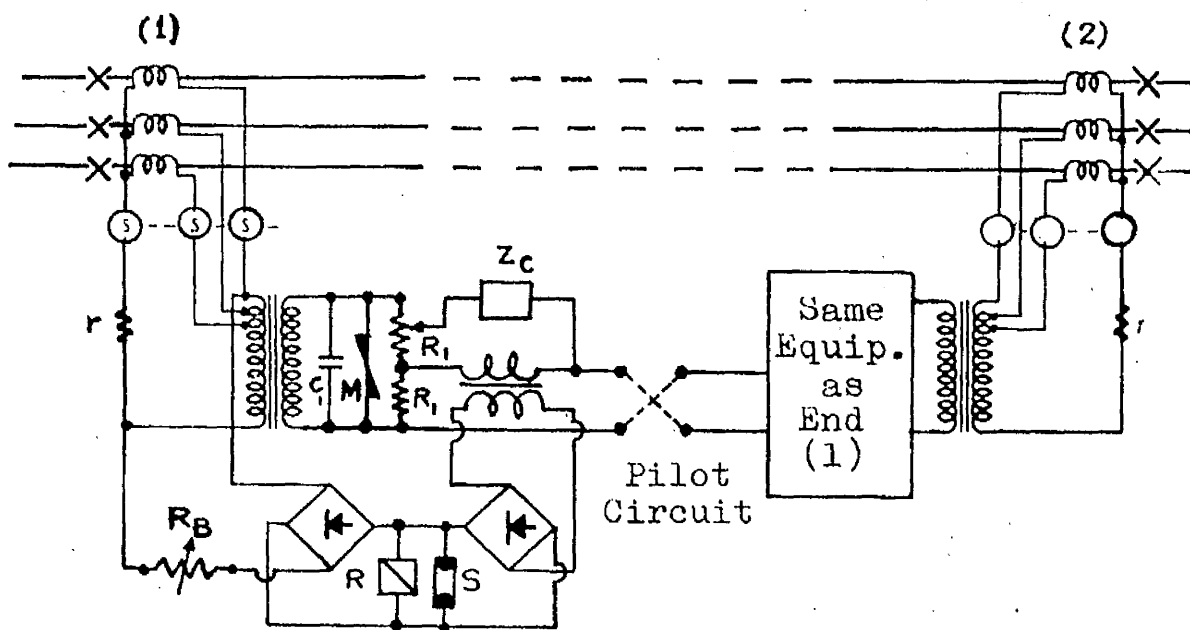
S   Starting Relays

Z_c Pilot Replica Imped.

R   Differential Relay

M   Non-Linear Resist.

FIG. (1.8)   BRIDGE COMPARATOR SCHEME USING
              REPLICA IMPEDANCE COMPENSATION.

The scheme uses the opposed voltage principle and a pilot replica impedance for compensation. The replica impedance Z_C is energised by a voltage equal and of opposite polarity to the pilot voltage and the current drawn through the replica Z_C is therefore equal and opposite to the pilot circuit current under external faults (healthy conditions).

The operating rectifier bridge of the differential relay R is connected in series with the pilot wires, and thereby carries a current proportional to the out of balance current between the two ends of the feeder. A bias feature is also provided to ensure stability under external faults by causing a current to flow in the relay in a restraining direction. This bias current is supplied from a rectifier bridge connected across the input side of the summation current transformer.

A voltage limiting circuit, composed of a non-linear resistor/condenser combination, is connected across the secondary of the summation transformer.

Compensation for G.P.O. pilot circuits is provided by the replica impedance Z_C which is composed of a resistor and a capacitor connected in series. The magnitude of the voltage applied to this compensating network is made adjustable, as well as the series resistor of the compensating circuit itself. This arrangement provides continuous variable adjustment using fixed values of the compensating circuit capacitor.

Instantaneous starting relays are used to control the protection and to prevent inadvertent tripping due to pilot failures. The starting relays permit the differential relay to operate and control tripping.

The relay circuit itself comprised two rectifier bridges connected in a circulating current circuit with the differential relay, (plain amplitude comparator), connected across equipotential points.

Under external fault conditions the bias current will exceed the operating current and the relay will be restrained from operating. On the other hand an internal fault will reverse this condition and the relay current flows in the operating direction.

It is possible to provide an acceptor circuit, not shown in diagram, composed of a condenser/choke tuned to 100 c/s, connected across the bias resistor R_B . This circuit exerts negligible effect on the restraining current at fundamental or odd harmonics frequencies.

Under transformer magnetising current inrush conditions where a predominating 2nd harmonic content is present, the circuit provides an additional restraining current feature by shunting R_B. This feature is advantageous where the scheme is applied to rather short transformer/feeder circuits.

A conventional form of pilot supervision equipment, not shown in Fig. (1.8), is also incorporated.

Testing results on G.P.O. circuits show that the scheme
operates satisfactorily over pilot circuits up to 6000 ohms loop
resistance and gives symmetrical tripping characteristic.

However, it is felt that this scheme has been developed
over the years as a result of long field experiences. It is also
the only scheme which has been thoroughly tested on mixed G.P.O.
circuits and provides a practical approach as far as commissioning
procedures are concerned.

This scheme, like most others, uses voltage limiting circuits,
with a result of a pilot voltage waveshape being completely
different from sinusoidal over most of the working range. The
setting of the bias and the pilot compensating impedance are
generally carried out under the linear part of the limiting circuit
characteristics, i.e. with sinusoidal voltages. For an
unsymmetrical pilot circuit the compensation at the two ends
differs, and consequently different pilot voltages are obtained,
for the same type of fault, at the two ends of the protected
section. The setting would also vary according to the type of
pilot-circuit used. These factors are, in fact, common to all
schemes of this type.

CHAPTER 2

BASIC OPERATING PRINCIPLES OF A

TRANSISTORISED SCHEME ASSOCIATED WITH IRONLESS-CORE C.T.s

2.1 Introduction

Pilot-wire schemes have been applied in recent years to longer high voltage feeders. The increasing length of the protected section has precluded the use of private pilots and introduced telephone type pilots, privately owned or rented circuits from G.P.O. The use of G.P.O. circuits, with their limitations, needed a new design approach to take into account the parameters of the pilot circuits.

In general, most modern pilot-wire schemes function satisfactorily when applied within their capabilities. Unfortunately the limits and capabilities are not always clearly laid. This is possibly due to the simple treatment of pilot-circuits in terms of loop-resistance and intercore capacitance. Long pilots are actually composed of different conductor size sections and therefore, tend, in effect, to be treated as a more complex four terminal network.

The development of modern pilot-wire schemes has been evolving, as given in Chapter (1), round the two basic concepts of replica impedance and biassed relays.

It appears, however, that with increasing improvements in telephone techniques, the G.P.O. will eventually tend to reduce the size of conductors below the present practice. In such a case the

protective schemes must be able to operate satisfactorily over
increased pilot-circuit resistances and a range of 5000 Ω to
8000 Ω does not seem unreasonable.

The introduction of a super-grid of 400 KV in the U.K.[12],
would put other systems of lower voltages, e.g. 132 KV, as merely
for distribution, and consequently carrier or distance protection
for these feeders would not be economically justified. This would
open the field for pilot-wire protection application on longer
feeders than its present limit and consequently over higher pilot
loop resistances.

For circuits where high speed reclosing is envisaged, most
present pilot-wire schemes, given in Chapter (1), require careful
investigation of their characteristics before application. It should
be pointed out that since their characteristics are incalculable and
depend upon pilot-circuit conditions, it is therefore impossible
to predict accurately the scheme characteristics in advance of
commissioning.

Ideally, of course, the pilot-wire scheme characteristics
should be independent of the pilot circuit, but this would appear
to be an impossible requirement with the present day schemes unless
some fundamentally new technique is evolved.

Another interesting practical case for the application of
pilot wire protection schemes on untransposed transmission lines
is mentioned[18]. In this particular case of four parallel circuits,

of untransposed lines, the residual zero-sequence circulating current has reached as high as 4.0% of rated load, due to mutual effects. The setting of relays was then difficult without a reduction in the sensitivity of a combined overcurrent (o.c.)/earth fault protection scheme. This was mainly due to high transformer earthing resistors to comply with P.O. regulations in order to limit the earth current. It was noticed that the occurrence of an earth fault on one circuit would cause the relays of sound circuits to trip due to the increase in the residual current which approached earth fault settings.

The use of pilot-wire protection seems the only solution with current phase-comparison, since the residual circulating current would simply be added to, or subtracted from, the load current without any effects on phase comparison principle.

As a general case for protection of untransposed lines it was recommended[18] that pilot-wire schemes should be studied with preference to other alternatives.

2.2 Basic Approach

From the previous section it is clear that another approach and new techniques should be developed to meet the increase in pilot-wire circuit resistance either to cover longer distances or due to using smaller conductor sizes.

Present pilot-wire differential schemes have almost reached

their limits of application, and as the pilot-wire resistance increases, less current can be carried over the pilot circuit for a given maximum permissible voltage. This consequently leads to the requirement of developing more sensitive relays. Higher sensitivity in the relaying elements could be achieved by amplification.

Unfortunately, the capacitive current of the pilot circuit increases as the pilot length increases and it will tend to override the differential effect principle. The effect of the remote end voltage in decreasing or increasing the relay current will, for long pilot-circuits, undergo a phase shift and under such conditions the minimum differential current will not occur on conditions representing an external fault. It is these phase shifts together with the inherent increasing sensitivity of relay elements which impose practical limitations on differential pilot-wire protection. It has been mentioned, in section (2.1), that ideal pilot-wire scheme characteristics should be independent of the pilot-circuit.

With the successful applications of transistorised circuits[8][19][20] in power system protection and the practical progress obtained in the field of ironless-core C.T.s[21], the way has been opened for further developments. A sophisticated pilot-wire scheme using narrow-angle phase comparator techniques, similar to those used in carrier protection, is envisaged.

2.3 Performance and Design Requirements of the Scheme

Prior to the design of any protective relaying scheme, it is rather important to prepare a guide for the required performance. This should take into account the performance of power system under extremes of internal and external fault conditions and then deciding on a satisfactory relay characteristics to give adequate discrimination.

System behaviour under healthy and faulty conditions should be analysed to determine the most desirable relay characteristics and to select the relaying quantities.

Normal system conditions, including power swing, could be investigated by means of a locus diagram[22] which shows that the overall relay characteristics should include a definite setting associated with a finite stability angle. It is noted that for lines up to 100 miles in length negligible error is involved in using standard capacitive current values (0.36 and 0.94 A/mile of 132 KV and 275 KV lines respectively) in the evaluating of the locus. With underground cables it is also permissible to use quoted charging current figures as a basis for constructing the locus diagram. For a pilot-wire protection scheme this locus diagram gives complete information of relay input quantities since the effect of any attenuation and phase shift in the pilot circuit will be included in the derivation of the overall relay characteristics.

In general, a minimum current setting of about 200-300 A with a stability angle of $\pm 30^{\circ}$ to $\pm 45^{\circ}$, will give good performance even for long cable systems (about 20 miles on 132 KV).

The selection of relaying quantities to provide a reliable output under internal fault conditions would require investigation in the performance of power systems under various fault conditions. This topic is discussed at length in Chapter (4). A combination of phase sequence currents to provide a relaying quantity has been recommended[9]. Further analysis of this combination for phase-comparison schemes is given in Chapter (5).

The summation transformer, as a means of providing single phase output for feeder protection, suffers from "blind spots" and a brief analysis for the summation transformer under various conditions is given also, in some detail, in Chapter (4).

A large number of pilot-wire relaying schemes use sequence currents or voltages derived from the power system. These quantities were generally produced by conventional sequence networks driven from C.T.s. These segregating networks contained large and expensive chokes and high rating resistances. Undue amounts of power are generally dissipated in these segregating networks. Very little can be done, in fact, to economise on cost or space when these networks are fed from conventional C.T.s and are required to operate insensitive relays.

Ironless-core C.T.s, do not produce sufficient output[21]

to operate heavy relays through sequence networks, but where transistorised relaying circuits are involved their output would be sufficient. Chapter (6) deals with the development of these networks for extracting relaying quantities.

From the foregoing requirements it is possible to list some of the desirable design and performance characteristics of the envisaged pilot-wire scheme.

(a) The scheme shall have a small stable zone and wide tripping zone. In general, a stability angle of $\pm 30^{\circ}$ to $\pm 45^{\circ}$ is almost ideal.

(b) Phase comparison should take place at current levels corresponding to maximum through faults, as well as for currents in the load range.

(c) Sequence segregating networks driven from ironless-core C.T.s would provide the relaying quantities.

(d) Transistorised circuits to perform logical and relaying functions.

(e) Starting elements are desirable to eliminate incorrect comparison due to the shunt admittance of the protected section or pilot circuit failures.

(f) The scheme characteristics would be completely independent of the pilot-circuit, if possible.

2.4 General Principles of Operation

In order to develop a scheme to comply with the characteristic requirements, mentioned in the previous section, some basic principles are put forward.

Preliminary investigations were carried-out to exploit the different possible ways for achieving the required performance. Many methods and different arrangements are investigated, but it is decided to adopt only those simple, cheap, and uncomplicated ones.

Simplicity and economy are the two major factors which influenced the design and development of the scheme.

The basic general principles of the scheme are briefly stated as follows:-

(a) Deriving a single relaying quantity from the 3-phase system at each end of the protected section. This output should have a sufficient magnitude under load and all types of fault occurring on the power system.

(b) Simultaneous transfer of information, between the two ends of the protected section, over the pilot circuit as a link.

(c) Compensation for the attenuation and phase shift introduced by the characteristic of the pilot-circuit.

(d) Comparison to be carried locally at each end by transistorised circuits suitable to perform any logic and/or relaying functions.

2.4.1 Preliminary Investigations

The result of many preliminary investigations have influenced to some extent the operating principles of the scheme. It is, however, convenient to state briefly at this stage some of these results before explaining the overall principle of operation of the scheme.

A great deal of thought and investigations were carried out to determine the voltage wave shape to be impressed on the pilot-circuit. Simulated pilot-circuits are used (Chapter 7), and since the scheme to be adopted is mainly of a phase comparison nature, a square wave voltage is the best suitable to apply from transistorised circuits and its recovery at the far end is comparatively easy. Troubles were experienced with half-rectified sine waves, and with sine wave at very small voltages due to attenuation, interference, pick-up —— etc.

At very small voltage levels as those experienced with the output of ironless-core C.T.s, it is ideal to drive a transistor (as a switch) with a small input, or a saturated amplifier, thus giving a voltage output depending only on its collector voltage supply. Using the transistor as a squaring element introduces some inherent problems associated with it. These are dealt with in detail in Chapter (8).

For a phase comparison scheme the effect of error due to attenuation is minimised by squaring the waveform for any

amplitude greater than some value below the minimum signal level,
i.e. the square wave gives a fixed interval in comparison with a
variable interval in case of sinusoidal wave.

This lines up with the fact that most present pilot wire schemes
use some sort of voltage limiters and therefore the pilot voltage is
no longer sinusoidal over most of its working range. Moreover, most
of these limiters have by no means perfect voltage limiting
characteristics. The introduction of a square wave voltage over
the pilot circuit is therefore not unfamiliar to pilot wire protection
schemes.

To achieve the aim of a scheme with characteristics independent
of the pilot wire circuit, the question of sending tripping power over
the pilot was investigated. One of the major limitations for pilot-
wire differential protection is to send enough power over long
pilot circuits, as explained earlier, to operate the differential
relay. This may be overcome by amplification and sensitive relay
elements, however, the scheme characteristic would still be
dependant on the pilot-circuit. Another method has therefore to
be selected to provide the tripping power in order that the scheme
would be independent of the pilot-circuit. The most suitable
alternative is the provision of the tripping power from local
auxiliary supplies.

In such a case the pilot circuit would then act only as a
communication channel between the 2 ends of the protected section.

By approaching the problem from this view point, the pilot length may therefore be considerably increased.

Auxiliary supplies, for providing the tripping power, as well as the power supply for the static transistorised relaying circuitry may on one hand introduce some complications. On the other hand, the frequent maintenance attention required for electro-mechanical relays is no more necessary, or it is greatly reduced, in case of static relays.

2.4.2 Overall Operating Principles

In view of the previous discussion, the basic overall operating principles of the scheme were concluded. It is simpler to design and study the equipment on the basis of a functional block diagram showing only the functional relationships of groups of circuit components. For a complete detailed understanding of the equipment this diagram will be subdivided into a number of main stages according to their functions and a detailed description of the design of each stage is given in Chapter (8).

Fig. (2.1) illustrates the equipment at one end of the protected section.

The three phase outputs $(V_A, V_B$ and $V_C)$ of the ironless core C.T.s (L.C.s) are fed to segregating networks which produce three output voltages proportional to the zero sequence, the positive sequence component, and the third one is proportional to the sum
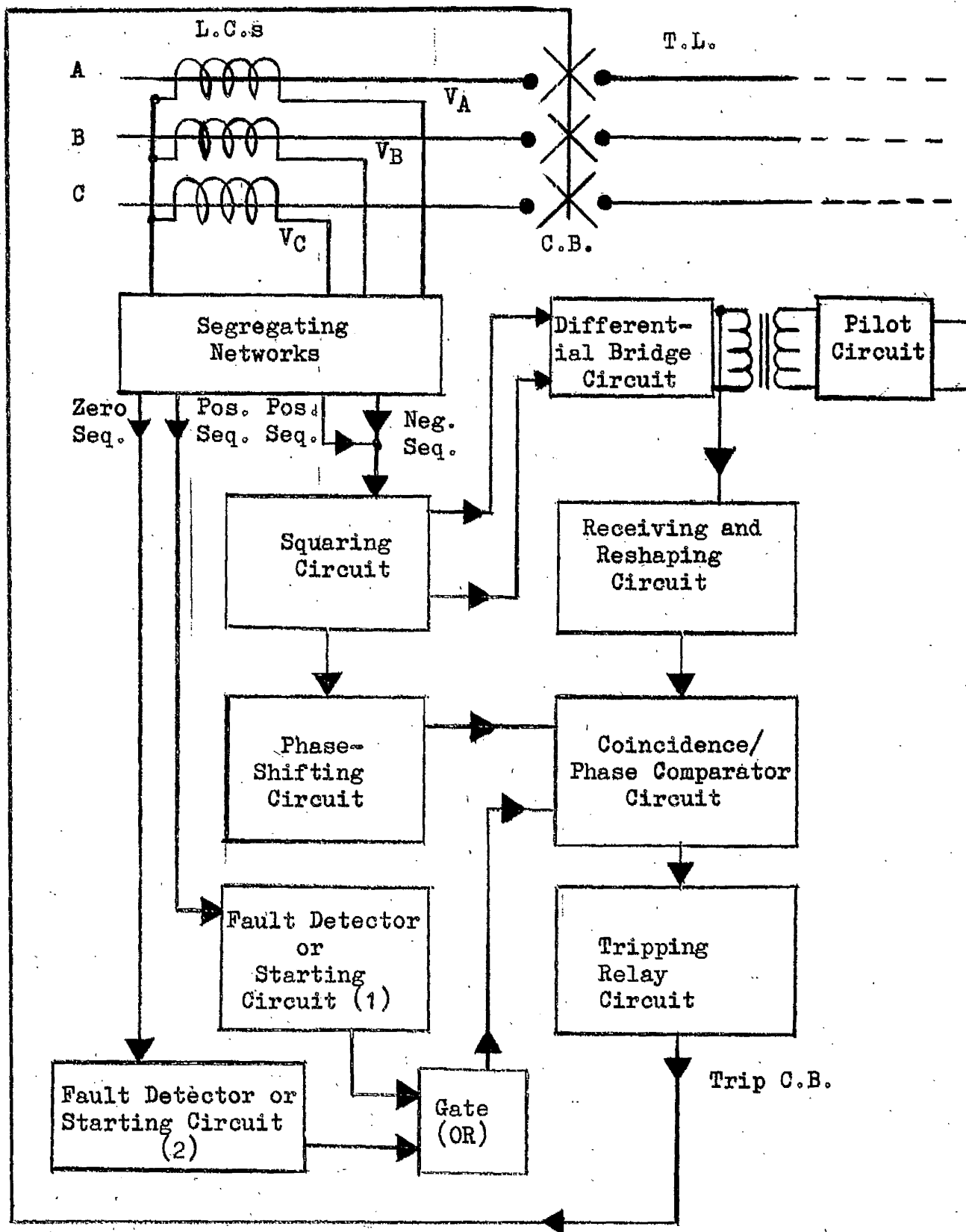
FIG. (2.1).   FUNCTIONAL BLOCK DIAGRAM OF THE SCHEME
(ONE END SHOWN).

of the negative and the positive sequence components of the primary currents. The magnitude and phase of this third output are the main information signals upon which the relaying circuits perform their functions. It will be shown in Chapter (5) that such a relaying quantity will provide adequate representation of the fault current under most primary system fault conditions.

The other two output signals are fed each in turn to a fault detecting (starting) circuit, which responds to the amplitude of the input signal and give a step output when the amplitude reaches a predetermined level. The stepped outputs of the two fault detecting (starting) circuits (1) and (2) are gated (OR) to control the coincidence circuit.

The main relaying signal is fed to a squaring circuit which produces three square-wave voltage outputs, two of which are fed to the differential bridge circuit resulting in a square-wave to be transmitted to the pilot-circuit, while the other output is fed to the phase-shifting circuit.

The phase shifting circuit produces a square-wave output lagging its input by a certain angle equal to pilot circuit phase shift. This is fed to the coincidence/phase comparator circuit in order to be compared with another square-wave derived from a received signal transmitted from the remote end over the pilot circuit. Before this received signal is applied to the phase comparator, it passes through a receiving/reshaping circuit.

It restores to the received signal its square-wave shape, to compensate for the attenuation the signal has undergone over the pilot-circuit.

The phase-comparator produces an output, depending on the phase difference between its inputs, which is fed to the tripping relay circuit provided that the fault detector signal has been previously received.

The tripping relay circuit causes the relay contact to close when the pulse width (in degrees) from the phase comparator has a certain predetermined value. The relay contacts provide the tripping signal to the C.B. In fact a train of pulses 360° apart will be given to the relay until the C.B. opens.

The discrimination between internal and external faults is, therefore, provided by the fact that, for external faults the two square-wave outputs representing the current at the two ends of the protected section, will be of opposite polarity and therefore no pulse is given to the tripping circuit from the phase comparator. However, if the fault is internal the two square-waves are of the same polarity, and provided that the signal from the starting circuit is present, then a pulse (of 180° width) is given to the tripping circuit every cycle, until the C.B. clears the fault. The two terminal equipments will tend then to trip simultaneously.

The fault detectors, which respond to the magnitude of the positive and zero sequence components of the fault current, are used to supervise the operation of the comparison scheme and to

avoid incorrect tripping under pilot failures as well as to eliminate incorrect comparison due to shunt admittance of the protected section.

2.5 Phase-Comparison Scheme Circuits

In the last section the overall principles of operation of the scheme have been discussed and in this section some functional detail of each stage is explained to give a broader understanding of the scheme.

The design details of the transistorised relaying circuits are given in Chapter (8) and that of the segregating networks in Chapter (6).

2.5.1 Fault Detecting (Starting) Circuits

The scheme contains two fault detecting circuits, Fig. (2.1), which are identical in function. They produce a step voltage output, when either of the magnitude of the positive or zero-sequence component of the fault current reaches a predetermined level. These two outputs are fed to a gate (OR) which controls the phase comparator circuit and affects tripping if necessary.

The functional diagram of the different stages of this circuit is shown for one fault detecting arrangement in Fig. (2.2).

Three voltage inputs V_a, V_b and V_c, proportional to the primary current are fed from the ironless-core C.T.s (L.C.s) to
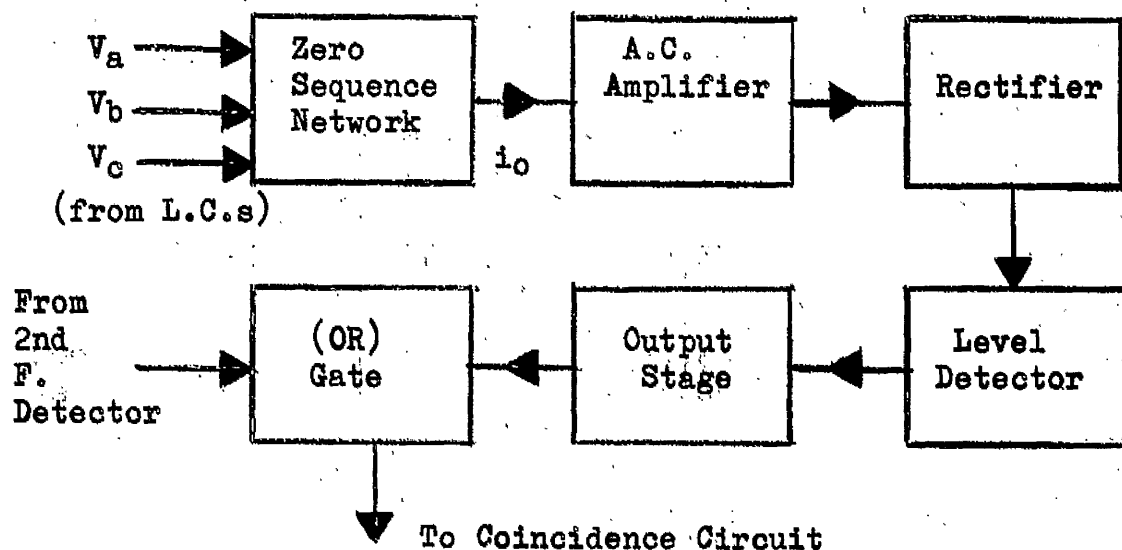
(A) Fault Detecting Circuit.
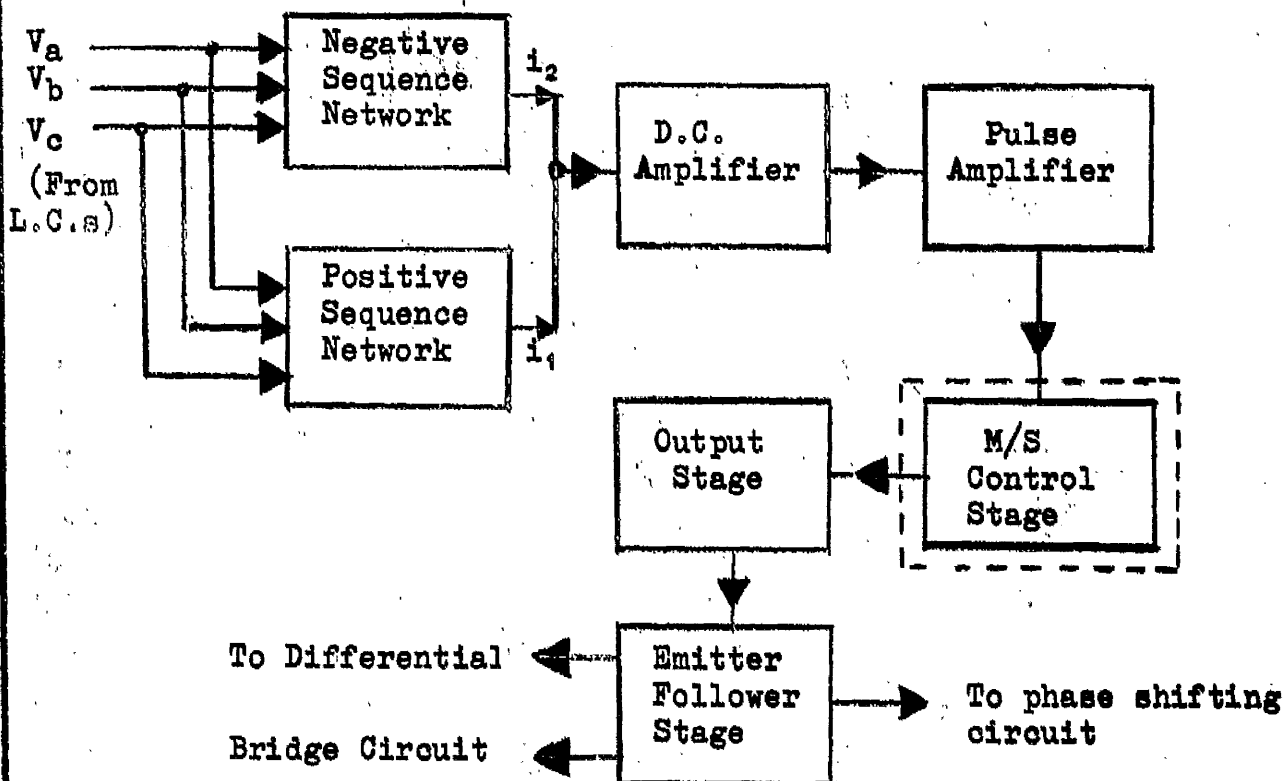
(B) Square-Wave Generating Circuit.

FIG. (2.2). CIRCUITS FUNCTIONAL DIAGRAM.

a zero sequence segregating circuit which produces an output voltage proportional to the zero sequence component I_0 of the primary currents.

The output voltage of the segregating network is amplified linearly in a one stage transistor amplifier. In fact, the design details were such that no voltage limiters are required, unlike conventional schemes, before the amplifier input.

The ironless-core C.T.s produce a voltage output of 10 V/KA primary current and according to the design of the segregating circuits, section (6.7.4), a voltage of 10 V would appear on the amplifier input at a fault level of about 50 KA for a single phase/earth fault. However, such a voltage would drive the amplifier to operate between cutoff and fully bottomed, thus producing a square-wave output without causing any further over-voltage hazards to the circuit components.

The amplified a.c. signal is then rectified for magnitude measurement by the fault level detector. The pick-up level detector is made variable and can be calibrated in terms of the primary zero sequence current I_0. The step output of the level detector is applied to an output stage (invertor) which gives a zero voltage output when the zero sequence current reaches a threshold value corresponding to level detector pick-up setting. If the current is below this level, the output stage level is at a certain negative value. The two output stages for the two fault detecting

circuits are combined in an arrangement of an (OR) gate. The output of which will be normally negative. When one of the fault detectors picks-up, then it changes to zero level in a step waveform which acts in turn as a control "let go" signal for the phase comparator circuit.

In special circumstances, e.g. pilot failure and local signal failure, the output of the fault detectors effects a tripping pulse to the relay circuit.

2.5.2 Square-wave generating circuit

The function of this circuit is to act as a square-wave generator having unity mark/space. An input voltage, the relaying quantity, signal derived from the segregating networks is applied to the square-wave generator which is followed by a unity mark/space control circuit. The squaring circuit has an output stage followed by an emitter follower (E.F.) where three square-wave outputs are produced.

The functional diagram of the different stages of this circuit is shown in Fig. (2.2B).

Three voltages V_a, V_b and V_c, are applied to two segregating networks producing output voltages proportional to the positive and the negative sequence components of the primary currents. These two outputs are combined, to form a relaying quantity, and applied to a D.C. transistor amplifier characterised by a very low input

impedance, section (8.2). The input current to the amplifier is therefore also proportional to the relaying quantity.

This single stage amplifier allows the current to flow only on one half cycle, thus converting the A.C. into unidirectional half cycle pulses. This amplifier operates between cutoff and saturation on very low magnitude input excursions, so that the output is a unidirectional square-wave. Bias control on the input of the amplifier allows to obtain a square-wave output of equal half periods, i.e. unity mark/space.

In this case also, no voltage limiting devices are required to be applied to the output of the segregating networks. In fact in order to reach the rated current of the amplifier, and for an earth fault case, the current in the primary circuit of the ironless-core C.T.s, used here, should be of the order of 30 - 50 K.A. The inherent nature of circuit eliminates the possibility of damage by overvoltages.

The square-wave output of the first amplifier is further amplified in a pulse amplifier having a very high gain in order to produce a rather sharp steep-sided wave output. As the mark/space ratio of the square wave is essential for the sensitivity of any phase comparison scheme, another circuit may be included to control the mark/space ratio. This circuit is composed of a level detector with a variable input bias to adjust the "M/S" ratio. It is followed by an output stage which produces a square-wave.

output having a magnitude from zero level to the power supply voltage. This technique has proved not to be very essential as the output voltage wave shape of the two first amplifiers is satisfactory for all practical applications, section (8.2 and 3).

The last stages of this square wave generating circuit is an invertor/emitter follower (E.F.), in order to reduce the loading effect of the following stages. Three square-wave outputs of unity "M/S" and of the same polarity as the relaying quantity are produced, two of which are fed to the differential bridge circuit and the third one is fed to the phase shifting circuit.

2.5.3 Differential Bridge Circuit

It has been established earlier in this chapter that the principle of the scheme involves the simultaneous transmission of signals from one end of the protected section to the other over the pilot-circuit. This is accomplished by the differential bridge circuit arrangement, which directs the local square-wave towards the pilots circuit.

Fig. (2.3) shows schematically the arrangement of the circuit.

The two square wave outputs from the squaring circuits are applied, after one being inverted, with different polarities to an amplifier employing two transistors in a push-pull configuration.

This push-pull stage enables to double the voltage magnitude of the square-wave to twice the available power supply voltage on the output bridge transformer.

(A) Differential Bridge Circuit

$T_{P.L.}$ Pilot Line Isolating Transf.
T_B Bridge Output Transf.
Z_c Balancing Impedance
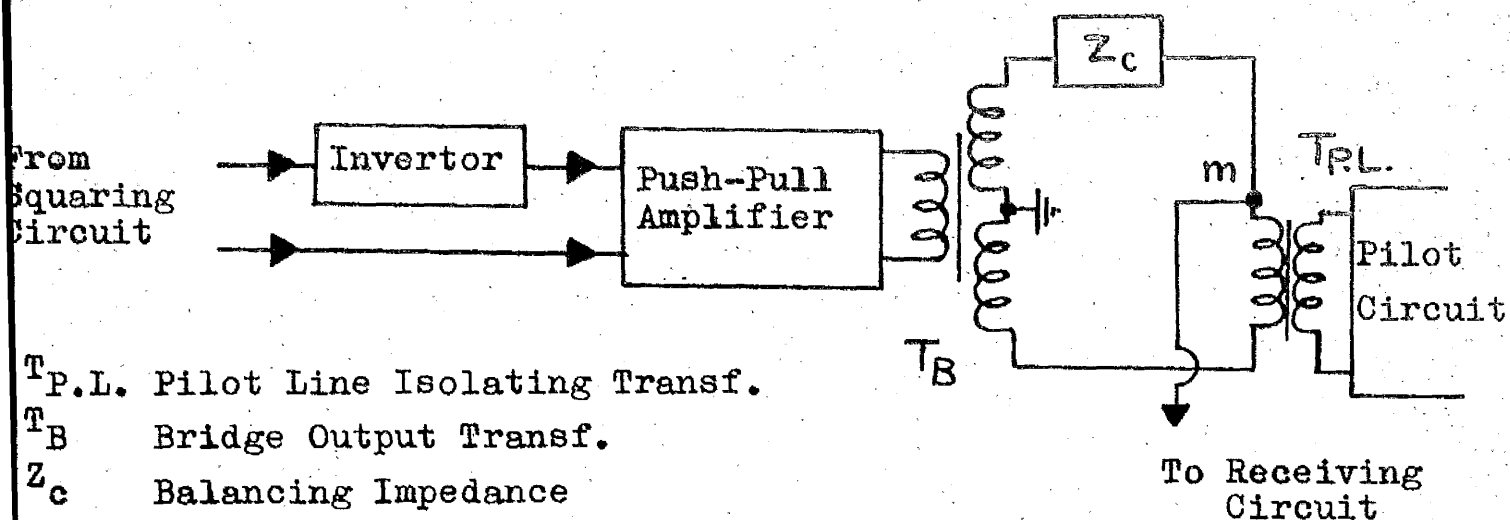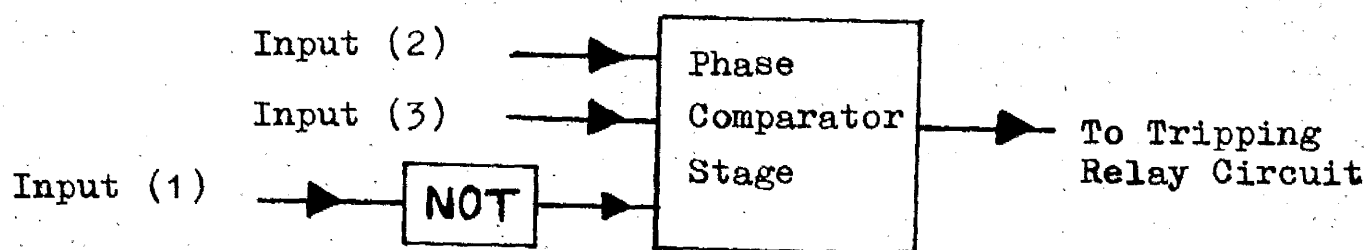
(1) Starting Circuit Output
(2) Received Square-Wave
(3) Local End Square-Wave
    (Delayed)

(B) Phase Comparator Circuit
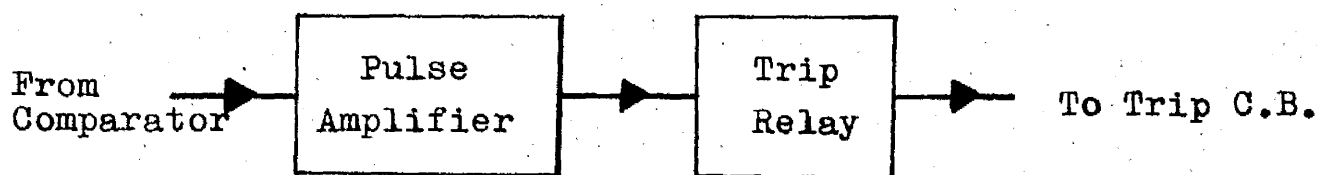
(C) Tripping Relay Circuit

FIG. (2.3) CIRCUITS FUNCTIONAL ARRANGEMENTS.

The differential bridge arrangement also avoids the return of the local square wave signal to the receiving circuit connected at point "m" Fig. (2.3). This has been achieved by the arrangement shown which comprises the balancing (compensating) impedance Z_c , so that the voltage due to the local end signal appearing at point m is practically nil. Further details of the performance of this circuit are given in section (8.8). The output bridge and the pilot line insulating transformers, are designed as pulse transformers to produce the square wave faithfully on their secondary circuits.

The power for the push-pull stage could be drawn from a separate supply different from that of the relaying circuits. This adds the flexibility of deciding, with the transformers ratios, on the magnitude of the square-wave to be impressed on the pilot-circuit.

2.5.4 Coincidence/Phase Comparator Circuit

The coincidence/phase comparator is the main logic circuit in this relaying scheme. It is composed of a coincidence stage controlled by the fault detector output. Three inputs are fed to the coincidence stage.

The functional diagram of the gating arrangement is shown in Fig. (2.3B). It comprises a "NOT" gate and a comparator stage.

Input (1) is the output of the fault detectors and normally produce zero output from the comparator irrespective of inputs

(2) and (3). When the comparator is made operative, by the application of the input signal to the (NOT) gate, then its output depends on the phase coincidence of the two square wave inputs (2) and (3). When both signals are of opposite polarity, no comparator output is produced. Any departure by angle θ^o between inputs (2) and (3), from the antiphase position, would produce an output pulse having a width equal to θ^o. The output pulse is applied in turn to the tripping relay circuit.

Inputs (2) and (3), to the comparator circuit, are the remote end square wave, received over the pilot, and the phase shifted (delayed) local square wave.

2.5.4.1 Tripping Relay Circuit

The tripping relay circuit consists of a pulse amplifier driving a sensitive relay. The input from the comparator to the tripping circuit is in the form of a train of pulses 360° apart. The width of the pulse may vary theoretically from 0° in the case of external fault to 180° for internal faults.

These pulses, as input to the amplifier stage, cause the trip relay contacts to close. This tripping stage is the final arrangement before the circuit breaker (C.B.) trip circuit.

Due to the fact that the auxiliary relay tripping current appears as pulses 360° apart, the tripping rate depends on the instant of occurrence of the fault, but it will trip always in

about one cycle, provided that the pulse width exceeds the
minimum required for the relay to trip.

2.5.5 Phase Shifting Network

The function of this circuit, as mentioned earlier in section
(2.4), is to produce an output voltage wave, either a sinusoidal or
a square-wave, lagging the input by a certain angle (delay).
Fig. (2.1) shows that the input to this circuit is provided from
the squaring circuit. In fact many alternatives for the nature of
this circuit and its input have been investigated, section (8.5),
and finally two arrangements are developed for this purpose.

The functional arrangement of the first circuit is shown in
Fig. (2.4A). It comprises of delay circuits and two amplifying
stages. Since using an amplifier would mean a phase reversal for
the input signal, therefore a second amplifier (as invertor) is
needed to correct the polarity of the output. Advantage of this
is taken by sharing the total phase shift required on the two delay
circuits. One of these circuits is made adjustable to provide
a variable delay over a certain range, and the second amplifier
would provide a control over the mark to space ratio of the square-
wave output.

The second arrangement, which is a general circuit to be
employed in conjunction with any practical pilot circuit, and to
provide a square-wave output of unity "M/S", lagging the input by

```
Input              ┌─────────┐      ┌───────────┐      ┌─────────┐      ┌───────────┐
From Squaring ───▶ │  Delay  │ ───▶ │ Amplifier │ ───▶ │  Delay  │ ───▶ │ Amplifier │
Circuit            │ Circuit │      │   Stage   │      │ Circuit │      │   Stage   │
                   └─────────┘      └───────────┘      └─────────┘      └───────────┘
                                                                              │
                                                                              ▼
                                                                          Output
                                                                     To Coincidence
                                                                         Circuit
```
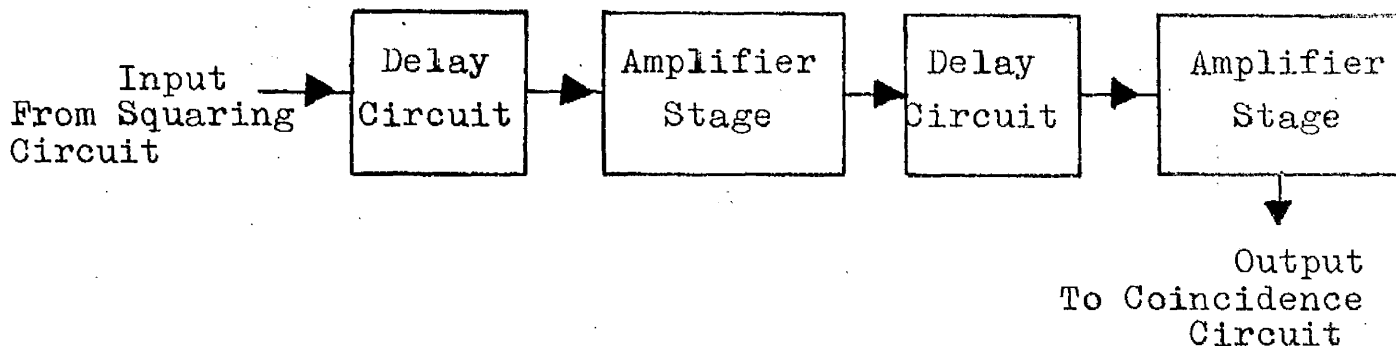
(A) Phase Shifting (Delaying) Circuit

```
Input           ┌─────────────┐      ┌──────────┐      ┌──────────────┐
Square Wave ──▶ │ Integrating │ ──▶  │  Level   │ ──▶  │ Diffrentiating│
                │    Stage     │      │ Detector │      │   Circuit     │
                └─────────────┘      └──────────┘      └──────────────┘
                                                              │
                                                              ▼
                ┌─────────────┐      ┌──────────────┐
     Output ◀── │  Monostable │ ◀──  │    Pulse     │
 Square Wave    │   10 m.s.   │      │  Rejecting   │
                └─────────────┘      │   Circuit    │
                                     └──────────────┘
```
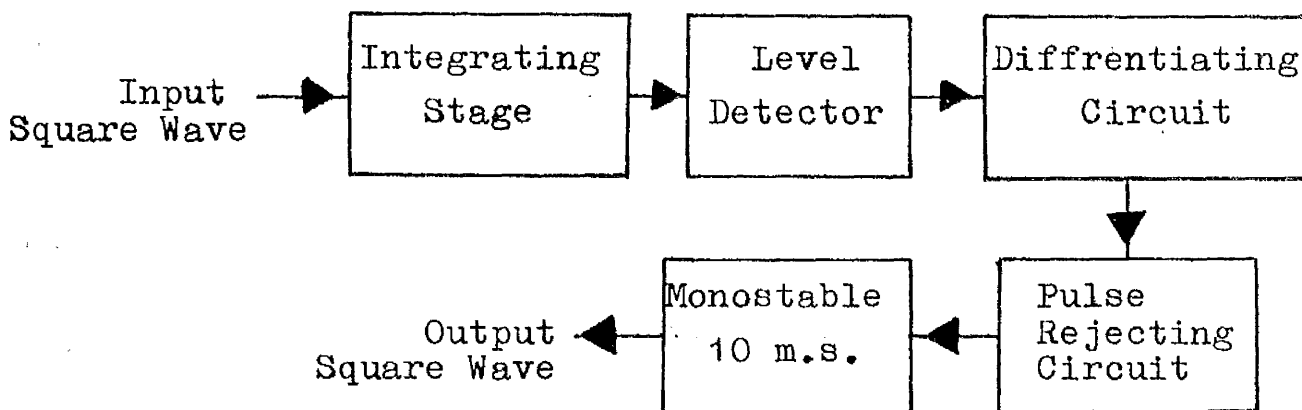
(a) Square-Wave-Input

(b) Integrator Output   L.D. Pick-up
         (A.C)   Level

(c) Level Detect. Output   L.D. Drop-out
                                                                   Level
(d) Diffrentiating Stage

(e) Rejecting Circuit

(f) Monostable Output
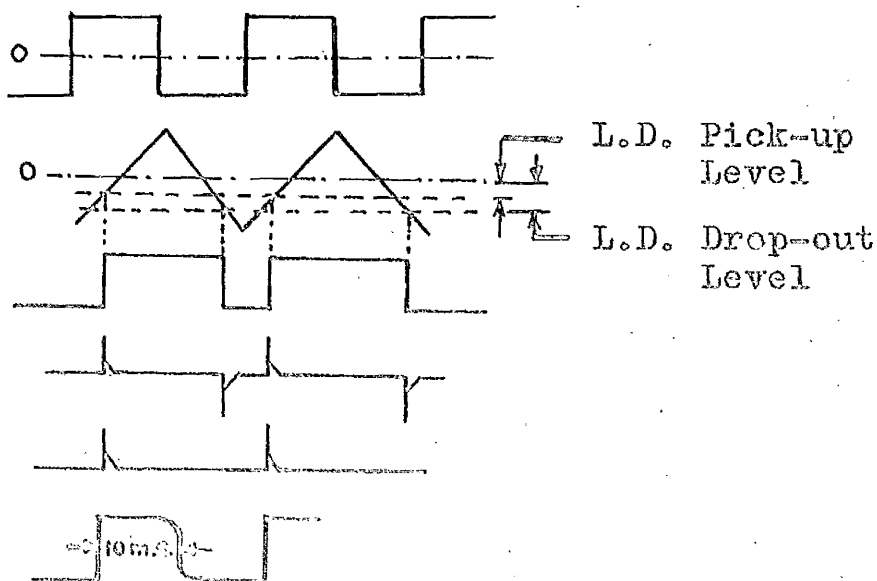
(B) Alternative Arrangement

FIG. (2.4) PHASESHIFTING CIRCUIT FUNCTIONAL DIAGRAM.

any angle ranging between $(0° \rightarrow \pi/2)$. The circuit arrangement is shown in Fig. (2.4B). The fundamental principle of the function of this circuit can be explained in the following manner:-
The integrating stage output is in the form of a triangular wave, since its input is a squarewave, having the same period as the input when taken in the form of a symmetrical A.C. signal. The level detector has an adjustable pick-up level and it produces a step output whenever the input reaches the pick-up level and drops off when it passes, (going less negative), its drop-off level. The output is, therefore, in the form of a rectangular wave as shown in Fig. (2.4B). The differentiating circuit produces positive and negative pulses at the points of sign change of the rectangular input wave, each consecutive positive or negative pulses are (2π) apart. The rejecting circuit eliminates the negative pulses leaving the positive ones to trigger the monostable which has a fixed unstable duration time of 10 m.s. This results in producing a square wave of a unity "M/S". It can be seen also that by changing the setting of the pick-up level of the level detector the monostable output lagging (delayed) angle can vary between $(0° \rightarrow \pi/2)$. However, the behaviour of this circuit is mentioned again in section (8.6), and such circuits would produce an error in the "M/S" ratio of the output wave, due to any primary system frequency deviation.

2.5.6 Receiving/Reshaping Circuit

The function of this circuit is to recover and restore the square-wave from the remote end which has been transmitted over the pilot-circuit.

In other words this circuit compensates for the signal attenuation over the pilot-circuit.

It is composed of an amplifier of two stages, with "M/S" adjustment, to restore the steep fronts of the received signal from the differential bridge circuit. The output square wave of the receiving circuit is then applied to the coincidence circuit to be compared with the output of the phase shifting network.

The first stage amplifies the signal and controls the "M/S" ratio, while the second stage which is acting as pulse-switch produces a square wave signal with the same polarity as the received input.

CHAPTER 3

IRONLESS CORE CURRENT TRANSFORMERS

OR LINEAR COUPLERS

3.1 Introduction

In certain applications, in protective gear, iron-cored current transformers have reached the limits for further development. These applications are mainly those in which high relaying speeds and/or very high primary currents are involved. Ironless-core current transformers (air-cored toroids), or linear couplers as they are generally called in protection, can operate satisfactorily in such conditions. It is for these reasons that they have been investigated in the Power Systems Laboratory of the Manchester College of Science and Technology[21][26] and have been chosen to be incorporated with the scheme developed here.

Their use is not, however, confined to extreme conditions; they can be used, with an advantage, in a wide range of protective gear applications.

Ironless-core C.Ts (linear couplers) usually take the form of a toroidal winding similar to that of a conventional current transformer, but are wound on a non-magnetic core. They are usually constructed for operation from a primary bar, which is the normal practice for systems with high short-current levels, but a wound primary could be provided if necessary.

The absence of the iron core in a C.T., causes the mutual inductance m , between the secondary winding and the primary circuit, particularly with bar primary circuit, to be rather low. This leads also to the consequence that ironless core C.T.s have two major advantages over the iron-cored ones

(i) Under normal steady state conditions, the open-circuit voltage in the secondary circuit is $j\omega m\, I_p$, where I_p is the primary current. The mutual inductance "m" is a function only of the geometrical shape of the winding, and does not vary with the primary current. The secondary voltage is therefore a perfectly linear function of the primary current even at the highest values encountered, unlike air gap conventional C.T.s, where linearity is over a range not exceeding 10 KA.

(ii) The instantaneous secondary voltage, under transient conditions is $m(dI_p/dt)$, where I_p is the instantaneous value of the primary current; therefore, if the waveform of the primary current contains any exponentially decaying unidirectional components, as it generally does under fault conditions, these components will be decreased in the secondary voltage waveform with respect to the sinusoidal components if their time constant is large. High speed relay operation is generally limited by the presence of these unidirectional components in the fault current waveform, so that their reduction by linear couplers can be used as a basis for much faster protective relays.

3.2 Factors Governing the Application of Ironless-Core C.T.s (Linear Couplers)

3.2.1 Power Output

It is clear that the power available from an ironless-core C.T. is much less than that from a conventional one. This has been so far the principle limitation for the use of ironless-core C.T.s in full replacement for conventional ones. With the advent of low burden relays, including completely transistorised schemes, low output has become no longer a major disadvantage for most applications.

It is convenient, however, to specify the output of an ironless-core C.T. power in terms of the apparent short circuit power, i.e. the magnitude of the short circuit current multiplied by the magnitude of open-circuit voltage, at one K.A. (say), primary current in each case. Approximately one quarter of this apparent short circuit power will be available to a matched burden.

3.2.2 Considerations Governing Power Output

The output power from an ironless-core C.T. is determined mainly be the following considerations.

(a) The available space: Like conventional C.T.s, they must be made to fit into switchgear chambers. The switchgear designer generally stipulates the maximum external diameter, the minimum internal diameter and the axial length.

(b) The core size for a given overall external dimensions,
determines the actual power output.

(c) The winding space factor: This modifies the optimum core size
to a small extent, but generally for medium wire gauges, this factor
is in the order of 0.6.

3.2.3 Stability

It is well known that, the stability of protective gear under
through fault conditions depends on the accuracy of the current
transducers. In the case of ironless-core C.T.s the quantity which
should be controlled is the mutual inductance and this, in general,
can be wound to an accuracy of about one per cent, representing
a stability ratio of 100 in a voltage summation scheme as
discussed in Chapter (4).

Uniformly wound toroids are unaffected by stray fields in
planes perpendicular to the bar primary axis, other than those due
to the ampere-turns actually passing through the centre opening.
They are therefore independent of the primary position, and return
circuits in parallel configuration. Small stray effects may arise
from fields having a component parallel to the axis and interlinking
the coil since from this point of view each layer constitutes one
turn linking such a field. These strays may be eliminated, if
necessary, by reversing the progression of winding every one or
two layers.

3.4 Transient Behaviour of Iron and Ironless-Core C.T.s

3.4.1 Primary Current Equation

Power distribution networks are usually highly reactive. High voltage networks may have a reactance to resistance ratio of more than twenty to one. As a result, fault currents are usually accompanied by exponential transient currents, which are presented to any current transducers in the circuit. These types of transient currents cause a considerable difficulty in the design of iron-cored C.T.s and their associated relay circuits[13].

Fig. (3.1) shows an equivalent circuit of a power system referred to the secondary side of a current transformer. The occurrence of a fault on the system is represented by closing the switch "S" at the instant $t = 0$, i.e. when the applied voltage is $E \sin \phi$. The current which will subsequently flow is given by the equation

$$L \frac{di}{dt} + Ri = E \sin (\omega t + \phi) \qquad \ldots\ldots \ (3.1)$$

hence
$$I = \frac{E}{|Z|} \left[\sin (\omega t + \phi - \theta) - \sin(\phi - \theta) e^{-\frac{R}{L}t} \right]$$
$$\ldots\ldots \ (3.2)$$

where $|Z| = (R^2 + \omega^2 L^2)^{1/2}$

$\theta = \text{arc tan } \omega L / R$,

and $\phi = $ angle at which the fault occurs.
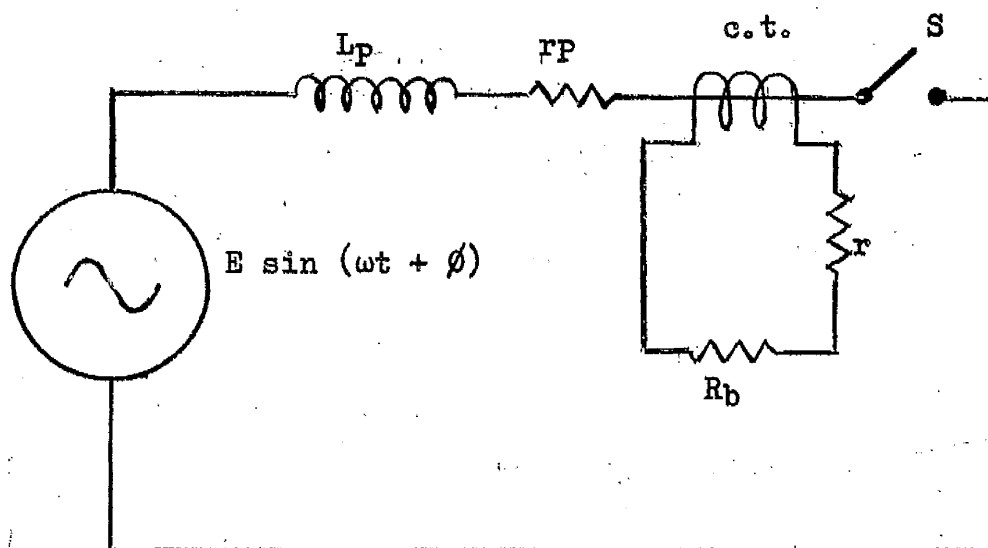
FIG. (3.1). SIMPLIFIED POWER SYSTEM FOR
TRANSIENT CALCULATIONS.

N = No. of Turns
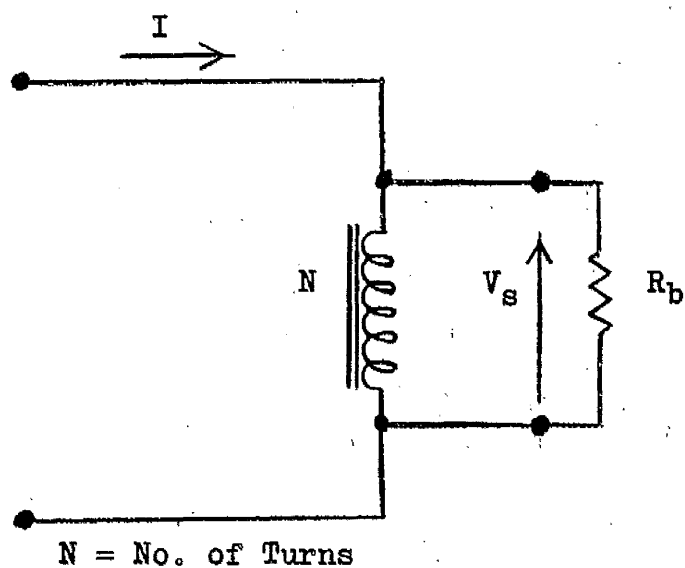
FIG. (3.2). EQUIVALENT CIRCUIT FOR DERIVATION
OF FLUX IN AN IRON-CORE C.T.

Eqn. (3.2) implies that under the worst possible conditions, the magnitude of the transient term can be equal to the peak value of the alternating current component.

3.4.2 Transient Flux of Iron-Cored Current Transformers

It is important to investigate the effect of the current wave of eqn. (3.2) on the flux in the iron core of the current transformer. The analysis given here is rather brief, and only considers the effect in an ideal C.T. working with the severest possible practical burden conditions, i.e. with a resistive burden.

Fig. (3.2), shows the simplified equivalent circuit for flux calculation, the secondary voltage is:-

$$V_s = I \cdot R_b \qquad \ldots \ldots \ (3.3)$$

Now the flux   in the core of a current transformer, considered to be ideal and having N turns, is given by:-

$$\phi = \frac{1}{N} \int_0^t V_s \, dt \qquad \ldots \ldots \ (3.4)$$

Substituting eqns. (3.2) and (3.3) in (3.4) it follows:-

$$\phi = \frac{R_b \, E}{\omega N \, |Z|} \left[\cos(\omega t + \phi - \theta) + \frac{\omega L}{R} \sin(\phi - \theta) e^{-\frac{R}{L}t} \right] + K \qquad \ldots \ldots \ (3.5)$$

where K is the integration constant.

Two extreme cases may now be considered:-

(i) When $\sin(\phi - \theta) = 0$, i.e. $\phi - \theta = 0$

Substituting this in eqn. (3.5), then

$$\phi_1 = \frac{R_b\, E}{\omega N |Z|}(\cos \omega t - 1) \qquad \dots (3.6)$$

It should be noted that this condition if substituted in eqn. (3.2), then the primary current contains no transient term. Nevertheless, the flux wave has a component, due to the transient, equal in magnitude to the peak of the alternating flux. This phenomena is known as flux doubling effect.

(ii) When $\sin(\phi - \theta) = 1$, i.e. $\phi - \theta = \frac{\pi}{2}$

Substituting in eqn. (3.5), it follows:-

$$\phi_2 = \frac{R_b\, E}{\omega N |Z|}\sin \omega t + \frac{\omega L}{R}(1 - e^{-\frac{R}{L}t}) \qquad \dots (3.7)$$

This condition gives the maximum transient in the primary current wave. The transient flux in the iron-core of the C.T. rises exponentially to a value $\omega L/R$ times the peak of the alternating value. In view of the fact, mentioned in section (3.1), that $\omega L/R$ may be equal to or greater than 20, this simply means that in designing conventional C.T.s a very large flux margin must be allowed. As an example, if linear operation up to ten times full load has to be permitted, a margin of 200 or more must be allowed on the full load peak alternating flux. This is clearly

an impossible margin or rather an impractical one. In practice the transient flux to be expected will be somewhat less than that given by eqn. (3.7).

It is clear from eqn. (3.3) that with a purely inductive burden, transient flux components are much reduced.

3.4.3 Time taken to reach Saturation

From eqn. (3.7) is is apparent that shortly after the inception of a fault-current containing a transient unidirectional component, the current transformer core will saturate. As the build-up of the flux is exponential there will, however, be an initial time interval in which the current transformer will function normally. If this time interval is sufficiently large to permit the operation of the protective gear, then high speed protection is possible; if it is not, then a delay in the operation of the protection has to occur until the current transformer core desaturates (or comes out of saturation). Such a delay may be of the order of 10 cycles or more.

The actual time may be calculated from eqn. (3.7), but the analysis would be tedious. An approximate time can be derived by assuming that the exponential term rises linearly with its initial slope.

In eqn. (3.7), the term $\dfrac{R_b E}{|Z|}$ is the peak value of the steady-state alternating secondary voltage V_s . Substituting this in eqn. (3.7) and differentiating, the linearised transient

flux is :-

$$\Phi' = \frac{V_s}{N} t \qquad \qquad \ldots\ldots \quad (3.8)$$

Now V_s may be expressed as a fraction of the alternating saturation voltage, so one may write:-

$$V_s = \frac{2\pi f \, N \, \Phi_s}{K}$$

where Φ_s = saturation flux.

and $\quad K$ = ratio between the steady state saturation alternating voltage and V_s.

Substituting from eqn. (3.8) then:-

$$\Phi_s = \frac{2\pi f \, N. \, \Phi_s \, t}{KN}$$

$$\qquad \qquad \ldots\ldots \quad (3.9)$$

Hence $\quad t = \frac{K}{2\pi f}$

The number of cycles "n" , which elapse before reaching saturation is, therefore,

$$n = t \cdot f = \frac{K}{2\pi} \qquad \qquad \ldots\ldots \quad (3.10)$$

This last eqn. (3.10) indicates that one cycle of the alternating current can be transformed faithfully only if the ratio between saturation flux and peak steady alternating flux is about six to one. Eqn. (3.10) is pessimistic, and is also

for the worst possible transient conditions; as such it is
considered a reasonably safe criterion of practical design.

It follows that, in order to economise on conventional
current transformer size, very high speed protective gear is
essential. If operation has for example to take place in the
period of two cycles, then the flux ratio K must be about
twelve.

3.5 Transient Response of Ironless-Core C.T.s or Linear Couplers

Considering the case of a current as given by eqn. (3.2)
with 100% unidirectional component, i.e. $\sin(\phi - \theta) = 1$, to be
applied to the primary bar of an ironless core C.T., then:-

$$I_p = \frac{E}{|Z|} \cos \omega t - e^{-\frac{R}{L}t} \qquad \ldots \ldots (3.11)$$

where Ip is the primary fault current,

R and L are components of primary impedance Z

E is the system primary peak voltage.

If this current transducer has a mutual inductance "m"
with the primary conductor, then the secondary induced voltage
V_s will be given by :-

$$V_s = m.\left(\frac{d\,I_p}{dt}\right) \qquad \ldots \ldots (3.12)$$

hence $V_s = -j\omega m.\frac{E}{|Z|}\left\{\sin \omega t - \frac{R}{\omega L}.e^{-\frac{R}{L}t}\right\}$

$$\ldots \ldots (3.13)$$

Thus the secondary transient voltage term is reduced by the reactance to resistance ratio, or the Q factor, of the primary circuit impedance. In section (3.4.2) it has been shown that iron-cored current transformers meet increasing difficulties when the "Q" factor of the primary circuit is large, while ironless-core current transducers are relatively not influenced by it.

Generally speaking, when the Q factor is low, the transients produced are short in duration, and have no effect beyond a fraction of the first cycle. On the other hand, when the Q factor is large, the amplitude of the transient is reduced by the ironless-core current transducer and causes little error. For instant, if the Q factor is 30, the time constant of the transient is 95 m.s., or 4.75 cycles, and its amplitude is reduced to 3.3% of the peak of the alternating quantity. The secondary voltage is, therefore, offset by 3.3% when the primary current is containing a 100% unidirectional component, i.e. fully offset. Any error which may occur in the pick-up, or any time delay in operation due to the transient cannot exceed 3.3%, and will generally be less. It may, therefore, be concluded that linear couplers are, for all practical applications, free from transient errors.

3.6 The Effect of Fault Current Asymmetry on Phase Displacement

In the developed phase-comparison scheme the sensitivity of phase displacement between the two end currents of the protected section is limited to a minimum stability angle $\pm \alpha^o$, i.e. a fault causing a phase displacement less than $\pm \alpha^o$, (measured from the anti-phase position) would not cause any tripping.

The presence of a unidirectional transient component in the fault current, at any of the two ends, will tend to modify the stability angle of the scheme.

In fact the presence of a unidirectional component reduces the duration of the square-wave on one half cycle and increases it on the other half, resulting in a deviation from a unity mark to space ratio.

The most extreme unfavourable case, for this scheme, is that of an internal fault with a negative unidirectional offset at both ends. Fig. (3.3A), represents the current waves for such a case. It is assumed that the remote end current leads the 180° out of phase position by an angle α^o. The tripping relay current in the absence of unidirectional component will be a train of pulses each of a duration α and 360° apart, as shown in Fig.(3.3B).

From Fig.(3.3C) it can be seen that the first positive half cycle of the local end current is reduced by an angle
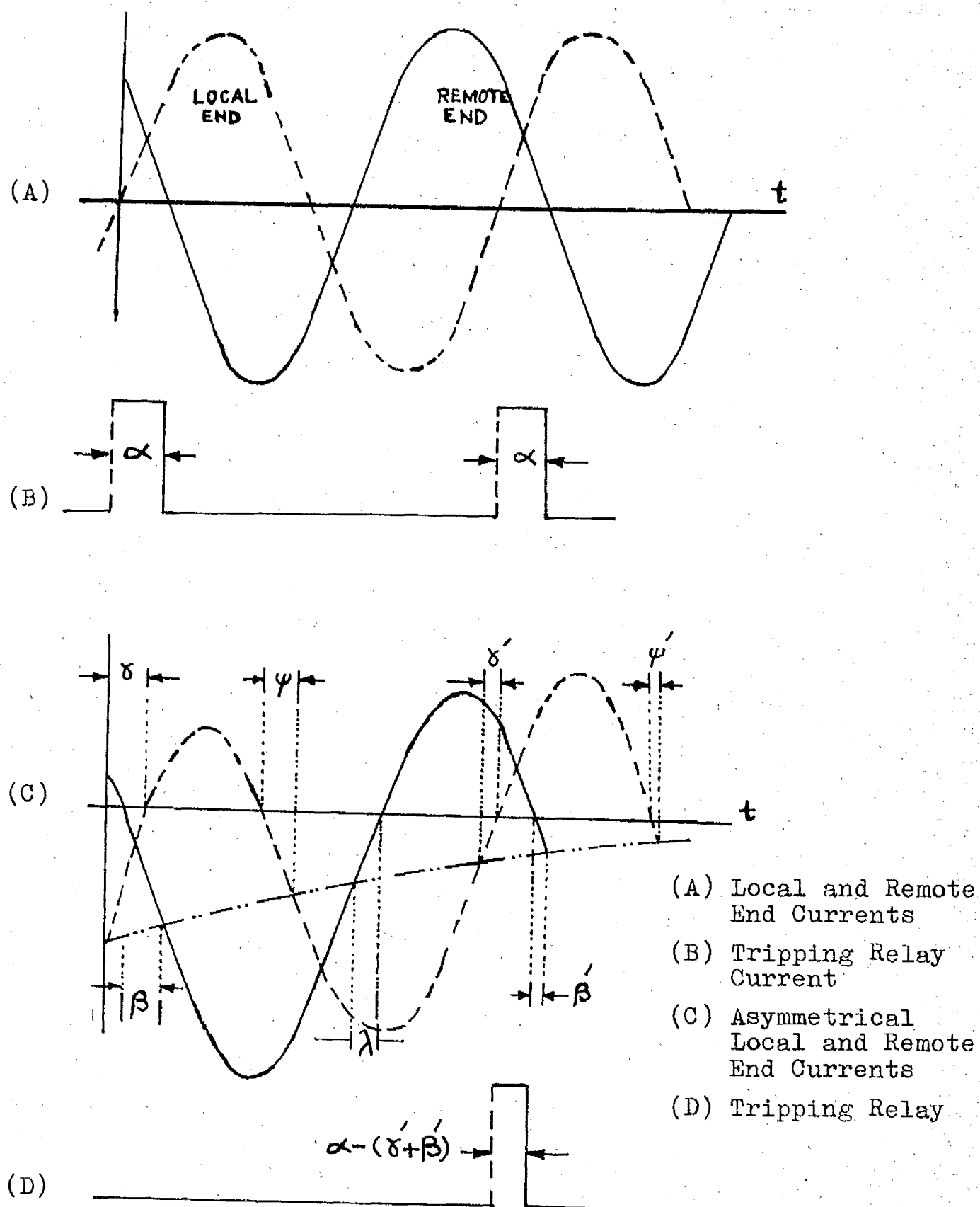
FIG. (3.3)   EFFECT OF UNIDIRECTIONAL COMPONENTS
ON STABILITY ANGLE.

$(\gamma + \psi)$ and the first negative half cycle of the remote end is increased by an angle $(\beta + \lambda)$. On the second cycle the reduction and increase will be $(\gamma' + \psi')$ and $(\beta' + \lambda')$ respectively.

The result is that the tripping relay current pulse, Fig. (3.3D), is reduced by an angle $(\gamma' + \beta')$ and consequently the instantaneous angle of stability is increased by the same amount. In Fig. (3.3D) the magnitude of the offset component is large enough that the first tripping relay pulse disappears as $(\gamma + \beta)^\circ$ are bigger than α°. This has been done so for the sake of illustration only.

The reduction in the tripping relay pulse disappears in proportion to the rate of damping of the unidirectional components themselves.

The risk remains nevertheless that such phenomena would cause appreciable delay in tripping if such schemes were associated with iron-cored conventional C.Ts. Fast schemes, as the one envisaged, designed to operate within 2 cycles would, therefore, definitely suffer from delay.

However, the use of ironless-core current transducers would reduce the magnitude of unidirectional transient component on practical systems to less than 5% and therefore, the risk of any delay or stability angle reduction would be practically negligible if tripping has to occur within 2 cycles.

This arrangement has totally eliminated the need for

complicated and expensive d.c. filter networks which are

generally associated with schemes using conventional C.T.s.

CHAPTER 4

RELAYING QUANTITIES FOR DIFFERENTIAL

FEEDER PROTECTION

4.1. Introduction

The principle of comparing input and output currents is well established in the protection of feeders. The quantities at each end of the protected section may be compared in either magnitude or phase, or a combination of both. This could be carried out for each phase individually thereby introducing a great deal of complexity in the protective gear, such schemes have been abandoned on the grounds that they are complex and uneconomical. In general, differential feeder protection uses a single relaying quantity at each end of the protected section. To achieve this some device is necessary which will combine the currents of all three phases. This may be done by means of:-

(a) a summation transformer, associated with conventional phase-current transformers,

(b) or its equivalent connection for ironless-core C.Ts (linear couplers), shown in Fig. (4.6).

(c) by the use of a combination of symmetrical phase sequence components derived from segregating networks.

A detailed analysis of the outputs of the summation

transformer and various combinations of phase sequence currents

under different single shunt faults has been made by Adamson and

Talkhan[9].

A critical review of the summation transformer and its

equivalent connection with linear couplers is discussed in this

chapter.

The single relaying quantities for feeder protection have

some specific functions to perform in a relaying scheme as a

whole, and in particular for a phase-comparison scheme as the

one under discussion.

4.2. The Functions of Relaying Quantities for Phase-Comparison

Schemes

The relaying-quantities, derived from a system under fault

conditions, have two main functions in the envisaged phase-

comparison scheme, described in this work:-

(i) The magnitude of the relaying quantity should represent

and give indication of the occurrence of a fault. The fault

indicating quantity is usually fed to fault detecting elements,

generally known as the starting elements. The output of these

starting elements would render the protection scheme ready to

carry out its function and under special cases may initiate

tripping.

(ii) The phase angle of the relaying quantity should represent faithfully the phase angle of the current under all fault conditions. This phase angle representing signal is transferred over a link (channel) to the remote end of the protected section where it is compared in phase with a similar relaying quantity representing the fault conditions at the local end. Proper compensation for phase shift due to the link, if any, has to be carried out before comparison takes place.

Some schemes[6] use the same relaying quantity for both fault detection and for phase representation, while others[7] use different relaying quantities. The decision affecting the choice of the relaying quantities was taken on the basis of experience gained from difficulties arising from the applications to a particular system. In other words, the relaying quantities were decided upon for local circumstances, with the result of using different relaying quantities for the same scheme.

It was recently[9] shown that a particular combination has been favoured as a relaying quantity for feeders. It can be used for most faults which may occur on a transmission system.

4.2.1. Relaying Quantities Representing and Indicating Fault Conditions

Relaying quantities, when expressed as a function of the fault current, depend mainly on the type of fault. Symmetrical three phase faults are sometimes detected in a manner different

from that for unsymmetrical ones. Three phase faults are generally
associated with extremely high values of positive sequence current
and therefore higher relay settings are used to discriminate
between faults and overloads.

In the case of unbalanced faults, however, the fault current
may be resolved to its symmetrical component currents. These may
include also the zero sequence component when the fault involves
earth or in cases of series unbalance, e.g. an open conductor.
This last type of fault has attracted special attention in recent
years as a result of practicing single phase switching on high-voltage
systems in order to clear single phase to earth faults. The
appearance of the negative sequence component current is common
to all types of unbalanced faults whether they involve earth or
not. This feature together with the fact that its magnitude is
zero under normal balanced load conditions makes it suitable as a
fault indicating and/or representing relaying quantity. Fault
detecting elements in some cases are made to respond to the presence
of the negative sequence component of fault current. When the
amplitude of this component reaches a predetermined level, the
detecting elements respond instantaneously and holds so long as
the fault persists.

The present of the zero-sequence component of the fault
current, or its appearance, does indicate either a fault involving
earth or a series fault, and, therefore, is used also for fault
detection.

Low fault currents are generally encountered with single phase to earth faults and therefore the presence of the zero sequence component current is a favourable choice for the detection of these faults. The positive sequence component can also then be used to indicate and/or represent polyphase faults, not involving earth, where the current levels are generally much greater than the normal loads encountered on any system.

The choice of any two of the sequence components would be generally suitable as relaying quantities for fault indication but for phase-comparison schemes the phase angle of the fault representing relaying quantity has to be examined also before any definite choice is favoured.

4.2.2. Phase Angle Representation Under Different System Conditions

A relaying quantity, for phase-comparison protection schemes, has to represent faithfully the current at each end of the protected section, either under normal loads or fault conditions.

It is clear that none of the sequence component currents alone can represent the phase of the fault current. The positive-sequence component of the fault current cannot be used alone since the load current, which is totally positive sequence, may mask it under maximum loading conditions when associated with low fault currents. This may cause also failure to trip under certain internal faults.

The absence of negative sequence component, though it gives a correct phase representation without being affected by the load current, during symmetrical three phase faults is a drawback and therefore limits its choice alone.

The zero sequence component of the fault current depends on the different methods of neutral earthing and may even not be present at one end of a protected line having an isolated transformer neutrals. Also its absence during three phase faults adds another limitation to its application as fault representing quantity.

In papers published[8][9] the authors held the opinion that the optimum combination of phase-sequence components for adequate representation of the fault current under all system fault conditions, is a combination of the negative and positive sequence components. The general form of the suggested relaying quantity I_m, which is used to represent the fault current of the 3-phase system both in magnitude and phase, is given by:-

$$I_m = MI_{a2} + NI_{a1} \qquad \dots\dots (4.1)$$

where I_{a1} and I_{a2} are the positive and negative phase sequence components of the current in phase "A" respectively, "M and N" are coefficients which may have a range of relative values.

A detailed analysis and investigation in the nature of this relaying quantity I_m is given in the next chapter.

Another method used to obtain a single relaying quantity, from the 3-phase currents, is the well-known summation current transformer derived by 3 C.T.s one on each phase.

4.3. Summation Current Transformer (S.C.T.)

The summation current transformer is widely used for the derivation of a single relaying quantity for protective systems because of its inherent construction simplicity.

It is well-known that the summation transformer has its limitations. A critical study of these limitations is made here in this section. It is also known that certain "blind spots" may occur, with the application of S.C.T.s for which a low output is obtained under internal fault conditions, particularly with resistance earthed systems.

The following examines its limits of application.

4.3.1. Summation Current Transformer Limitations

A typical S.C.T. arrangement is shown in Fig. (4.1), having primary winding ratios of 1:1:n.

The output of the S.C.T. (I_{ST}) is thus given in a matrix form by:-

$$I_{ST} = \left[(2 + n) \quad (1 + n) \quad (n) \right] \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad \ldots \ldots (4.2)$$
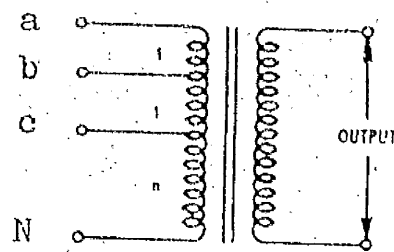
(S.C.T.)
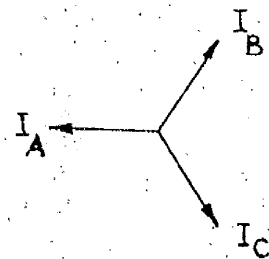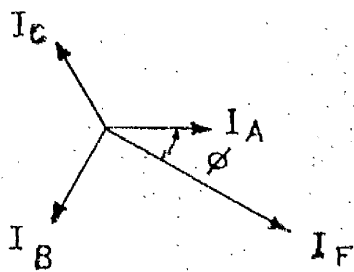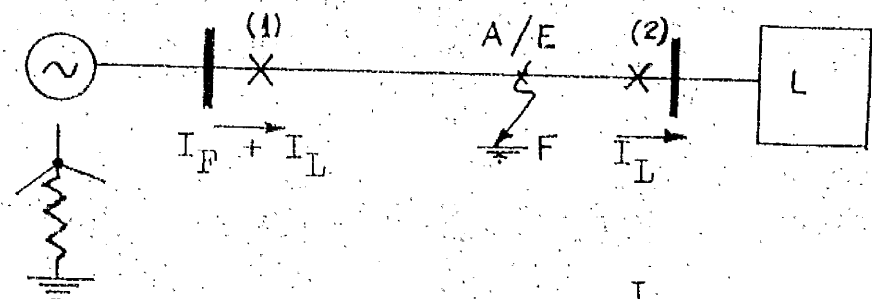
$$\vec{OA} = (n+2)(I_F + I_A) + (n+1)I_B + nI_C \qquad \vec{OB} = (n+2)I_A + (n+1)I_B + nI_C$$

END (1)   END (2)

FIG. (4.1) SUMMATION CURRENT TRANSFORMER.

$$= \left[3(1+n) \quad (2 + a^2) \quad (a + 2) \right] \begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix} \quad \ldots \ldots \ (4.3)$$

where I_0, I_1 and I_2 are the zero, positive and negative sequence components of the reference phase current I_a.

Phase rotation given by "ABC".

There are, however, certain well-known "blind spots" with S.C.T.s in general and with their application for pilot wire protection in particular. A condition of phase angle comparison masked by load current is illustrated, in Fig. (4.1), for an earth fault on phase "A" coincident with a heavy load current flowing through the feeder. If I_a, I_b and I_c are unity P.F. load currents of phases "A, B and C" respectively. The S.C.T. ampere-turns at the two ends of the feeder are drawn, (assuming n = 3), giving outputs $(\overline{OA})$ at the fault in feed end (1) and $(\overline{OB})$ at the load end (2).

With the particular values shown for I_a and ϕ_F it is seen that the outputs are almost in antiphase but differ in magnitude. "ϕ_F" being the angle of the fault current. A phase-comparison pilot wire protection scheme, associated with S.C.T.s may then fail to trip when used in conjunction with power systems having resistive earthing for limiting the single phase to earth fault current. It is, therefore, important that amplitude comparison should be applied up to approximately twice the rated feeder load current in such cases.

Two conditions for zero, or rather low, outputs from a S.C.T. are also illustrated in Fig. (4.2 A and B).
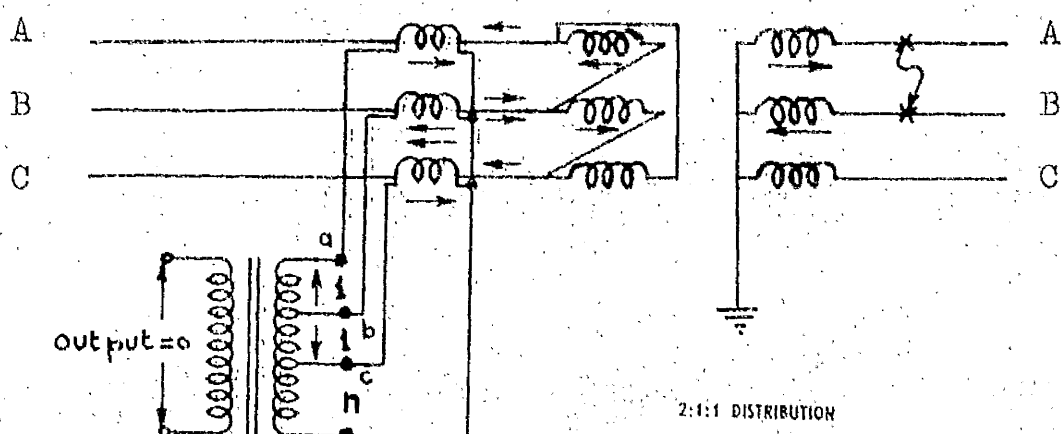
(A) Star/Delta Transformer.
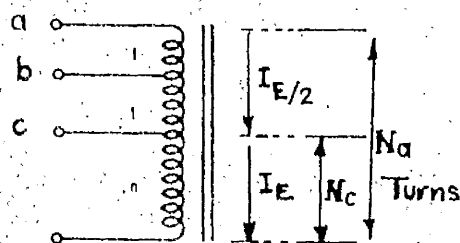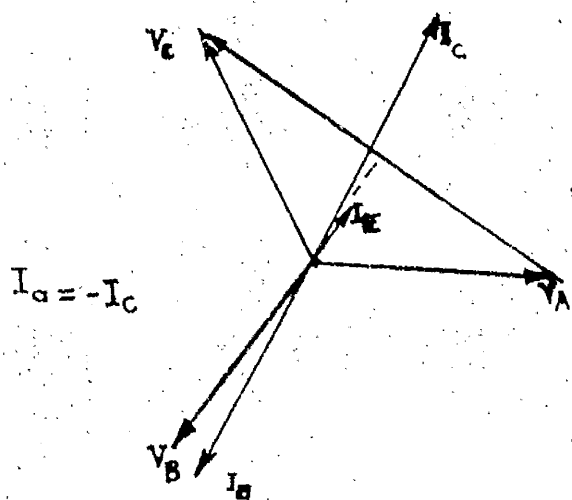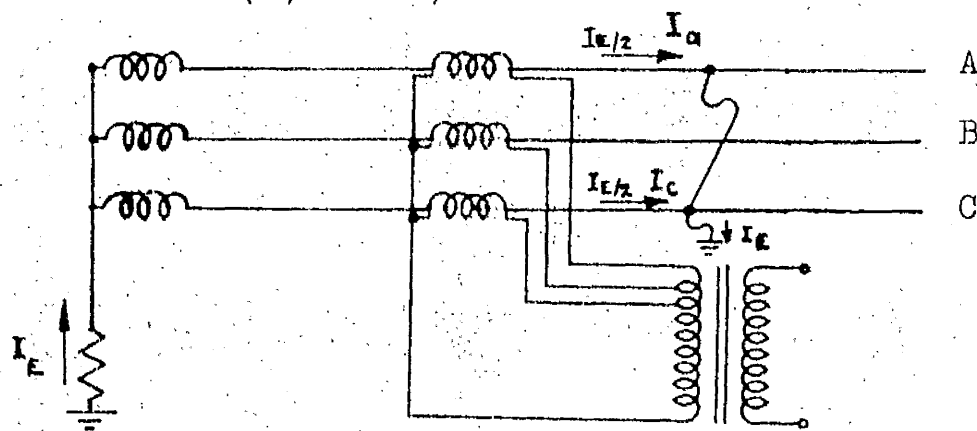
(B) Double Phase to Earth Fault.

FIG. (4.2) SUMMATION CURRENT TRANSFORMER.
(No Output Conditions)

A phase to phase fault as shown in Fig. (4.2 A), on the star connected secondary of the transformer would lead to a current distribution on the delta side of 2:1:1 on phases B, C and A, respectively. With equal ab and bc turns on the S.C.T. primary, the secondary output will then be zero. The simple S.C.T. is, therefore, not suitable for use on a transformer/feeder over all pilot-wire protection scheme. A general case analysed in more detail for similar conditions is given in Section (4.3.3.).

Another possible low output condition is under double phase to earth fault conditions on a system with resistance earthed neutral, as shown in Fig. (4.2 B). For a certain ratio of phase/earth fault current the S.C.T. output may be low. In Fig. (4.2 B), if it is assumed that I_C and I_E are in phase, then the S.C.T. primary amp.-turns is given by:-

$$\text{Total A.T.s} = \tfrac{1}{2} I_E (Na + Nc) - I_C (Na - Nc) \quad \dots \dots \quad (4.4)$$

Then the condition for no output will be:-

$$\frac{I_C}{I_E} = \frac{(Na + Nc)}{2(Na - Nc)} \qquad \dots \dots \quad (4.5)$$

For a typical S.C.T. having turns ratios of 1:1:3, the expression in eqn (4.5) would give $\frac{I_C}{I_E} = 2$, a ratio that may well occur in practice.

4.3.2. <u>Summation Current Transformer Output under Fault Conditions.</u>

For the typical S.C.T. arrangement shown in Fig. (4.1), the output "I_{ST}" is given by eqns (4.2 and 4.3).

For balanced three phase input currents I_a, I_b and I_c, the output

$$I_{ST} = (2 + a^2) I_a$$

Hence $I_{ST} = \sqrt{3} \ I_a \ \underline{/-30^\circ}$

..... (4.6)

The effect of an unbalanced input, e.g. a fault condition, will be considered by the use of symmetrical components as given in eqn (4.3).

(a) <u>Single phase to earth fault</u>

The connection of the sequence networks for such a fault is shown in Fig. (4.3). Under this fault condition,

$$I_1 = I_2 = I_0 = \frac{V}{Z_1 + Z_2 + Z_0} = \frac{V}{Z_1} \ \frac{1}{1 + 2K}$$

..... (4.7)

where $K = \frac{Z_0}{Z_1} = \frac{Z_0}{Z_2}$

For phase "A"/earth fault, I_a = fault current,

Hence $I_a = I_F = 3I_0 = 3 \frac{V}{Z_1} \ \frac{1}{1 + 2K}$ ..... (4.8)

The vector relationships between the sequence component currents are also shown in Fig. (4.3). For such a fault, the

Phase "A/E" Fault

Phase "B/E" Fault
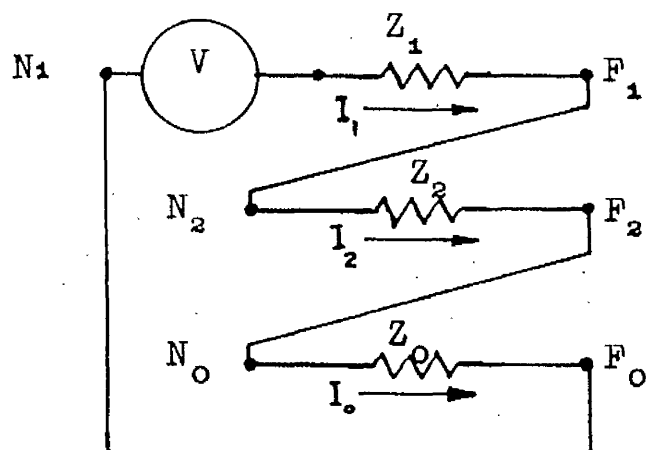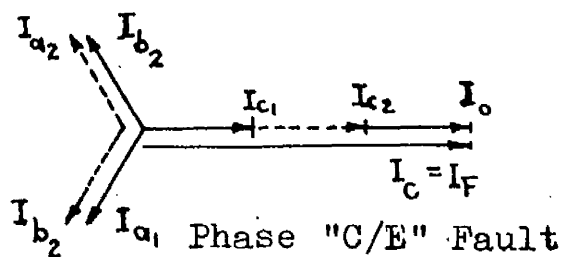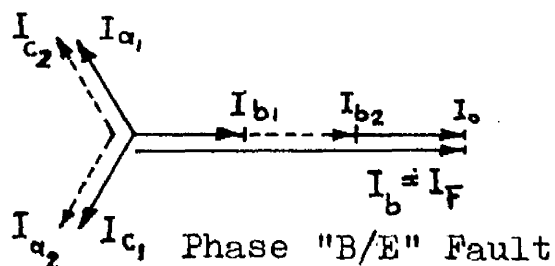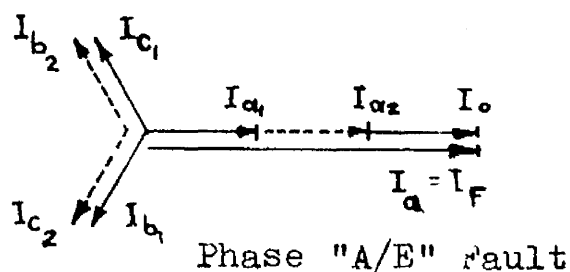
Phase "C/E" Fault

FIG. (4.3) SEQUENCE NETWORKS CONNECTION.
(Single Phase Faults)
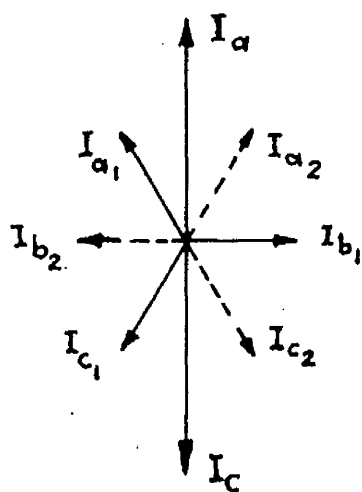
"A-C/E" Fault

(A) Double Phase Faults

(B) Double Phase/Earth Faults
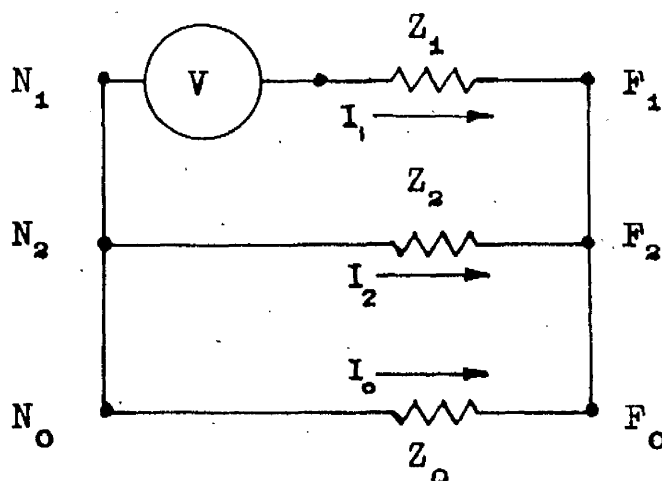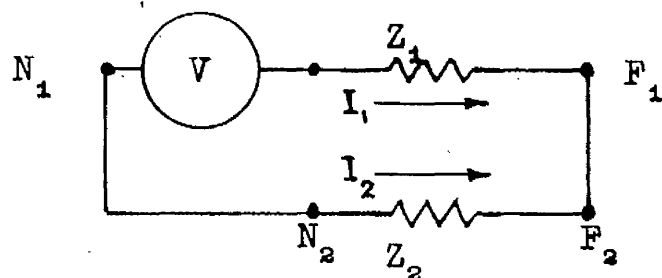
FIG. (4.4) SEQUENCE NETWORKS FOR DOUBLE PHASE/E. FAULTS.

output of S.C.T. as given by eqn (4.3) will be:-

$$I_{ST} = 3I_0 (2 + n) \qquad \qquad \ldots\ldots (4.9)$$

Substituting from eqn (4.7) for I_0 therefore,

$$I_{ST} = 3\frac{V}{Z_1} \cdot \frac{1}{1 + 2K} (2 + n) \qquad \left.\begin{array}{c} \\ \\ \\ \\ \end{array}\right\} \quad \ldots\ldots (4.10)$$

hence $\left|\dfrac{I_{ST}}{I_F}\right| = (n + 2)$

Similarly, and by reference to Fig. (4.3), it can be proved that the S.C.T. output for a phase "B"/earth fault,

$$I_{ST} = I_0 (3 + 3n) \qquad \left.\begin{array}{c} \\ \\ \\ \\ \end{array}\right\} \quad \ldots\ldots (4.11)$$

hence $\left|\dfrac{I_{ST}}{I_F}\right| = (n + 1)$

and for a phase "C"/earth fault,

$$I_{ST} = I_0 (3 + 3n) - 3I_{c_1} \qquad \left.\begin{array}{c} \\ \\ \\ \end{array}\right\} \quad \ldots\ldots (4.12)$$

hence $\left|\dfrac{I_{ST}}{I_F}\right| = n$

(b) **Phase to phase faults**

The connection of the sequence networks for a "C-A" fault, not involving earth, is shown in Fig. (4.4 A). For such fault conditions it can be seen that:-

$$I_{b_1} = -I_2 = \frac{V}{Z_1 + Z_2} = \frac{V}{2Z_1} \qquad \ldots\ldots (4.13)$$

(assuming that $Z_1 = Z_2$)

The vector relationships between the sequence component currents are also illustrated in Fig. (4.4 A), and assuming the fault current $I_F = I_c$.

Then
$$I_c = I_F = -j \sqrt{3} \, |I_1|$$
$$= -j \sqrt{3} \, \frac{V}{2Z_1} \qquad \ldots\ldots (4.14)$$

The output from the S.C.T. for such a fault, as given by eqn (4.3), will be:-

$$I_{ST} = 2(I_{a_1} + I_{a_2})$$
$$\text{hence} \left| \frac{I_{ST}}{I_F} \right| = 2 \qquad \left.\rule{0pt}{40pt}\right\} \qquad \ldots\ldots (4.15)$$

Similarly, it can be shown that for phase "A-B" and "B-C" faults that:-

$$\left| \frac{I_{ST}}{I_F} \right| = 1 \qquad \ldots\ldots (4.16)$$

(c) <u>Three phase faults.</u>

For this condition of fault the phase currents are equal, i.e.

$$I_a = I_b = I_c = I_F = I_1, \quad \text{where} \quad I_1 = V/Z_1.$$

Eqn. (4.3) for S.C.T. output will then give:-

$$I_{ST} = (2 + a^2) I_1$$
$$\text{and therefore} \left| \frac{I_{ST}}{I_F} \right| = \sqrt{3} \qquad \left.\rule{0pt}{40pt}\right\} \qquad \ldots\ldots (4.17)$$

(d) Double phase to earth faults

For the three possible cases of fault, the S.C.T. output is:-

(i) $[3(1+n) \quad (2+a^2) \quad (2+a)]$ $\begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$ for a B-C/earth fault

(ii) $[3(1+n) \quad (1+2a) \quad (1+2a^2)]$ $\begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$ for a C-A/earth fault

(iii) $[3(1+n) \quad (a+2a^2) \quad (2a+a^2)]$ $\begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$ for a B-A/earth fault

These outputs are given for the conditions of a "B-C"/earth fault applied to the various sections of the primary winding of the S.C.T.

Referring to Fig. (4.4 B), for a double phase to earth on a "B-C"/earth it can be seen that:-

$$I_b = \frac{V}{Z_1} \cdot \frac{1}{1+2K} \left[-\frac{3}{2} - j \frac{\sqrt{3}}{2} (1+2K) \right] \quad \ldots \ldots (4.18)$$

and
$$I_c = \frac{V}{Z_1} \cdot \frac{1}{1+2K} \left[-\frac{3}{2} + j \frac{\sqrt{3}}{2} (1+2K) \right] \quad \ldots \ldots (4.19)$$

where $K = \dfrac{Z_0}{Z_1} = \dfrac{Z_0}{Z_2}$

Considering the fault current $I_F = I_b$, then the output of S.C.T. for various faults is:-

For a "B-C"/earth fault,

$$I_{ST} = -\frac{V}{Z_1} \cdot \frac{1}{1+2K} \angle (\frac{3}{2} + 3n) + j \frac{\sqrt{3}}{2} (1+2K) \, \rfloor \quad \ldots \ldots (4.20)$$

Therefore

$$\frac{I_{ST}}{I_F} = 1 + \frac{2n}{1 + j(1+2K) / \sqrt{3}} \quad \ldots \ldots (4.21)$$

for a "C-A"/earth fault,

$$I_{ST} = -\frac{V}{Z_1} \cdot \frac{1}{1+2K} \angle 3(1+n) - j \sqrt{3} \, (1+2K) \, \rfloor$$

$$\ldots \ldots (4.22)$$

hence $\frac{I_{ST}}{I_F} = 2 \, (-1 + \frac{2 + n}{1 + j \frac{1+2K}{\sqrt{3}}})$ $\ldots \ldots (4.23)$

Similarly, for a "B-A"/earth fault,

$$\frac{I_{ST}}{I_F} = 1 + \frac{2(1+n)}{1 + j \frac{1+2K}{\sqrt{3}}} \quad \ldots \ldots (4.24)$$

In considering the two extreme cases of $Z_0 = jX_0$ and $Z_0 = R_0$, the magnitude $|\frac{I_{ST}}{I_F}|$ is given by the modulus of the above quantities substituting $K = -jk_1$ for the case of $Z_0 = R_0$.

In a general case, where the zero sequence impedance is composed of a resistive as well as a reactive part, the magnitude of the relaying quantity $|\frac{I_{ST}}{I_F}|$ is given by the modulus of eqns (4.21, 23 and 24), substituting K by the expression,

$$(k - jk_1) \quad \ldots \ldots (4.25)$$

4.3.3. S.C.T. Performance in Phase Comparison Protection Schemes

A basic arrangement of a S.C.T. is shown in Fig. (4.1). For a balanced three phase input the output was shown in eqn. (4.6), to correspond to $\sqrt{3}$ times the phase current and to be lagging with the reference phase current I_a by 30°.

The effect of an unbalanced input, under fault conditions, has been considered, in the previous section, giving the S.C.T. outputs expressions by using symmetrical components.

In phase comparison schemes, for feeder protection and during an external fault, neglecting the capacitive charging currents, the outputs of the S.C.T.s at the two ends of the transmission line are equal in magnitude and of opposite phase. On the occurrence of an internal fault the phase difference is reduced and should therefore cause tripping.

For single phase to earth faults the phase relationship of the S.C.T.s outputs is a function of "n" and the ratios of the balanced to zero sequence current $\int (I_1 \text{ or } I_2)/I_0 \, \rfloor$ at the two ends of the protected sections. It is an essential requirement that these considerations should not give rise to incorrect outputs and consequently wrong operation. The expressions for S.C.T. outputs during the three single phase/earth fault conditions are derived in eqns (4.10, 4.11 and 4.12). An investigation is required to determine a suitable value of "n", such that a correct output is always obtained under practical fault conditions.

For an internal single phase/earth faults the output of the S.C.T. is given by:-

(a) For a phase "A"/earth fault.

$$I_{ST} = I_0 \, (3n + 3) + 3I_{a1} \qquad \ldots \ldots (4.26)$$

In order to obtain an output of a positive polarity then,

$$I_0(3n + 3) \geqslant -3I_{a1}$$

$$\text{or} \qquad n \geqslant -\frac{I_{a1}}{I_0} - 1 \qquad \ldots \ldots (4.27)$$

Hence for all positive values of "n" the polarity is positive.

Considering the magnitude of the S.C.T. output, the minimum value of it should correspond to a 3 phase input of the per unit rated current I_R where $|I_{ST}| = \sqrt{3} \, |I_R|$ from eqn. (4.6).

Therefore,

$$I_0 \, (3n + 3) + 3I_{a1} \geqslant \sqrt{3} \, |I_R|$$

$$\text{or} \quad n \geqslant \frac{\sqrt{3} \, |I_R| - 3I_{a1}}{3I_0} - 1 \qquad \ldots \ldots (4.28)$$

(b) For a phase "B"/earth fault.

The S.C.T. output under this fault condition is given by eqn (4.11) namely:-

$$I_{ST} = I_0 \, (3n + 1)$$

For an output of a positive polarity,

$$I_0 \, (3n + 3) \geqslant 0$$

Therefore,

$$n \geqslant -1 \qquad\qquad \ldots\ldots (4.29)$$

Eqn (4.29) which gives the output of S.C.T. does not contain a positive sequence current component term, the zero sequence currents must therefore be present otherwise the output is zero for all values of "n". The presence of the zero sequence current gives the correct polarity to the output for all positive values of "n".

Considering the magnitude of the output, the minimum value of which should be equal to $\sqrt{3} \, |I_R|$.

Thus $\qquad I_0 \, (3n + 3) \geqslant \sqrt{3} \, |I_R|$

or $\qquad\qquad n \geqslant \dfrac{|I_R|}{\sqrt{3} \, I_0} - 1 \qquad \ldots\ldots (4.30)$

(c) For a phase "C"/earth faults.

Eqn (4.3) gives the output as,

$$I_{ST} = I_0 \, (3 + 3n) - 3 \, I_{c1}$$

For an output of positive polarity therefore,

$$I_0 \, (3n + 3) - 3 I_{c1} \geqslant 0$$

or $\qquad\qquad n \geqslant \dfrac{I_{c1}}{I_0} - 1 \qquad \ldots\ldots (4.31)$

Considering the minimum output to be equal to $\sqrt{3}\,|I_R|$.

Therefore,

$$I_0\,(3n + 3) - 3I_{c_1} \geqslant \sqrt{3}\ |I_R|$$

or
$$n \geqslant \frac{\sqrt{3}\ |I_R| + 3I_{c_1}}{3I_0} - 1 \qquad \ldots\ldots (4.32)$$

Fig. (4.5) shows the connection of the sequence networks for a phase/earth fault, of a transmission system with double current infeed.

It is assumed that, as in most practical cases, the positive sequence network and the negative sequence networks are identical. This assumption is justified for all equipment except rotating machinery. The vector diagram of the sequence component current is also shown in Fig (4.5).

Considering eqns (4.30, 4.31, and 4.32) it is apparent that the phase "C"/earth fault condition is the one which determines a requirement of "n",

i.e. $n \geqslant I'_{c_1}/I'_0 - 1$ or $I''_{c_1}/I''_0 - 1$ $\qquad \ldots\ldots (4.33)$

A practical ratio of balanced to zero sequence infeed at the end of a long transmission line during a single phase to earth fault at one end, can be as high as 3.5, which is a typical value of 132 K.V. double circuit lines. It can be shown from eqn (4.31) that under such conditions a S.C.T. having ratios of 1:1:2 is prone to failure. This particular ratio was used in a manufacturer's scheme
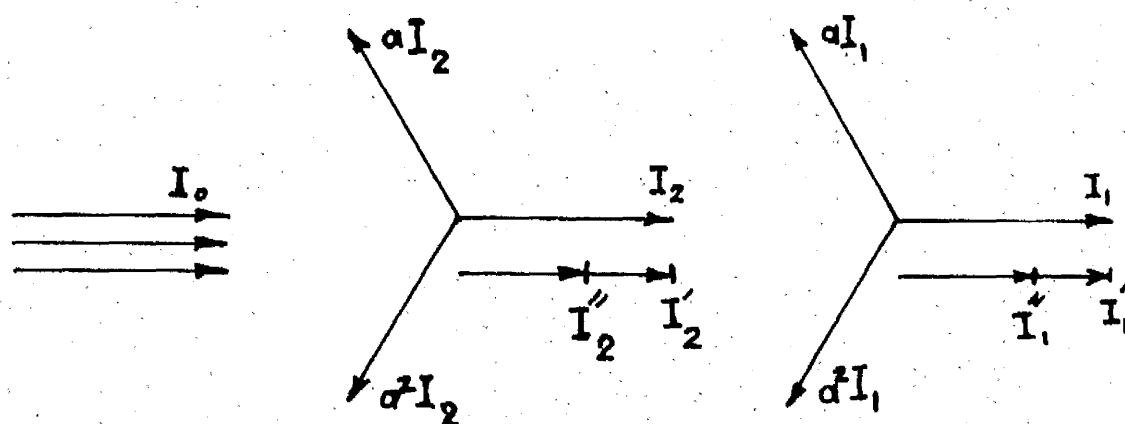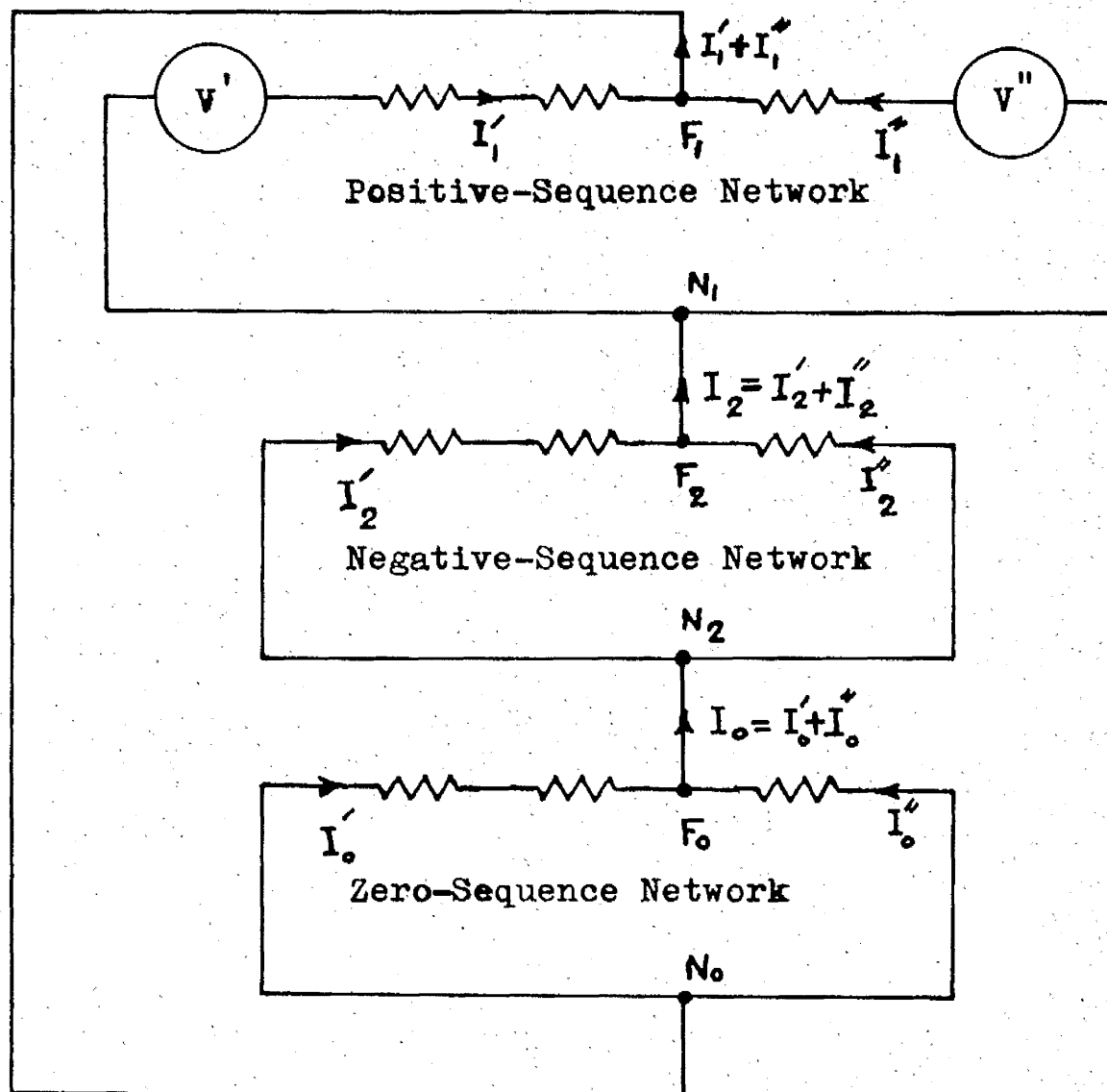
FIG. (4.5) SINGLE PHASE/EARTH FAULT ON A TRANSMISSION LINE.
(With Double Infeed)

known as "Contraphase" protection. A satisfactory turn ratios would be of at least 1:1:5.

Generally the infeed ratio of $(I_1/I_0 = 3.5)$ would be for lines greater in length than 25 miles and therefore does not necessarily apply to shorter pilot-wire schemes.

For shorter lines the ratio of balanced to zero sequence current infeed would be considerably less than 3.50.

Eqn (4.32), which states the limit for the output of S.C.T. under phase "C"/earth fault and by substituting 3.5 for the ratio of (I_1/I_0) gives:-

$$n \geqslant \frac{|I_R|}{\sqrt{3}\,|I_0|} + 2.5 \qquad \ldots\ldots (4.34)$$

For a practical case where $I_R = 500$ A, I_0'' was equal to about 130 amperes (on a double circuit 132 K.V. system), and eqn (4.24) then gives

$$n \geqslant 4.7 \qquad \ldots\ldots (4.35)$$

The case considered, with the fault being at one end of the line, was made to be a limiting case to illustrate the basic elements in the determination of the value of n.

In the above analysis no consideration has been given to the phase shift which is introduced between the zero sequence components I_0' and I_0'' , particularly of I_0' of the remote end from the fault. However, these effects are quite small in such a case. This can be better seen by considering the difference in I_1 as

given by $\left|I_f' + I_0''\right|$ and $\left|I_0' + I_0''\right|$, which was less than 5%, for the practical case considered in the analysis.

From eqn (4.35) the ratios 1:1:5 for S.C.T. would seem a reasonable minimum to operate with phase comparison schemes, thus avoiding the choice of unsuitable turn ratios which might result in having a 180° phase shift under certain internal fault conditions. It is understood that the value of $n = 5$ would be satisfactory for double phase/earth faults[9].

It is now left to the art of the designer to arrange for the "blind spots" to fall outside the normal range of system fault conditions encountered in practice. The designer should also check the suitability of the S.C.T. turn ratios for his particular system in a similar manner to that described above.

4.4. Linear Couplers Summation Arrangement to Provide Single Relaying Quantity

The other alternative of providing a single relaying quantity from a 3 phase system is by using linear coupler summation arrangement.

For three phase systems, the arrangement is very similar to the conventional S.C.T. one.

The linear couplers on the three phases have different transfer impedances; for instance, that on phase "A" may be rated at 10 V/kA, on the "B" phase at 8 V/kA, and on phase "C" at 6 V/kA, i.e. of the ratios 5:4:3. This arrangement being equivalent to having different turn ratios on the S.C.T.

All the three linear couplers, one on each phase, are connected in series and in series with the tripping relay.

A diagram of a typical arrangement with two sets of linear couplers, is shown in Fig. (4.6). It would be appropriate here to investigate the settings of the relay operated with this arrangement under different fault conditions.

(a) <u>Phase to earth faults</u>

In the above mentioned example, it is clear that the earth fault setting will be different for each phase, similar to a S.C.T. arrangement.

If the primary operating current (P.O.C.), which is the threshold operating current, for phase "A" is, say, 300 A, then that of the "B" phase will be 375 A, and 500 A for "C".

The earth fault settings may be formulated in the following manner.

If I_A, I_B, and I_C are the earth fault P.O.C. for phases A, B, and C, respectively.

Z_C, Z_B, and Z_A the transfer impedances of linear couplers and their ratios are $n : n+1 : n+2$, for phases C, B and A, respectively.

Then the minimum secondary voltage V_s required for relay operation is given by:-

$$V_s = I_A Z_A = I_B Z_A \cdot \frac{n+1}{n+2} = I_C Z_A \frac{n}{n+2} \qquad \ldots \ldots (4.36)$$

Therefore $\quad I_B = I_A \cdot \frac{n+2}{n+1}$

$\left. \begin{array}{c} \\ \\ \end{array} \right\} \qquad \ldots \ldots (4.37)$

and $\quad I_C = I_A \cdot \frac{n+2}{n}$

Tripping Relay

Bus-Bar

L.C.(1)   L.C.(2)   L.C.(3)

Feeders   F(1)   F(2)   F(3)
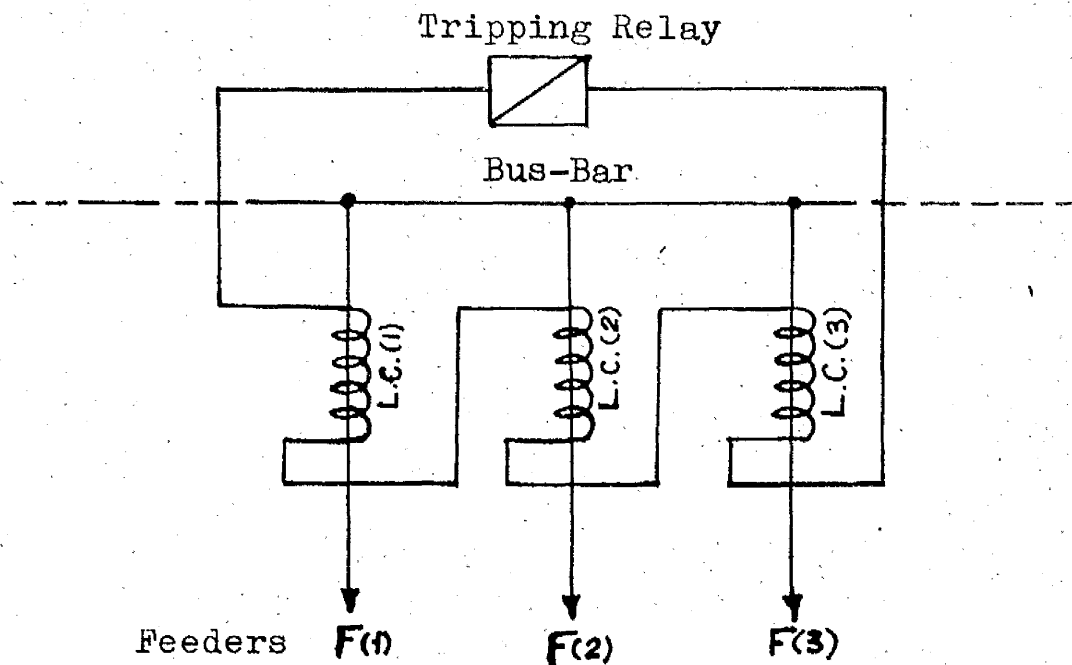
(A) Simple Summation Scheme

6V/KA

8V/KA

10V/KA

Tripping
Relay

A   B   C
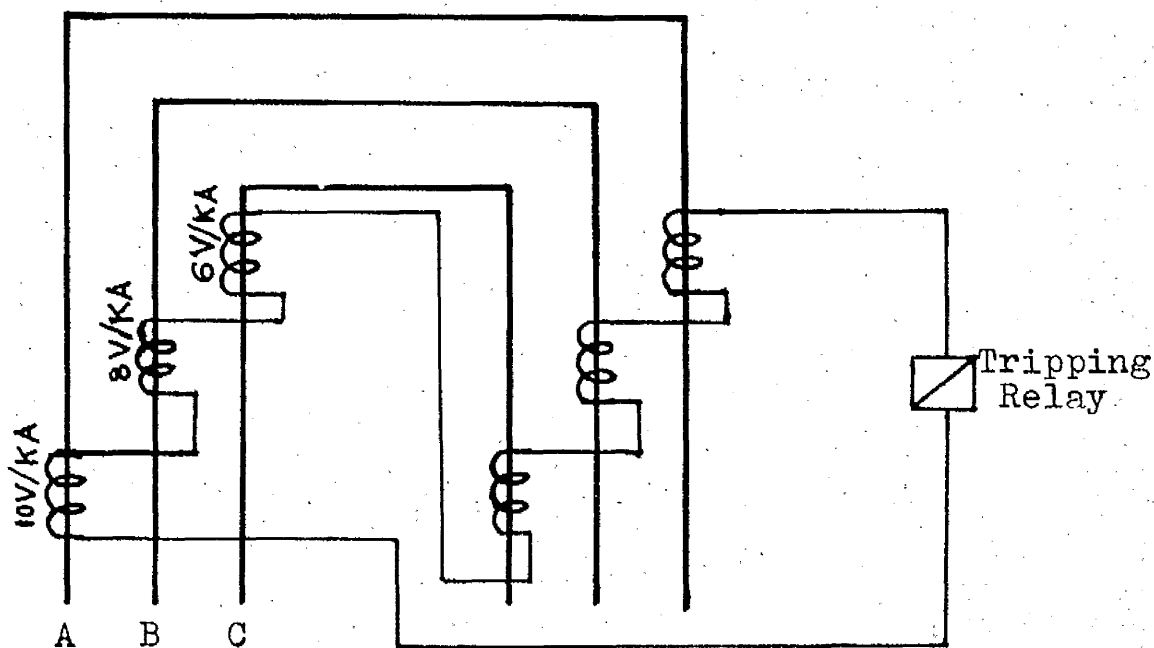
(B) Three Phase Summation Arrangement

FIG. (4.6) LINEAR COUPLER SUMMATION SCHEMES.

(b) <u>Phase to phase faults</u>.

There are only two different settings for phase/phase faults, that of "A-B" and "B-C" being the same.

Generally speaking, by referring to eqns (4.36 and 4.37), and denoting the P.O.C. by I_{AB}, for "A-B" phase/phase fault, I_{BC} for "B-C" fault, and I_{AC} for "C-A".

Then $\qquad V_s = I_A Z_A = I_{AB} \cdot Z_A \left[1 - \frac{n+1}{n+2} \right]$ $\qquad$ ..... (4.38)

since for phase faults $I_A = - I_B$ of "A-B" fault, $I_B = -I_C$ for "B-C" and $I_C = -I_A$ for "C-A" fault.

Therefore, $\qquad I_{AB} = (n+2) I_A$ $\qquad$ ..... (4.39)

Similarly, for a "B-C" fault, it can be proved that,

$$I_{BC} = I_B (n+1) \qquad\qquad ..... (4.40)$$

and for an "A-C" fault

$$I_{AC} = \frac{(n+2)}{2} I_A \qquad\qquad ..... (4.41)$$

It is clear that for the above example, if the most sensitive phase has an earth fault P.O.C. of 300 A, then "A-B" or "B-C" phase faults will have a P.O.C. of 1500 A, and "A-C" fault will have a P.O.C. of 750 A.

(c) <u>Three phase faults</u>

The calculation of the three phase setting is a little more complex than the previous cases of phase to phase faults.

Assuming that I_{ABC} is the three phase P.O.C., then from eqn (4.36) it follows:-

$$V_s = I_A Z_A = I_{ABC} \left\{ 1 + \left(\frac{n+1}{n+2}\right) a^2 + \left(\frac{n}{n+2}\right) a \right\} Z_A \ldots \ldots (4.42)$$

therefore

$$I_{ABC} = I_A \frac{(n+2)}{2+a^2} \qquad \ldots \ldots (4.43)$$

and hence

$$I_{ABC} = \frac{n+2}{\sqrt{3}} I_A \qquad \ldots \ldots (4.44)$$

Eqn (4.43) shows that I_{ABC} is leading I_A by an angle of 30°.

In the previously mentioned example, the three phase P.O.C. would be 870 A.

The above mentioned eqns (4.37, 4.38 - 4.41 and 4.43) could be expressed, as for the case of S.C.T., sec. (4.3.2.), in terms of the sequence component currents of the faulted system. However, this will generally follow the same procedure as explained before in the S.C.T. case.

4.4.1. Effect of System Configuration on P.O.C. and Stability Ratio.

(a) Primary operating current (P.O.C.)

In resistance-earthed systems, the earth-fault current level may be very low due to the earthing resistance limiting effect, say of the order of 500 A. To ensure correct tripping under exceptional circumstances, it is desirable that the primary operating current

be made less than this, e.g. about 300 A as in the example previously considered.

In solidly earthed systems, and always for multi-phase faults, a much higher setting is both permissible and desirable. A figure of about 20% of rated breaking capacity is the maximum usually chosen for the phase/phase fault settings, and about half of this for phase/earth faults.

(b) <u>Stability ratio (S.R.)</u>

The maximum through-fault current which can be cleared is fixed by the breaking capacity of the switchgear. This current level is the minimum stable limit in the case of phase/phase faults. For earth faults, the minimum level is about half of this in resistance earthed systems (the earthing resistance may flash over), but where multiple solid earthing is practiced, the minimum level is the same as for phase/phase faults.

The stability ratio, defined as the ratio between the primary current level I_p at which instability occurs and the P.O.C., is considered to represent the range of currents over which a particular scheme will operate satisfactorily. Thus the S.R. is highest for resistance earthed systems. For instance, the P.O.C. may be 300 A for phase/earth faults, and the maximum through fault current could be as high as 30 kA, giving a ratio of 100:1. In some countries, and in the U.K., in the near future, through fault current levels are as high as 60 kA, thus giving a ratio of 200:1 for the previous example.

This position has considerably worsened by some limitations of users such as the G.P.O., insisting on low earth fault settings to protect their equipment from any damage which may occur due to high earth fault currents circulating during faults on power systems. On the other hand, in multiple solidly earthed systems the maximum earth-fault through current may be of the same order of magnitude as that of phase/phase fault current.

The stability ratio, however, is determined in the case of linear couplers by the degree of accuracy to which individual coupler coils can be adjusted, sec. (3.2.3.), i.e. independent of fault current. The stability ratio (S.R.) is given by[26]:-

$$S.R. = \frac{1}{\delta} \qquad \qquad \dots \dots (4.45)$$

where "δ" is the practical error band within which all coupler coils are adjusted. This error is evaluated for a set of 3 couplers and was found to be less than 0.4%, sec. (6.2.7.).

It has been previously mentioned that the earth fault through current, for resistance earthed systems may be, at the most, one half of the phase fault through level.

Providing that the value of n, sec. (4.4.), is at least 2, the accuracy of winding the linear coupler coils need only be half of that determined theoretically by eqn (4.45).

The reason for this is that the phase/phase and three phase faults stability ratios are reduced by $(\frac{n\pm2}{2})$ and $\frac{n\pm2}{\sqrt{3}}$, respectively eqns (4.41 and 4.44), and the earth fault stability ratio is only

half that required in a solidly earthed scheme. Hence, provided that $\frac{n+2}{2} > 2$, i.e. $n > 2$, the three phase linear coupler arrangement has an effective S.R. which is only half that of a summation arrangement for a single phase case, sec. (6.2.7.).

4.4.2. Comparison with S.C.T. Arrangement

The foregoing analysis shows, that the only limit to the stability ratio attainable with linear coupler schemes is the degree of accuracy to which the toroid coil can be adjusted. Instability in iron-cored C.T. summation schemes may be caused by variation of the C.T. shunt admittance or by saturation of one or more of the C.T.s. Stability ratios of about 60:1 are attainable with iron-cored C.T.s, but for linear coupler schemes much greater ratios can be obtained.

The P.O.C. for internal faults, for the case of linear couplers arrangement, is unaltered in the presence of the highest values of through fault current. All saturation troubles associated with iron-cored schemes are absent, and there is no necessity for elaborate schemes of stabilisation, compensation, or bias, thus making this type of arrangement more attractive, from the application and financial points of view.

4.5. Conclusions

In this chapter it was attempted to indicate some of the problems associated with relaying quantities for feeder protection.

The function of relaying quantities for phase-comparison schemes have also been mentioned and arguments for the choice, in the developed scheme, of the positive and the zero phase sequence current as fault detecting quantities, or starting signals, have been put forward.

A detailed study of the summation current transformer (S.C.T.) and the equivalent connection for linear couplers was also discussed. A procedure of checking the suitability of S.C.T. turns ratio, for different system configurations, under single phase to earth faults has been described.

Summation transformers are generally satisfactory for most solidly earthed systems. But the analysis of the ironless-core C.T.s arrangement, to provide a single relaying quantity, has shown that its behaviour is far better than a S.C.T. scheme, supplied from conventional C.T.s at least as far as stability is concerned. Summation schemes operated from ironless-core C.T.s (linear couplers) have therefore advantages over the existing ones as they eliminate saturation and its associated troubles.

However, it is the opinion of the author that a similar analysis for the S.C.T. case, and its equivalent with linear couplers, for a system with double circuit lines and having double infeeds would be worth tackling on a digital computer. The effect of the mutuals of untransposed lines as well as a moving fault could also then be considered, to give a better understanding of the problems.

CHAPTER 5

ANALYSIS OF SEQUENCE CURRENTS
COMBINATIONS FOR PHASE ANGLE REPRESENTATION

5.1 Introduction

Phase sequence segregating networks have been used increasingly for selection of relaying quantities for feeder protection, particularly in conjunction with phase-comparison schemes.

Different combinations of sequence quantities are possible[9], but each combination may also have its "blind spots". It is therefore important to assess the combination most suitable as a relaying quantity.

It was previously mentioned in section (4.2.2) that the combination $(MI_{a_2} + NI_{a_1})$, as a phase representing quantity, has given satisfactory output characteristic under all possible single shunt fault conditions.

It has been also noticed that this recommended combination referred to the sequence component currents of the reference phase "a", in a phase sequence rotation given by "abc". Furthermore, the analysis given[9] was thorough and lengthy in particular for systems with reactive zero-sequence impedance only. The behaviour of such a combination has been investigated, under one type of fault conditions, for a system having a zero-sequence resistance R_0 .

However, the analysis given for the general practical case of a zero-sequence impedance $Z_0 = R_0 + jX_0$, would be inadequate to generalise and may be a little inaccurate.

All these factors lead to the necessity of further investigations for this particular combination of sequence currents as a relaying quantity, with the possibility of using combinations of sequence component currents of the different phases.

5.2 Relaying Quantities

For the purpose of the analysis given in this Chapter, three combinations are selected:-

(a) $I_{m1} = MI_{a2} \pm NI_{a1} = MI_2 \pm NI_1$

(b) $I_{m2} = MI_{a2} \pm NI_{b1}$ $\qquad$ ..... (5.1)

(c) $I_{m3} = MI_{a2} \pm NI_{c1}$

where I_1 and I_2 are the positive and negative sequence component currents of the reference phase "a", and (M and N) are coefficients.

These three different combinations $\underline{/}$ eqn. (5.1) $\underline{/}$ cover most of the possible alternatives. A positive sign is only adopted in the analysis, but in the general case of evaluating the relaying quantities either positive or negative values for N are considered.

In a three phase system with phase currents I_a, I_b and I_c,

the relationship of the symmetrical component currents of, phase "a" say, is related to the phase currents by the well known equations :-

$$I_{a_1} = \frac{1}{3}(I_a + aI_b + a^2I_c)$$

$$I_{a_2} = \frac{1}{3}(I_a + a^2I_b + aI_c) \qquad \dots\dots (5.2)$$

$$I_o = \frac{1}{3}(I_a + I_b + I_c)$$

where a and a^2 denote the operators e^{j120^o} and e^{j240^o} respectively.

Similar expressions for phases "b" and "c" could easily be derived from the relationships

$$I_{b_1} = a^2I_{a_1}, \quad I_{c_1} = a\,I_{a_1}, \quad I_{b_2} = a\,I_{a_2} \text{ and } I_{c_2} = a^2I_{a_2}$$
$$\dots\dots (5.3)$$

Substituting the values of the phase sequence currents $\underline{/}$eqns. (5.2 and 3)$\underline{/}$ in the expressions of eqn. (5.1) for the relaying quantities, it follows:-

$$I_{m_1} = \frac{1}{3}\underline{/}(M + N)I_a - I_b\left\{\left(\frac{M+N}{2}\right) + j\frac{\sqrt{3}}{2}(M - N)\right\}$$
$$- I_c\left\{\left(\frac{M+N}{2}\right) - j\frac{\sqrt{3}}{2}(M - N)\right\}\underline{/} \qquad \dots\dots (5.4)$$

$$I_{m_2} = \frac{1}{3}\underline{/}I_a\left\{\left(\frac{2M-N}{2}\right) - j\frac{\sqrt{3}}{2}N\right\} + I_b\left(\frac{2N-M}{2} - j\frac{\sqrt{3}}{2}M\right)$$
$$- I_c\left(\frac{M+N}{2}\right)\underline{/} \qquad \dots\dots (5.5)$$

$$I_{m_3} = \frac{1}{3} \underline{/} I_a \left\{ \left(\frac{2M-N}{2}\right) + j \frac{\sqrt{3}}{2} N \right\} - I_b \left\{ \left(\frac{M+N}{2}\right) + j \frac{\sqrt{3}}{2} (M + N) \right\}$$

$$+ I_c \left\{ \left(\frac{2N-M}{2}\right) + j \frac{\sqrt{3}}{2} M \right\} \underline{/} \qquad \ldots\ldots (5.6)$$

Expressions (5.4, 5 and 6) give the relaying quantities as functions of the coefficients (M and N) and the three phase currents.

The relaying quantities, derived from the segregating networks, can therefore be evaluated under various faults occurring on the power system.

5.3 Single Phase to Earth Faults

5.3.1 Phase "a"/Earth Fault

Under this fault condition, the fault current

$$I_F = I_a \qquad \text{and} \qquad I_b = I_c = 0$$

Substituting these in eqns. (5.1), taking $I_a = I_F$ and $(M/N) = \alpha$, it follows:—

$$|I_{m_1}/I_F| = (M+N)/3 = N \cdot \frac{(1 + \alpha)}{3} \qquad \ldots\ldots (5.6)$$

and

$$|I_{m_2}/I_F| = |I_{m_3}/I_F| = \frac{1}{3} (M^2 + N^2 - MN)^{1/2}$$

$$= N \cdot \frac{(1 - \alpha + \alpha^2)^{1/2}}{3} \qquad \ldots\ldots (5.7)$$

5.3.2 Phase "b"/Earth Fault

For this fault condition $I_F = I_b$ and $I_a = I_c = 0$. Substituting these conditions in eqns. (5.1), and taking $(\alpha = M/N)$, it gives:—

$$\left| I_{m_1}/I_F \right| = \left| I_{m_2}/I_F \right| = \frac{1}{3} (M^2 + N^2 - MN)^{1/2}$$

$$= N \cdot \frac{(1 - \alpha + \alpha^2)^{1/2}}{3} \qquad \cdots \cdots (5.8)$$

and

$$\left| I_{m_3}/I_F \right| = \frac{1}{3} (M + N) = N \cdot \frac{(1 + \alpha)}{3} \qquad \cdots \cdots (5.9)$$

5.3.3 Phase "c"/Earth Fault

For this case $I_F = I_c$ and $I_a = I_c = 0$. Substituting these conditions in eqns. (5.1), and following the same procedure as above, it follows :—

$$\left| I_{m_1}/I_F \right| = \left| I_{m_3}/I_F \right| = \frac{1}{3} (M^2 + N^2 - MN)^{1/2}$$

$$= N \cdot \frac{(1 - \alpha - \alpha^2)^{1/2}}{3} \qquad \cdots \cdots (5.10)$$

and

$$\left| I_{m_2}/I_F \right| = \frac{1}{3} (M + N) = N \cdot \frac{(1 + \alpha)}{3} \qquad \cdots \cdots (5.11)$$

5.4 Three Phase Faults

Under such fault conditions,

$|I_F|$ = $|I_a|$ = $|I_b|$ = $|I_c|$, and the negative sequence component of current is zero.

The three relaying quantities given by eqns. (5.1) will therefore be equal, and having an amplitude given by :-

$$|I_{m1}/I_F| = |I_{m2}/I_F| = |I_{m3}/I_F| = N \qquad \ldots\ldots (5.12)$$

5.5 Double Phase/Earth Faults

A general double phase to earth fault condition is represented in Fig.(5.1A). The connections of the sequence networks to represent such a fault condition would be complicated to some extent and a common alternative is to represent the faulted system as shown in Fig.(5.1B). This case would, in fact, represent a normal 3 phase load at points F , earthed through an impedance ZG with one phase open circuited, or a double phase/earth fault (in the case shown a "b - c"/earth) through a fault impedance Z_F and an earthing impedance Z_G . The connection of the sequence networks for the "b - c"/earth fault, is shown in Fig.(5.2A), for a system with double in feeds V' and V".

It should be noticed from the figure that the impedances Z'_0 and Z''_0 depend on the earthing connections at the two ends of the system. In the case of a transmission line they
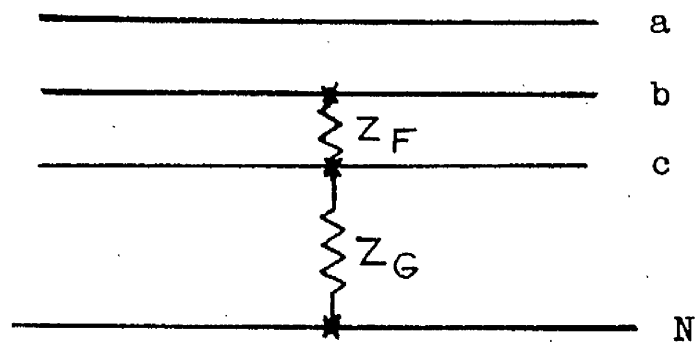
(A) General Case
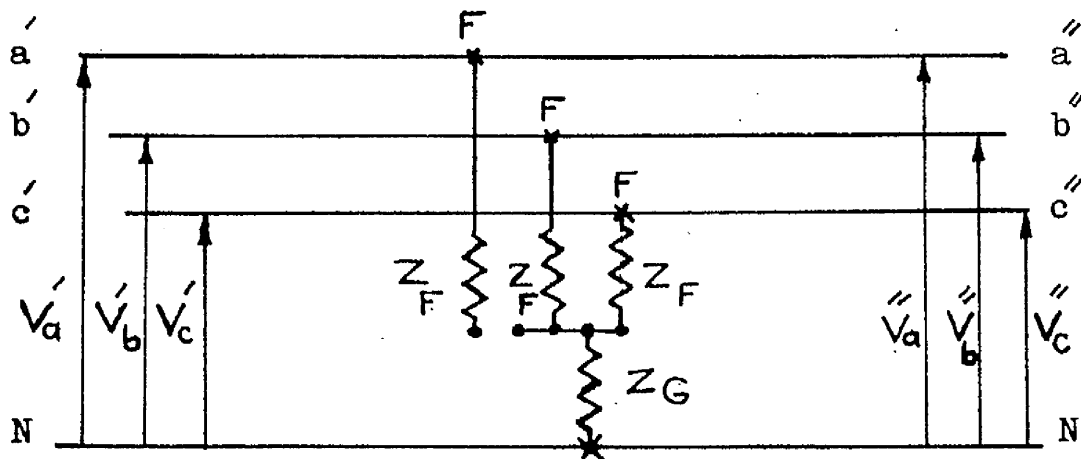
(B) Simplified Representation

FIG. (5.1) DOUBLE PHASE/EARTH FAULT.

depend on the two transformer connections, and whether they are directly earthed or earthed through a resistance. In other words, the ratio of the zero sequence currents I''_o/I'_o is governed by the impedance ratio of Z'_o/Z''_o and in the first place by the transformer connections at the line ends. A case worth mentioning is when one of the transformer connections is in delta, i.e. with no path for zero-sequence current, then either I'_o or I''_o will be zero. The importance of such a consequence would be envisaged in relation to the phase shift between the primary fault currents at the two ends, particularly if the earthing is through a resistance at the other end.

In a totally inductive system, the zero sequence currents I'_o and I''_o would be in phase but differ in magnitude as the inverse ratio of X'_o/X''_o. The inclusion of a resistive part in either Z'_o or Z''_o would result in a phase angle difference between I'_o and I''_o.

This would in turn introduce the phase angle displacement between the two primary currents, as stated above. This case has been mentioned also in Chapter 4, section (4.3.3) in connection with summation current transformers.

The connection of the sequence networks, Fig. (5.2A), could be further simplified as shown in Fig.(5.2B), by assuming that the two infeed voltages V' and V'' are in phase and of equal magnitudes.
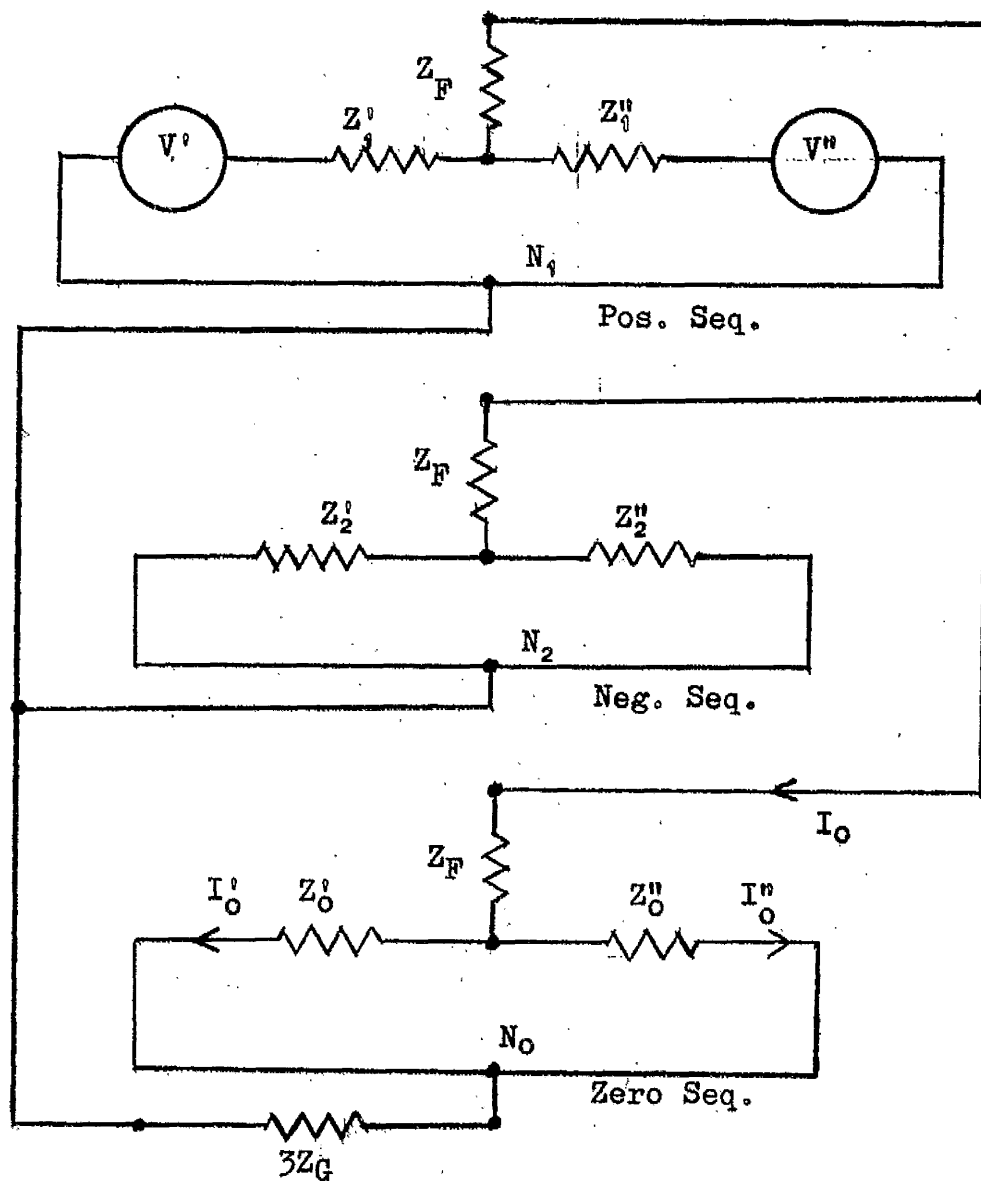
(A) Double Phase/Earth Fault ("b-c"/E)
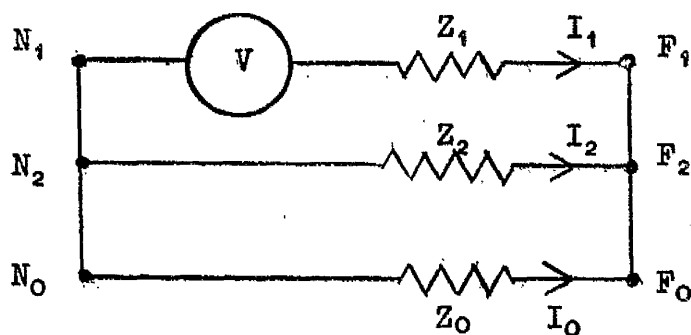
(B) Reduced Networks Connection

FIG. (5.2). SEQUENCE NETWORKS CONNECTIONS

This assumption implies the elimination of any load angle "δ" between the sources V' and V" , thus indirectly neglecting the effect of the load current. This effect could be taken into consideration[9] by superimposing the effect of the load on the fault current and thus modifying the phase angle between the primary currents.

The total effect of the load angle on the behaviour of phase comparison schemes was also analysed by Donaldson[22]. However, it was concluded[9][22] that it is only important to consider the effect of load current for systems with resistive earthing and low Q factor. A minimum stability angle of $30 - 40^{\circ}$ would be suitable for most cases.

5.5.1 Phase "b - c"/E Faults

For this fault condition $I_a = 0$.

Referring to the connections of the sequence networks for the reference phase "a", in Fig. (5.2B), it follows:-

$$I_{a_1} = I_1 = \frac{V}{Z_1} \cdot \frac{1 + K}{1 + 2K} \qquad \qquad \ldots\ldots (5.13)$$

where

$$K = \frac{Z_0}{Z_1} = \frac{Z_0}{Z_2}$$

It is assumed that both the positive and negative sequence impedances are equal. This assumption is generally justified for transmission lines and transformers but not for rotating machinery

which form a minor part of the total impedance of a power system.

Also, $I_{a2} = I_2 = -\frac{V}{Z_1} \cdot \frac{K}{1 + 2K}$ ..... (5.14)

and $I_{ao} = I_0 = \frac{V}{Z_1} \cdot \frac{1}{1 + 2K}$ ..... (5.15)

Substituting eqns. (5.13, 14 and 15) in eqns. (5.1) for the relaying quantities, it can be proved that :-

$$I_{m1} = MI_{a2} + NI_{a1}$$

$$= N \cdot \frac{V}{Z_1} \cdot \frac{(1 - \alpha)K + 1}{1 + 2K} \qquad ..... (5.16)$$

where

$$\alpha = (M/N)$$

Similarly,

$$I_{m2} = MI_{a2} + NI_{b1}$$

$$= N \cdot \frac{V}{Z_1} \cdot \frac{- \alpha K + a^2 (1 + K)}{1 + 2K} \qquad ..... (5.17)$$

and

$$I_{m3} = MI_{a2} + NI_{c1}$$

$$= N \cdot \frac{V}{Z_1} \cdot \frac{K(a - \alpha) + a}{1 + 2K} \qquad ..... (5.18)$$

Either I_b or I_c can be considered as the fault current I_F. As far as the protective gear is concerned the current in these two phases represents the fault current. The protective gear, therefore, sees I_F as the current in the secondary circuits

of the C.T.s at each end. In the simplified case, in Fig. (5.2B), with only one equivalent generation V, the phase current I_b (say) would be equal I_F.

From the symmetrical components relationship eqns. (5.2 and 3) would then be $I_b = I_0 + a^2 I_{a1} + a I_{a2}$, and substituting for I_0, I_{a1} and I_{a2} from eqns. (5.13, 14 and 15), it follows:-

$$I_F = I_b = -\frac{V}{Z_1} \cdot \frac{1}{1 + 2K} \cdot \frac{\sqrt{3}}{2} \left\{ \sqrt{3} + j(1 + 2K) \right\} \quad \ldots \ldots \quad (5.19)$$

Initially it will be assumed, for the sake of simplicity, that $Z_1 = Z_2 = jX_1$ and the zero sequence impedance $Z_0 = jX_0$. In practical cases Z_0 generally consists of a large resistive component R_0 and its effect will be considered in a later stage of the analysis in section (5.7).

The above assumption, also, implies that the ratio K, given as $\frac{Z_0}{Z_1}$ or $\frac{Z_0}{Z_2}$, is a scalar quantity.

When the effect of R_0 is considered, K would normally be a complex quantity rather than a scalar one.

Taking the case where K is a scalar quantity, the magnitude of the relaying quantities, as given by eqns. (5.1), and expressed as ratios of the fault current, eqn. (5.19), would be given by:-

$$\left| I_{m1}/I_F \right| = \frac{N}{\sqrt{3}} \cdot \frac{1 + (1 - \alpha)K}{(1 + K + K^2)^{1/2}} \quad \ldots \ldots \quad (5.20)$$

$$\left| I_{m2}/I_F \right| = \frac{N}{\sqrt{3}} \cdot \frac{\left\{ K^2(1 + \alpha + \alpha^2) + K(2 + \alpha) + 1 \right\}^{1/2}}{(1 + K + K^2)^{1/2}}$$

$$\dots \dots (5.21)$$

and similarly,

$$\left| I_{m3}/I_F \right| = \frac{N}{\sqrt{3}} \cdot \frac{\left\{ K^2(1 + \alpha + \alpha^2) + K(2 + \alpha) + 1 \right\}^{1/2}}{(1 + K + K^2)^{1/2}}$$

$$\dots \dots (5.22)$$

The results obtained above could be better understood from the symmetrical components vector diagram to show their relative phase displacement for the fault under consideration. For the totally reactive system assumed before with $R_0 = 0$ and $Z_0 = jX_0$, all the sequence component currents are in phase. Referring to Fig. (5.3A), it could be seen that $(I_0 + I_{a2})$ are in antiphase with I_{a1}.

The effect of different transformer connections, if any, at the ends of the line could be more demonstrated by assuming a delta connection at one end and an earthed star at the other. Such a case would result in different zero sequence currents namely either I'_0 or I''_0 will be zero at the delta connected side, e.g. I''_0. At this end, (2), of the line the sequence components vector relationship would be as shown in Fig.(5.3B). The negative sequence current I''_{a2} is therefore equal and 180° out of phase with respect to the positive sequence component I''_{a1}. Under such a case the choice of $N = + 1$ for the relaying quantity $I''_{m1} = MI''_{a2} + NI''_{a1}$, imposes a criterion
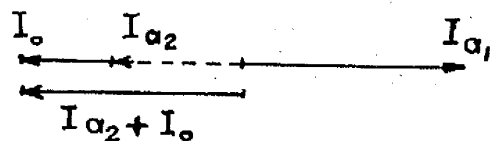
(A) "b-c"/E Fault ($R_o = 0$)
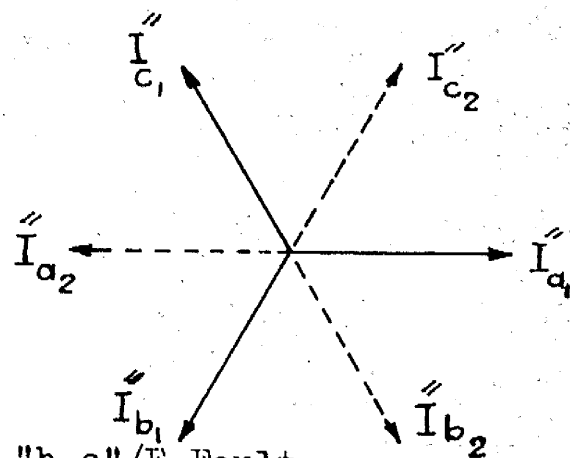
(B) "b-c"/E Fault
Transf. of End(2) Delta Connected
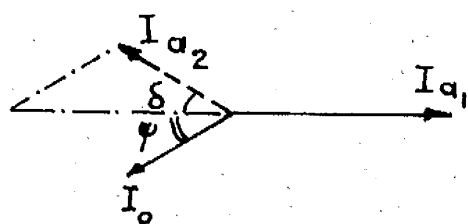
(C) "b-c"/E Fault ($R_o \neq 0$)
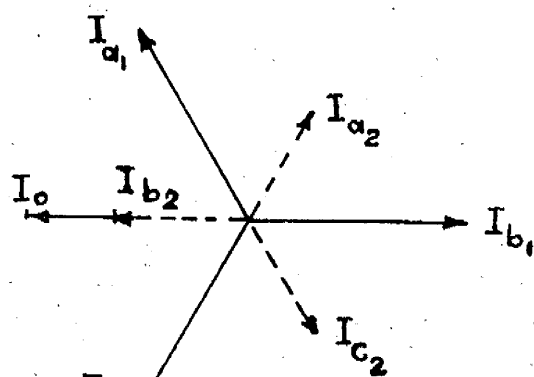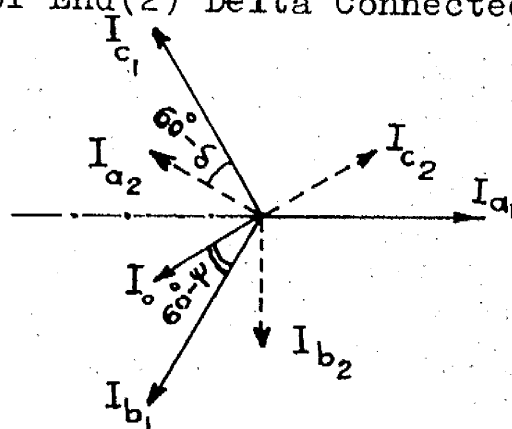
"c-a"/E Fault

"a-b"/E Fault

(D) Reactive System ($R_o = 0$)
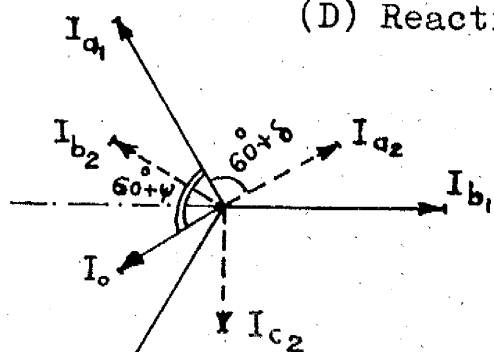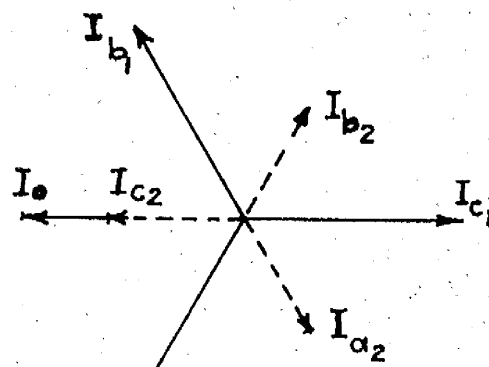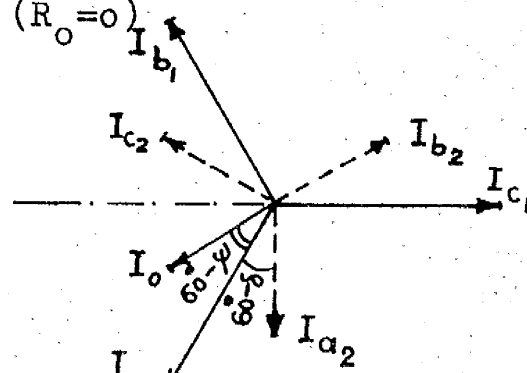
"c-a"/E Fault

"a-b"/E Fault

(E) $R_o \neq 0$

FIG. (5.3) SEQUENCE COMPONENTS FOR DOUBLE PHASE/EARTH FAULTS.

for M to be greater than one.

It can be easily seen from Fig. (5.3B) that the relaying
quantities given by eqns. (5.1) would give equal magnitudes, for
end (2) under this fault condition.

In the general practical case of a system having a considerable
resistive part in its zero sequence impedance, i.e. $R_0 = 0$, a
phase shift between the sequence component currents will be
introduced. The sequence component current, for the reference
phase "a," are then no longer in antiphase.

The relationship $I_a = I_0 + I_{a_1} + I_{a_2}$, will be still valid
and therefore the vector diagram will be as shown in Fig. (5.3C).
The values of I_{a_1} , I_{a_2} , and I_0 are still as given by eqns.
(5.13, 14, and 15), but the ratio $\dfrac{Z_0}{Z_1} = \dfrac{Z_0}{Z_2} = K$ would be a
complex quantity. A complete analysis of this case follows
later in section (5.7).

5.5.2 Phase "a - b"/E and "c - a"/E Faults

Before persuing the analysis any further, it is helpful
at this stage to draw the symmetrical components vector
relationships under such fault conditions. Fig. (5.3D) illustrates
this relationship for, as previously assumed, a totally reactive
system $(R_0 = 0)$. From Fig. (5.3D) it is seen that for
"a - b"/E fault I_{a_2} leads I_{a_1} by 60° and I_0 lags behind
I_{a_1} by a similar angle. For "c - a"/E fault I_{a_2} lags

behind I_{a_1} by 60° and I_0 also leads I_{a_1} by 60°.

If the effect of the zero sequence resistance R_0 has to be considered, the consequence of modifying the phase angle between the sequence components of phase "a" is shown in Fig. (5.3E) for both "a - b"/E and "c - a"/E faults.

The detailed analysis of this case is also given later in this chapter $\sqrt{}$ section (5.7) $\sqrt{}$.

Referring back to eqns. (5.1) for the relaying quantities, and assuming a completely reactive system, then for "a - b"/E fault it follows:-

$$I_{m_1} = MI_{a_2} + NI_{a_1}$$

$$= a. \frac{V}{Z_1} \cdot \frac{1}{1 + 2K} \cdot \frac{-N}{2} \sqrt{} (2\alpha K + K + 1) - j \sqrt{3} (1 + K) \sqrt{}$$

$$\cdots\cdots (5.23)$$

Following the same argument as before either I_a or $I_b = |I_F|$, since the current in the faulty phases represent the fault current as far as the protective gear is concerned.

From the symmetrical components, eqns. (5.2 and 3), and from the vector relationship for "a - b"/E fault, Fig. (5.3D), it follows:-

$$I_b = I_0 + aI_{o_1} + a^2I_{o_2} = I_F$$

$$= \frac{V}{Z_1} \cdot \frac{1}{1 + 2K} \cdot \frac{1}{2} \sqrt{} - 3 + j \sqrt{3} (1 + 2K) \sqrt{}$$

$$\cdots\cdots (5.24)$$

Therefore,

$$|I_{m_1}/I_F| = |I_{m_3}/I_F| =$$

$$= N \cdot \frac{\left[1 + K^2(\alpha^2 + \alpha + 1) + K(2 + \alpha) \right]^{1/2}}{\sqrt{3} \; (1 + K + K^2)^{1/2}}$$

$$\ldots\ldots \quad (5.25)$$

and

$$|I_{m_2}/I_F| = N \cdot \frac{(1 - \alpha) K + 1}{\sqrt{3} \; (1 + K + K^2)^{1/2}} \qquad \ldots\ldots \quad (5.26)$$

It can be shown from the symmetry of the vectors in Fig. (5.3D), that identical expressions for I_{m_1}, I_{m_2}, and I_{m_3} are expected for the relaying quantities under "c - a"/E fault. It is also worth pointing out that the three relaying quantities have attained the two possible values under one fault condition which will be attained for any particular one of them under different fault conditions. This in fact has demonstrated the principle that the chosen relaying quantities could be equivalent in behaviour to choosing one relaying and considering its value under different fault conditions or vice versa. The system behaviour could then be studied by considering two relaying quantities under one fault condition as shown in Table (5.1).

5.6 Double Phase Faults (Not Involving Earth)

5.6.1 "b - c" Fault

For this fault condition,

$$I_a = 0 \ , \quad I_b = - I_c = I_F$$

Substituting these conditions in eqns. (5.1) for the relaying quantities, it follows that :-

$$\left| I_{m1}/I_F \right| \ = \ N. \frac{(1 + \alpha^2 - 2\alpha)^{1/2}}{\sqrt{3}} \qquad \ldots\ldots (5.27)$$

Similarly,

$$\left| I_{m2}/I_F \right| \ = \ \left| I_{m3}/I_F \right| \ = \ N. \frac{(1 + \alpha + \alpha^2)^{1/2}}{\sqrt{3}} \qquad \ldots\ldots (5.28)$$

5.6.2 "a - b" or "c - a" Faults

Considering the case of "a - b" fault, then

$$I_c = 0 \ , \quad I_a = I_F = - I_b$$

Substituting in eqns. (5.1) it gives:-

$$\left| I_{m1}/I_F \right| \ = \ \left| I_{m3}/I_F \right| \ = \ N. \frac{(1 + \alpha + \alpha^2)^{1/2}}{\sqrt{3}} \qquad \ldots\ldots (5.29)$$

and

$$\left| I_{m2}/I_F \right| \ = \ N. \frac{(1 + \alpha^2 - 2\alpha)^{1/2}}{\sqrt{3}} \qquad \ldots\ldots (5.30)$$

As previously mentioned it could be seen that identical expressions are obtained for the relaying quantities under

"c - a" faults.

In fact the results obtained above show, as in Table (5.1), that two of the three relaying quantities attain two possible values under one fault condition. This is in effect equal to the fault condition being changed for a particular relaying quantity.

5.7 The Effect of Resistance in the Zero-Sequence Impedance

In the analysis given above the zero-sequence impedance has so far been assumed purely reactive having a value $j\,X_0$. As a general case the zero-sequence impedance, in practice, is composed of a large resistive part R_0 and a comparatively small reactive part jX_0, i.e. in the form $Z_0 = R_0 + jX_0$. This assumption leads to the consequence that the ratio Z_0/Z_1 is a complex quantity rather than a simple scalar one. Since Z_1 is mostly reactive and equal to jX_1 say, therefore,

$$Z_0/Z_1 \;=\; \frac{R_0}{jX_1} + \frac{jX_0}{jX_1} \;=\; \frac{X_0}{X_1} - j\,\frac{R_0}{X_1}$$

$$=\; k - jk_1 \qquad\qquad\qquad \ldots\ldots (5.31)$$

where $\qquad k = \dfrac{X_0}{X_1} = \dfrac{X_0}{X_2}\qquad$ and $\qquad k_1 = \dfrac{R_0}{X_1} = \dfrac{R_0}{X_2}$

Considering different fault conditions, as previously described, and substituting eqn. (5.31) for Z_0/Z_1 it follows:-

5.7.1 Phase "b - c"/Earth Fault

$$I_{a_1} = I_1 = \frac{V}{Z_1} \cdot \frac{1 + k - jk_1}{1 + 2k - 2jk_1} \qquad \ldots\ldots \ (5.32)$$

$$I_{a_2} = I_2 = -\frac{V}{Z_1} \cdot \frac{k - jk_1}{1 + 2k - 2jk_1} \qquad \ldots\ldots \ (5.33)$$

$$I_0 = -\frac{V}{Z_1} \cdot \frac{1}{1 + 2k - 2jk_1} \qquad \ldots\ldots \ (5.34)$$

Substituting these currents in eqns. (5.1), for the relaying quantities, it can be proved that:-

$$I_{m_1} = \frac{V}{Z_1} \cdot \frac{N}{1 + 2k - 2jk_1} \left[1 + k(1 - \alpha) - jk_1(1 - \alpha) \right]$$
$$\ldots\ldots \ (5.35)$$

where

$$\alpha = (M/N)$$

Similarly,

$$I_{m_2} = -\frac{V}{Z_1} \cdot \frac{N/2}{1 + 2k - 2jk_1} \left[2\alpha k + (1 + k + \sqrt{3}\, k_1) \right.$$
$$\left. - j\left\{ 2\alpha k_1 + (k_1 - \sqrt{3}k - \sqrt{3}) \right\} \right]$$
$$\ldots\ldots \ (5.36)$$

$$\text{and} \quad I_{m_3} = -\frac{V}{Z_1} \cdot \frac{N/2}{1 + 2k - j2k_1} \left[2\alpha k + (1 + k - \sqrt{3}k_1) \right.$$
$$\left. - j\left\{ 2\alpha k_1 + (k_1 + \sqrt{3}k + \sqrt{3}) \right\} \right]$$
$$\ldots\ldots \ (5.37)$$

Following the same argument as before by considering either I_b or I_c as the fault current I_F and substituting for the symmetrical component currents eqns. (5.32, 33 and 34) it follows:-

$$I_F = I_b = -\frac{V}{Z_1} \cdot \frac{\sqrt{3}/2}{1 + 2k - 2jk_1}$$

$$\left[(\sqrt{3}) \, 2k_1) + j(1 + 2k) \right] \quad \ldots \ldots \quad (5.38)$$

Expressing the relaying quantities as ratios of the fault current it gives:-

$$|I_{m_1}/I_F| = \frac{N \left[1 + (1 - \alpha)^2(k_1^2 + k^2) + 2k(1 - \alpha) \right]^{1/2}}{\sqrt{3} \left[1 + (k_1^2 + k^2) + (k + \sqrt{3} \, k_1) \right]^{1/2}}$$

$$\ldots \ldots \quad (5.39)$$

Similarly,

$$|I_{m_2}/I_F| = \frac{N \left[(1 + \alpha + \alpha^2)(k_1^2 + k^2) + k(2 + \alpha) - \sqrt{3} \, k_1 \alpha + 1 \right]^{1/2}}{\sqrt{3} \left[1 + (k_1^2 + k^2) + (k + \sqrt{3} \, k_1) \right]^{1/2}}$$

$$\ldots \ldots \quad (5.40)$$

and

$$|I_{m_3}/I_F| = \frac{N \left[(1 + \alpha + \alpha^2)(k_1^2 + k^2) + k(2 + \alpha) + \sqrt{3} \, \alpha k_1 + 1 \right]^{1/2}}{\sqrt{3} \left[1 + (k_1^2 + k^2) + (k + \sqrt{3} \, k_1) \right]^{1/2}}$$

$$\ldots \ldots \quad (5.41)$$

Comparing the expressions for I_1 and I_2 when R_o is neglected, eqns. (5.13 and 14), with the corresponding one

when R_0 is considered eqns. (5.32 and 33), it could be seen that in the former case I_2 is 180° out of phase with I_1, while in the latter case the phase relation of I_2 with respect to I_1 is given by:-

$$\delta = \sqrt{\tan^{-1} \frac{k_1}{1+k} - \tan^{-1} \frac{k_1}{k}} \quad \cdots \cdots \quad (5.42)$$

Referring to Fig. (5.30) and comparing eqns. (5.13) and (5.34), for I_0, it could be seen that I_0 in the second case is leading by an angle given by:-

$$\psi = \tan^{-1} \frac{2k_1}{1+2k} \quad \cdots \cdots \quad (5.43)$$

Also from the vector relationships, Fig. (5.3D), it can be shown that under these fault conditions, I_{m_3} would give, (for positive values of N), a relaying quantity larger than that of I_{m_2} because I_{a_2} is lagging the 180° position by an angle δ.

5.7.2 Phase "a - b"/Earth and "c - a"/Earth Faults

For the "a - b"/E fault conditions $I_c = 0$, I_a or I_b would represent the fault current as far as the protective gear is concerned.

The symmetrical component currents of phase "c" are given by eqns. (5.32, 33 and 34) namely:-

$$I_{c_1} = I_1 = \frac{V}{Z_1} \cdot \frac{1 + k - jk_1}{1 + 2k - 2jk_1}$$

$$I_{c_2} = I_2 = -\frac{V}{Z_1} \cdot \frac{k - jk_1}{1 + 2k - 2jk_1} \qquad \cdots\cdots (5.44)$$

$$I_0 = -\frac{V}{Z_1} \cdot \frac{1}{1 + 2k - 2jk_1}$$

The vector relationship of I_{c_1}, I_{c_2} and I_0 is shown in Fig. (5.3E).

Substituting eqns. (5.44) in eqns. (5.1) for the relaying quantities it follows:-

$$I_{m_1} = a(MI_{c_2} + NI_{b_1}) \qquad \cdots\cdots (5.45)$$

Eqn. (5.45) gives in fact a relaying quantity having a magnitude equal to that of I_{m_3} under "b - c"/E fault, given by eqn. (5.37), and has a phase shift of 120^0.
Therefore,

$$I_{m_1} = a. \frac{-V}{Z_1} \cdot \frac{N/2}{1 + 2k - 2jk_1}$$

$$\underline{/}2\alpha k + (1 + k - \sqrt{3}k_1) - j\left\{ 2\alpha k_1 + (k + \sqrt{3}k + \sqrt{3}) \right\}\underline{/}$$

$$\cdots\cdots (5.46)$$

The fault current is taken as $I_b = I_F$, and by substituting eqns. (5.44), for the component currents, it can be shown that :-

$$I_b = I_F = I_o + a I_{c_1} + a^2 I_{c_2}$$

$$= \frac{V}{Z_1} \cdot \frac{1/2}{1 + 2k - 2jk_1} \left[-3 + 2\sqrt{3}\, k_1 + j\sqrt{3}\,(1 + 2k) \right] \qquad \ldots\ldots (5.47)$$

Expressing the relaying quantities, eqns. (5.1), as ratios of the fault current I_F it gives:-

$$\left| I_{m_1}/I_F \right| = \frac{N \left[(1 + \alpha + \alpha^2)(k_1{}^2 + k^2) + k(\alpha + 2) + \sqrt{3}\,\alpha k_1 + 1 \right]^{1/2}}{\sqrt{3} \left[1 + k_1{}^2 + k^2 + k - \sqrt{3}\, k_1 \right]^{1/2}}$$

$$\ldots\ldots (5.48)$$

Following a similar way, the two other relaying quantities give:-

$$\left| I_{m_2}/I_F \right| = \frac{N \left[1 + (1 - \alpha)^2 (k_1{}^2 + k^2) + 2k(1 - \alpha) \right]^{1/2}}{\sqrt{3} \left[1 + (k^2 + k_1{}^2) + (k - \sqrt{3}\, k_1) \right]^{1/2}}$$

$$\ldots\ldots (5.49)$$

and

$$\left| I_{m_3}/I_F \right| = \frac{N \left[(1 + \alpha + \alpha)(k_1{}^2 + k^2) + k(2 + \alpha) - \sqrt{3}\,\alpha k_1 + 1 \right]^{1/2}}{\sqrt{3} \left[1 + (k_1{}^2 + k^2) + (k - \sqrt{3}\, k_1) \right]^{1/2}}$$

$$\ldots\ldots (5.50)$$

From these general expressions (5.48, 49 and 50), it is easily seen that the relaying quantities for the case of a totally reactive system, i.e. $R_o = 0$, can be obtained by putting $k_1 = 0$. The previously investigated cases, sections (5.5) and (5.6) for reactive systems would represent a special case of the general

case treated in this section.

For the case of "c - a"/E fault:-

$I_b = 0$, I_a or I_c would represent I_F as seen by the
protective gear. The symmetrical component currents, I_{b_1} , I_{b_2}
and I_o , of the healthy phase are given by eqns. (5.44) and
their vector relationship is as shown in Fig. (5.3E).

The relaying quantities, under such a fault condition, would
give the following expressions when expressed as ratios of the
fault current I_F :-

$$\left| I_{m_1}/I_F \right| = \frac{N \left[(k_1^2 + k^2)(1 + \alpha + \alpha^2) + k(2 + \alpha) - \sqrt{3} \, \alpha k_1 + 1 \right]^{1/2}}{\sqrt{3} \left[1 + k_1^2 + k^2 + k - \sqrt{3} \, k_1 \right]^{1/2}}$$

$$\ldots\ldots (5.51)$$

Similarly,

$$\left| I_{m_2}/I_F \right| = \frac{N \left[(k_1^2 + k^2)(1 + \alpha + \alpha^2) + k(2 + \alpha) + \sqrt{3} \, \alpha k_1 + 1 \right]^{1/2}}{\sqrt{3} \left[1 + k_1^2 + k^2 + k - \sqrt{3} \, k_1 \right]^{1/2}}$$

$$\ldots\ldots (5.52)$$

and

$$\left| I_{m_3}/I_F \right| = \frac{N \left[1 + (1 - \alpha)^2 (k_1^2 + k^2) + 2k(1 - \alpha) \right]^{1/2}}{\sqrt{3} \left[1 + (k_1^2 + k^2) + k - \sqrt{3} \, k_1 \right]^{1/2}}$$

$$\ldots\ldots (5.53)$$

Eqn. (5.53), could be seen to be equal to that of
I_{m_2}/I_F for a - b/E fault, i.e. eqn. (5.49).

5.8 Effect of Varying M in Magnitude and N in Sign

on the Relaying Quantities

The relaying quantities I_{m_1}, I_{m_2}, and I_{m_3} expressed as fractions of the fault current, under different fault conditions, were discussed in detail in the previous section. In order to get a better understanding of the behaviour of these quantities for different power systems, it was necessary to calculate their values for practical cases.

In this section the effect of the ratio "α" = (M/N), on the magnitude of the relaying quantity will be evaluated for different fault conditions on the power system.

Generally speaking N, the coefficient of the positive sequence component, will be taken either (+ 1 or - 1) and the ratio "α" would vary over a wide, but practical, range of values.

The value of the relaying quantities taken as a variable, expressed in the form of $|I_m/I_F| /_N$ would be evaluated against α .

5.8.1. Single Phase to Earth Faults

The expressions obtained before for the relaying quantities under such fault conditions are given below:-

Relaying Quantity	Single phase/Earth fault		
	a/E	b/E	c/E
$\dfrac{\lvert I_{m_1}/I_F \rvert}{N}$	$\dfrac{(1 + \alpha)}{3}$	$\dfrac{(1 + \alpha^2 - \alpha)^{1/2}}{3}$	$\dfrac{(1 + \alpha^2 - \alpha)^{1/2}}{3}$
$\dfrac{\lvert I_{m_2}/I_F \rvert}{N}$	$\dfrac{(1 + \alpha^2 - \alpha)^{1/2}}{3}$	$\dfrac{(1 + \alpha^2 - \alpha)^{1/2}}{3}$	$\dfrac{(1 + \alpha)}{3}$
$\dfrac{\lvert I_{m_3}/I_F \rvert}{N}$	$\dfrac{(1 + \alpha^2 - \alpha)^{1/2}}{3}$	$\dfrac{(1 + \alpha)}{3}$	$\dfrac{(1 + \alpha^2 - \alpha)^{1/2}}{3}$

TABLE (5.1)

Fig. (5.4A) gives the variations of these relaying quantities under such fault conditions for values of α varying from ± 2 to ± 16. Such a wide range of values, larger than what is required in practice, was only considered for the sake of illustration.

Table (5.1), in fact, comprises only two expressions, namely

$$\text{Exp.(1)} = \frac{1 + \alpha}{3} \quad \text{and} \quad \text{Exp.(2)} = \frac{(1 + \alpha^2 - \alpha)^{1/2}}{3}$$

Expressions (1) and (2) give the magnitude of the relaying quantities, for values of $N = \pm 1$, expressed as a ratio of the fault current.

$$\text{EXP. } (1) = \frac{1+\alpha}{3}$$

$$\text{EXP. } (2) = \left(\frac{1+\alpha^2-\alpha}{3}\right)^{1/2}$$

$$\text{EXP.}(3) = \frac{(1+\alpha^2+\alpha)^{1/2}}{\sqrt{3}}$$

$$\text{EXP.}(4) = \frac{(1+\alpha^2-2\alpha)^{1/2}}{\sqrt{3}}$$

(A) Single Phase to Earth Faults
(B) Double Phase Faults

FIG. (5.4)   EVALUATION OF RELAYING QUANTITIES.

From Fig. (5.4A), it can be seen that exps. (1) and (2) have linear relation with "α". Exp. (1) gives higher outputs than exp. (2) for positive values of "α", while exp. (2) gives higher output for negative "α".

5.8.2 For Double Phase Faults (Not Involving Earth)

The expressions for the relaying quantities previously obtained in section (5.6) could be summarised as in Table (5.2):-

Relaying Quantity	Phase to phase faults (not involving Earth)	
	"b − c"	"a − b" or "c − a"
$\dfrac{\lvert I_{m_1}/I_F \rvert}{N}$	$\dfrac{(1 + \alpha^2 - 2\alpha)^{1/2}}{\sqrt{3}}$	$\dfrac{(1 + \alpha^2 + \alpha)^{1/2}}{\sqrt{3}}$
$\dfrac{\lvert I_{m_2}/I_F \rvert}{N}$	$\dfrac{(1 + \alpha^2 + \alpha)^{1/2}}{\sqrt{3}}$	$\dfrac{(1 + \alpha^2 - 2\alpha)^{1/2}}{\sqrt{3}}$
$\dfrac{\lvert I_{m_3}/I_F \rvert}{N}$	$\dfrac{(1 + \alpha^2 + \alpha)^{1/2}}{\sqrt{3}}$	$\dfrac{(1 + \alpha^2 + \alpha)^{1/2}}{\sqrt{3}}$

TABLE (5.2)

Fig. (5.4B) gives the evaluation of the relaying quantities under such faults for values of "α" varying from ± 2 to ± 16. This range would be generally greater than any choice suitable for practical applications.

Table (5.2) contains, in fact, only two expressions for all possible double phase faults, namely Exp. (3) $= \frac{(1 + \alpha^2 + \alpha)^{1/2}}{\sqrt{3}}$ and Exp. (4) $= \frac{(1 + \alpha^2 - 2\alpha)^{1/2}}{\sqrt{3}}$.

Fig. (5.4B) gives the magnitude of the relaying quantities evaluates, for $N = \pm 1$, expresses as ratios of the fault current. Both Exps. (3) and (4) give linear characteristics against "α".

Exp. (3) gives higher output than Exp. (4) for positive values of "α", while expression (4) gives the higher values with "α" being negative.

5.8.3 Double Phase/Earth Faults

The analysis of such fault conditions, previously described in sections (5.5) and (5.7), was conducted on 2 stages. In the first part only a totally reactive system was considered with the assumptions that $Z_1 = Z_2 = jX_1$, the zero sequence impedance $Z_0 = jX_0$, and where $K = \frac{jX_0}{jX_1} = \frac{jX_0}{jX_2}$.

The expressions obtained for evaluating the relaying quantities, under such fault conditions, could be summarised as shown in the following table:-

Relaying Quantity	Double Phase/Earth faults	
	b − c/E	a − b/E or c − a/E
$\dfrac{\lvert I_{m_1}/I_F\rvert}{N}$	$\dfrac{1 + (1 - \alpha)K}{\sqrt{3}\,(1 + K + K^2)^{1/2}}$	$\dfrac{[1+(1+\alpha+\alpha^2)K^2+K(2+\alpha)]^{1/2}}{\sqrt{3}\,(1 + K + K^2)^{1/2}}$
$\dfrac{\lvert I_{m_2}/I_F\rvert}{N}$	$\dfrac{[1+(1+\alpha+\alpha^2)K^2+K(2+\alpha)]^{1/2}}{\sqrt{3}\,(1 + K + K^2)^{1/2}}$	$\dfrac{1 + (1 - \alpha)K}{\sqrt{3}\,(1 + K + K)^{1/2}}$
$\dfrac{\lvert I_{m_3}/I_F\rvert}{N}$	$\dfrac{[1+(1+\alpha+\alpha^2)K^2+K(2+\alpha)]^{1/2}}{\sqrt{3}\,(1 + K + K^2)^{1/2}}$	$\dfrac{[1+(1+\alpha+\alpha^2)K^2+K(2+\alpha)]^{1/2}}{\sqrt{3}\,(1 + K + K^2)^{1/2}}$

TABLE (5.3)

Figs. (5.5 and 6) illustrate the variation of these relaying quantities, under the fault conditions considered here, with respect to "α" varying from ± 2 to ± 16, and for different values of "K" from 0.1 to 16.

Table (5.3) comprises, in fact, only two expressions namely

$$\text{Exp. (5)} = \frac{1 + (1 - \alpha)K}{\sqrt{3}\,(1 + K + K^2)^{1/2}} \quad \text{and}$$

$$\text{Exp. (6)} = \frac{[1 + (1 + \alpha + \alpha^2)K^2 + K(2 + \alpha)]^{1/2}}{\sqrt{3}\,(1 + K + K^2)^{1/2}}$$

Figs. (5.5 and 6) give magnitude of the relaying quantities, for $N = \pm 1$, expressed as a fraction of the fault current I_F.

$$K = X_O/X_1 = X_O/X_3$$
$$R_O = 0$$

(K=16)
(K=10)
(K=5)
K=16
K=10
(K=5)
(K=2)
K=2
(K=10)
K=10
(K=05)
K=0·5
(K=0·2)
(K=0·1)
K=0·2
K=0·1

Double Phase/Earth Faults (EXP. V)
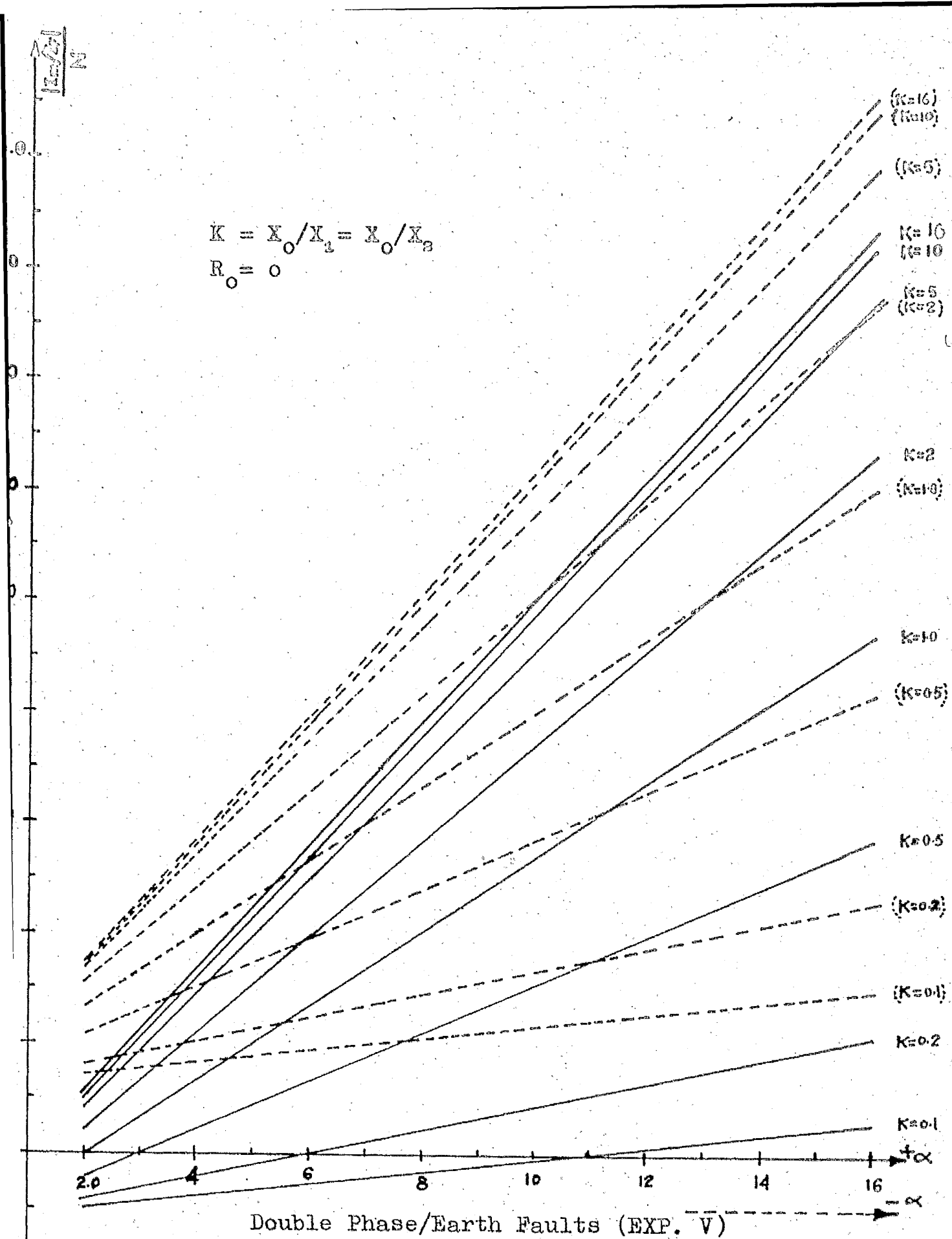
FIG. (5.5)   EVALUATION OF RELAYING QUANTITIES.

It can also be seen that the general trend is a bigger output as "α" increases, but it should be noticed that for positive values of "α" Exp. (4) passes through zero, for values of K $<$ 1.0. For negative values of "α" expression (5) does not change its sign, i.e. does not become zero for any value of K from 0.1 to 16. From Fig. (5.6) it can be seen that the relaying quantity as given by expression (6) does not change sign nor does it pass zero for positive and negative values of "α" and over the whole range of K from 0.1 to 16.

The second stage of the analysis, of the general case of section (5.7), followed the special case mentioned above and an analysis of a system having $Z_O = R_O + jX_O$ was considered with the assumptions,

$$k = \frac{jX_O}{jX_1} = \frac{jX_O}{jX_2}, \quad \text{and} \quad k_1 = \frac{R_O}{X_1} = \frac{R_O}{X_2}.$$

The expressions for the evaluation of relaying quantities under different double phase to earth conditions, are shown in Table (5.4) below:-

$$K = X_O/X_1 = X_O/X_2$$
$$R_O = 0$$
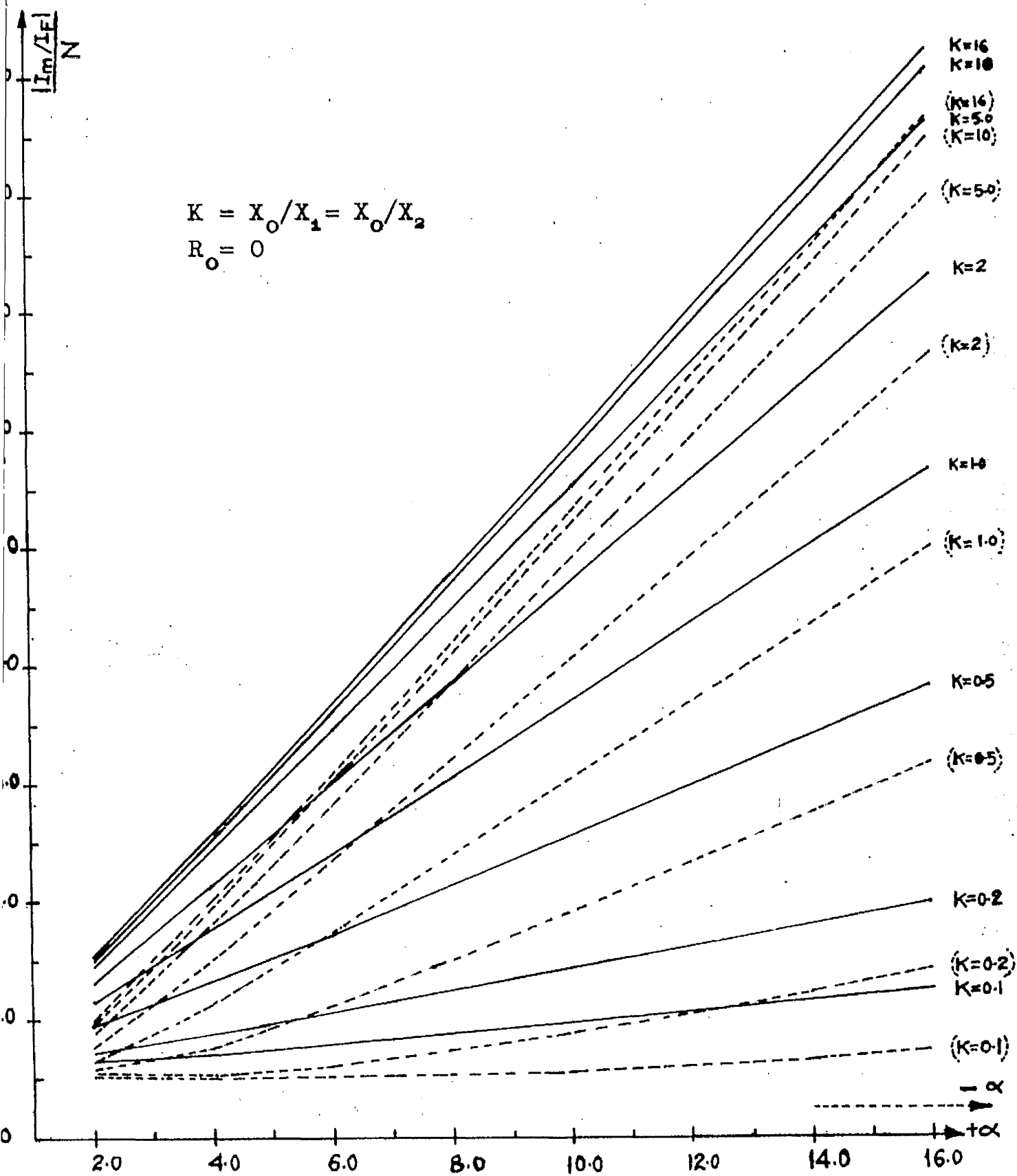
Double Phase/Earth Fault (EXP. VI)

FIG. (5.6) EVALUATION OF RELAYING QUANTITIES.

Relaying Quantity	Double Phase/Earth faults		
	"b − c"/E	"a − b"/E	"c − a"/E
$\dfrac{\|I_{m_1}/I_F\|}{N}$	Exp. (VII)	Exp. (XI)	Exp. (IX)
$\dfrac{\|I_{m_2}/I_F\|}{N}$	Exp. (VIII)	Exp. (XII)	Exp. (XI)
$\dfrac{\|I_{m_3}/I_F\|}{N}$	Exp. (X)	Exp. (IX)	Exp. (XII)

TABLE (5.4)

where

$$\text{Exp. (VII)} = \frac{\left[1 + (1 - \alpha)^2(K_1^2 + K^2) + 2(1 - \alpha)K\right]^{1/2}}{\sqrt{3}\left[1 + (K_1 + K) + (K + \sqrt{3}K_1)\right]^{1/2}}$$

$$\text{Exp. (VIII)} = \frac{\left[1 + (1 + \alpha + \alpha^2)(K_1^2 + K^2) + (2 + \alpha)K - \sqrt{3}K_1\alpha\right]^{1/2}}{\sqrt{3}\left[1 + (K_1^2 + K^2) + (K + \sqrt{3}K_1)\right]^{1/2}}$$

$$\text{Exp. (IX)} = \frac{\left[1 + (1 + \alpha + \alpha^2)(K_1^2 + K^2) + (2 + \alpha)K - \sqrt{3}\alpha K_1\right]^{1/2}}{\sqrt{3}\left[1 + (K_1^2 + K^2) + (K - \sqrt{3}K_1)\right]^{1/2}}$$

$$\text{Exp. (X)} = \frac{\left[1 + (1 + \alpha + \alpha^2)(K_1^2 + K^2) + (2 + \alpha)K + \sqrt{3}\alpha K_1\right]^{1/2}}{\sqrt{3}\left[1 + (K_1^2 + K^2) + (K + \sqrt{3}K_1)\right]^{1/2}}$$

$$\text{Exp. (XI)} = \frac{\left[1 + (1 + \alpha + \alpha^2)(K_1^2 + K^2) + (2 + \alpha)K + \sqrt{3}\alpha K_1\right]^{1/2}}{\sqrt{3}\left[1 + (K_1^2 + K^2) + (K - \sqrt{3}K_1)\right]^{1/2}}$$

$$\text{Exp. (XII)} = \frac{\sqrt{1 + (1 - \alpha)^2(K_1^2 + K^2) + 2(1 - \alpha)K\;\rule[-0.5ex]{0.1ex}{1.5ex}}^{1/2}}{\sqrt{3}\;\sqrt{1 + (K_1^2 + K^2) + (K - \sqrt{3}\,K_1)\;\rule[-0.5ex]{0.1ex}{1.5ex}}^{1/2}}$$

The previous analysis has shown that a relaying quantity having a negative "α" is preferable. For this reason the evaluation of Exps. (VII) to (XII) inclusive was carried out for only negative values of "α", varying from -2 to - 16, but a representative selection of curves only for the case of $\alpha = -6$ are illustrated in this section. This particular case was also recommended by other authors[8][9].

Fig. (5.7) shows the variation of the relaying quantity given by Exps. (VIII and XII), of Table (5.4), for values of $k_1 = {}^{R_0}/_{X_1}$ from 0.1 to 16 keeping the value of $k = {}^{jX_0}/_{jX_1}$ constant at 0.5, 1.0, 2.0, and 3.0 respectively. The chosen range of values would generally cover many practical cases.

Figs. (5.8 and 9) give also the variation of Exps. (VII, XI) and (IX, X) respectively, for the range of k_1 and k as that chosen for Fig. (5.7).

From the curves in Figs. (5.8 and 5.9) it can be seen that each relaying quantity passes through a range of values depending on the type of fault. The quantity I_{m_1} gives higher relaying outputs for the case of "c - a"/E fault, while I_{m_2} gives its highest value for an "a - b"/E fault and I_{m_3} for "c - a"/E fault.

The general trend of the magnitudes of the relaying quantities

$K = X_O/X_1 = X_O/X_2$

$K_1 = R_O/X_1$

EXP.(XII)

EXP.(VIII)

K=3.0

K=2.0

K=1.0

K=0.5

K=3.0

K=2.0

K=1.0

K=0.5

$\dfrac{N}{|I_m/I_f|}$

Double Phase/Earth Faults
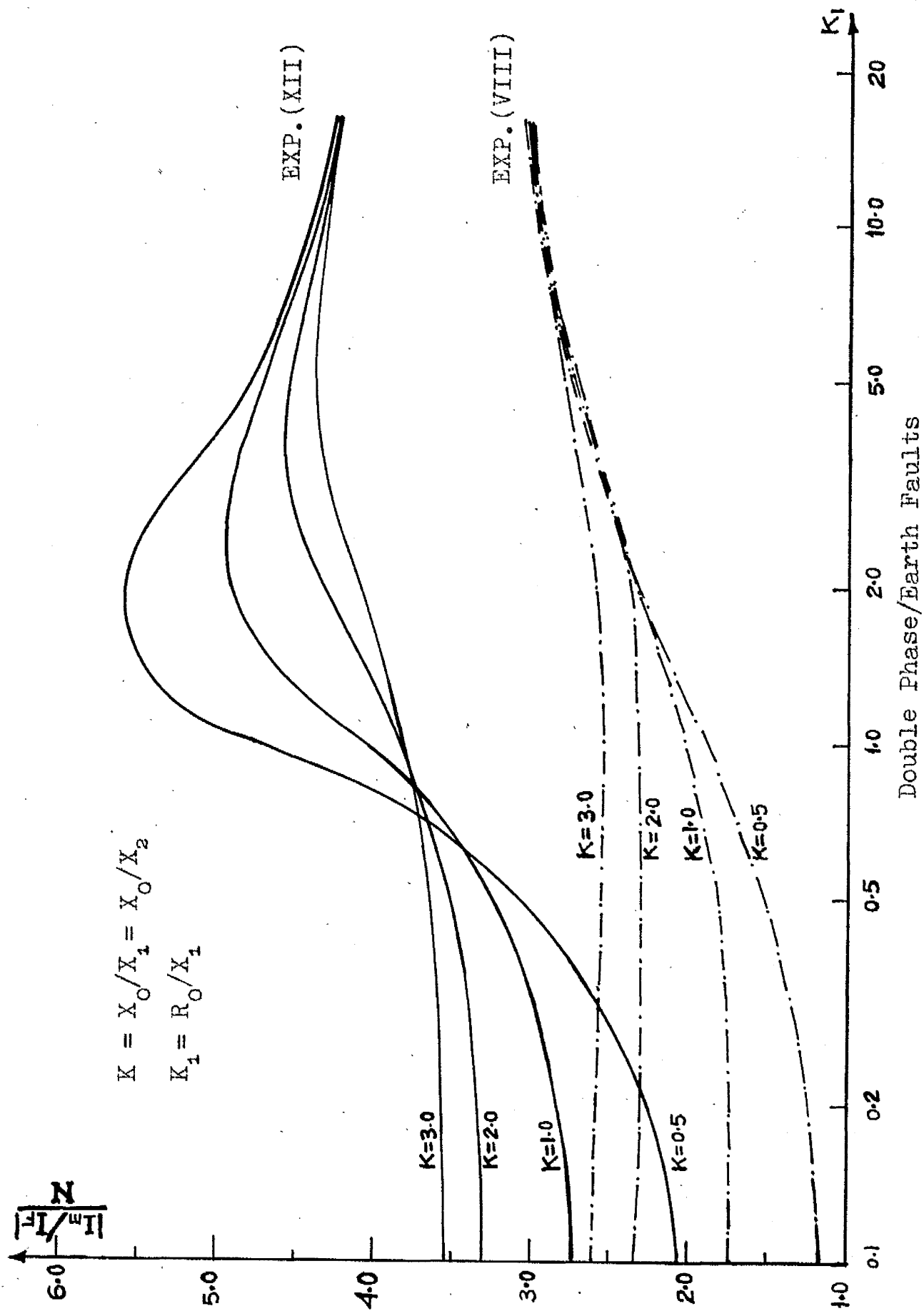
FIG. (5.7) EVALUATION OF RELAYING QUANTITIES.

is that the different output levels attained under various fault conditions approaches each other as k_1 increases. For a particular system having certain specific parameters, the difference in magnitudes of the relaying quantity, under different double phase/earth faults, would tend to be smaller if $k \geq 2.0$.

In other words, the variation in the magnitude of any relaying quantity decreases as k increases.

The wide range chosen for $k_1 = {}^{R_0}/X_1$ would cover cases of fault where the resistance of the earth path, or the arc resistance, would vary from one fault to another. Thus for a certain system having a particular k_1, may be taken as variable, while k is more or less fixed by the transmission lines and other system parameters.

5.9 Conclusions

This chapter was devoted completely to a detailed analysis of the combination of sequence currents for phase angle representation. Remarks and conclusions are generally mentioned with each section in their appropriate places. However, general conclusions can be reached for the chosen relaying quantities. Under single phase to earth faults, and by proper choice of either I_{m_1}, I_{m_2}, or I_{m_3} of eqns. (5.1), such a fault would appear, as a fault to earth on another phase. This has been demonstrated in section (5.8).

FIG. (5.8) EVALUATION OF RELAYING QUANTITIES.

$K = X_0/X_1 = X_0/X_2$

$K_1 = R_0/X_1$
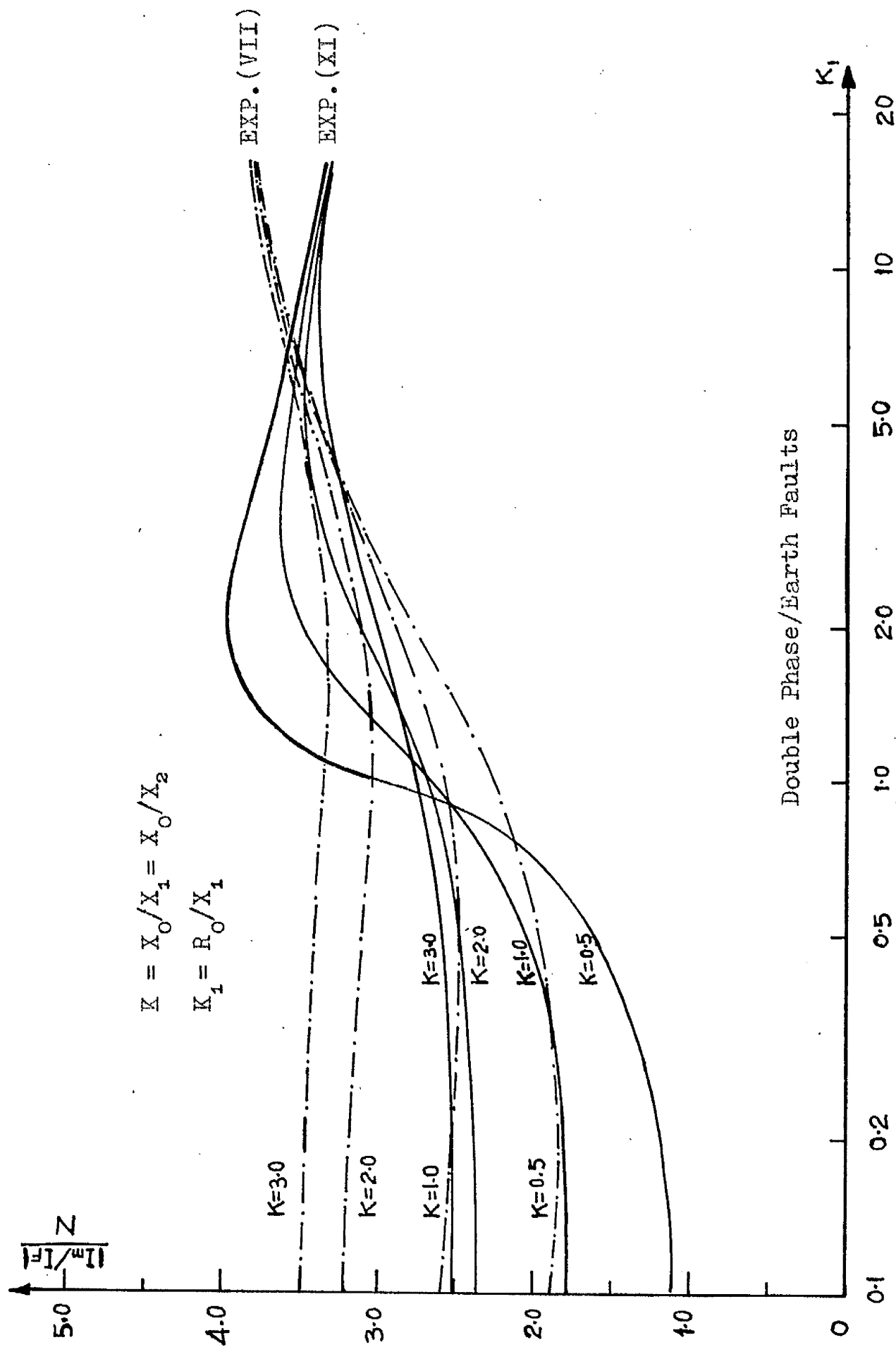
Double Phase/Earth Faults
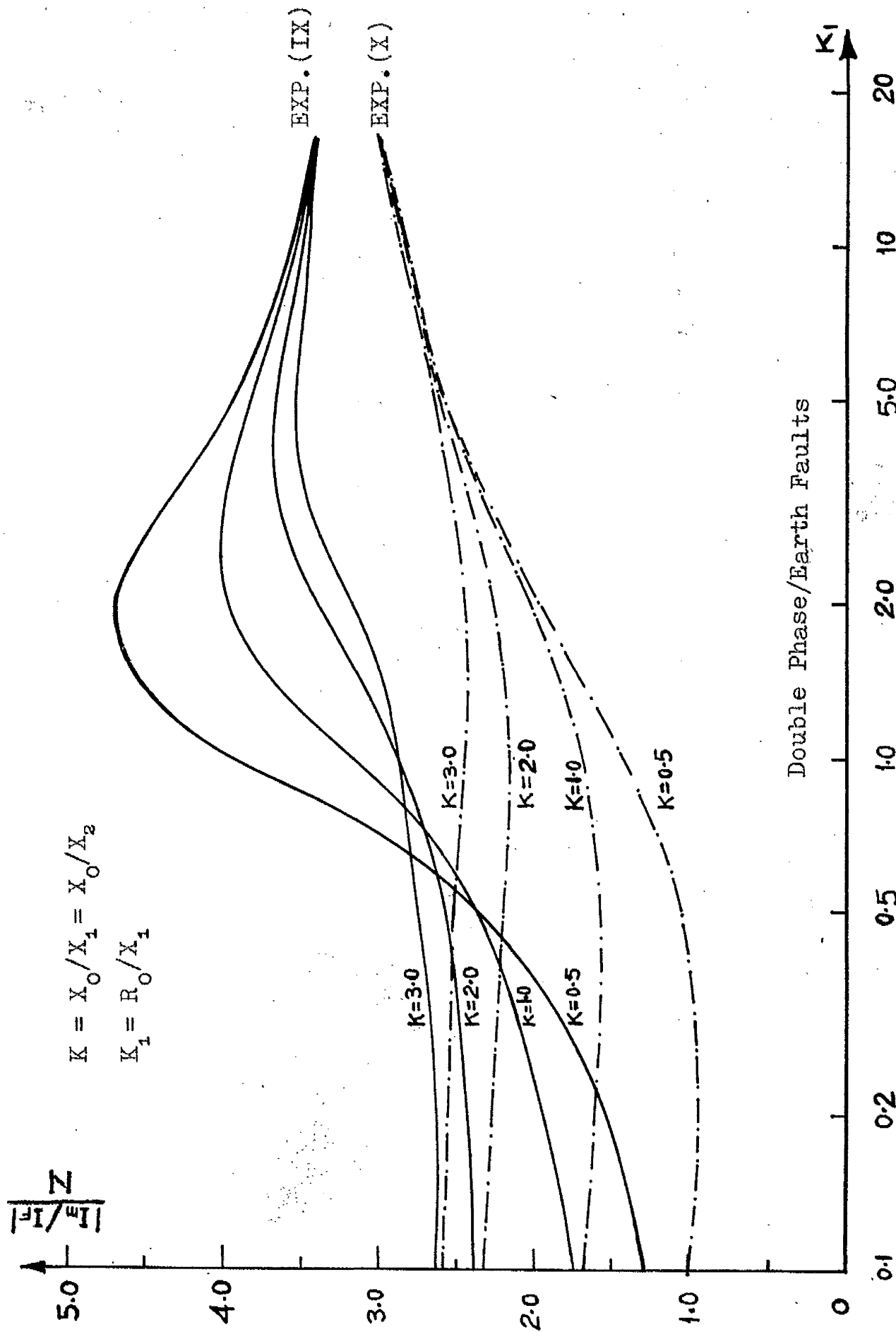
FIG. (5.9) EVALUATION OF RELAYING QUANTITIES.

The method of selecting different relaying quantities would
also result in the relaying quantity having an output level
corresponding to a fault on the reference phase.

Such a consequence could prove to be useful in some special
applications. One of these cases is that of double circuit
transmission lines. Such lines have generally one earth wire and
thus resulting in a different degree of shielding of the phase
conductors, because of their equal vertical spacings.

This leads to the fact that one phase may be more prone to
lightning strokes than the other two. The combination of the
relaying quantity could then be modified to suit such a condition
to give higher outputs, thus increasing the sensitivity of this
particular phase.

A general rule could not be easily drawn because the magnitude
of the relaying quantities could be higher or lower depending on
"α" being positive or negative, section (5.8).

Another case where these relaying quantities combinations
are useful is when different insulation levels on the phases is
practiced. By lowering the insulation level on one phase
conductor, it would be more vulnerable to lightning strokes and
flash overs than the other two. Advantage of different phase
combinations for the relaying quantity can also be taken here
to increase the sensitivity.

In fact, the idea behind the analysis of the different

relaying quantities I_{m_1}, I_{m_2}, and I_{m_3} was only to demonstrate the benefits of utilising the symmetry between sequence component currents of a 3-phase system. Higher relaying outputs could be obtained, by proper selection, and thus increasing sensitivity for any particular type of fault.

From Figs. (5.4, 5 and 6), it can be seen that the higher the value of "α", i.e. the greater the proportion of the negative sequence component in the relaying quantity, the higher becomes the ratio $|I_m/I_F|$. This conclusion is true in cases of single phase to earth or double phase faults (not involving earth) for all negative values of "α". For positive values of "α" and $K < 1.0$ the case is not so, as $|I_m/I_F|$ passes through zero and changes its sign. A relaying quantity which passes through such a "blind spot" should be avoided and therefore only negative values of "α" are recommended.

The effect of different transformer connections at the two ends of the line has been considered in section (5.5.1). The choice of $N = +1$ in the relaying expressions imposes a limitation on the value of "M" to be greater than one, when the transformer connections at one end does not allow any zero phase sequence current to flow.

The effect of the zero sequence resistance R_O is discussed in detail in section (5.7). The cases represented give more practical conditions than those obtained by previous investigators, [9]

and also the evaluation of the three chosen relaying quantities
covers a wider range of system parameters.

For further development, sufficient generality would be achieved
by considering the case of a double circuit teed feeder having ring
generations at the three ends. This problem is better tackled
by the help of a digital computer, in order to determine the
relaying quantities under different fault conditions. The effect
of mutual impedances, in the case of parallel circuits, on the zero-
sequence impedances may be also included. Shunt faults as well as
series faults can then be considered and even some simultaneous
faults, e.g. double earth faults, would provide a wide range of
studies. A moving fault on the double circuit lines would also be
a probability to be envisaged.

It is felt that such a rigorous analysis of relaying quantities
might prove easier to be tackled in primary phase quantities, and
not by phase sequence components. The simple analysis carried
out in this chapter using sequence components has proved to be
lengthy, and a computer would be most suitable for further
investigations.

CHAPTER 6

SEQUENCE COMPONENTS SEGREGATING NETWORKS

FOR EXTRACTING RELAYING QUANTITIES

6.1 Introduction

Generally speaking sequence component currents or voltages, have long been used in protection of power systems[20][27][28]. In this chapter some types of segregating networks have been developed and tested, and a complete analysis has also been described. These circuits are in general, suitable for voltage sources, such as voltage transformers and in particular ironless-core C.T.s (linear couplers).

The segregating networks produce signals which are used, in the scheme developed here, as relaying quantities. These signals are:-

(a) The positive sequence component of the fault current which is required as a fault detecting, or starting, signal. This quantity detects the presence of poly-phase faults.

(b) The zero sequence component of the fault current, which acts also as a starting signal, to detect mainly single phase to earth faults and any other types of fault involving earth. Series faults may also be detected by this quantity.

(c) A combination of the positive and the negative sequence components of the fault current, at each end of the protected feeder, to represent the phase angle, as explained earlier in Chapter (5).

The main purpose of segregating or sequence networks is therefore to provide outputs, voltages or currents, proportional to the sequence components of the fault current.

6.1.1 Basic Vectorial Approach

It can be easily proved, in the absence of the zero sequence component, that the positive sequence component of a particular vector of an unbalanced 3 phase system, is given correctly both in magnitude and in phase by adding to the vector concerned its succeeding one advanced by 60° and then advancing the resultant, divided by $\sqrt{3}$, by a further 30°.

There is also a corresponding method for obtaining the negative sequence component of this vector[28].

The general equations for the sequence components of an unbalanced 3 phase voltages are:-

$$V_0 = \frac{1}{3}(V_A + V_B + V_C)$$

$$V_{a_1} = \frac{1}{3}(V_A + V_B + a^2 V_C) \qquad \ldots \ldots (6.1)$$

$$V_{a_2} = \frac{1}{3}(V_A + a^2 V_B + a V_C)$$

where V_A, V_B, and V_C are the 3 phase voltages, suffix 1

denotes positive sequence and 2 the negative sequence component.

In the absence of the zero sequence component,
$V_A + V_B + V_C = 0$, and therefore $V_C = - (V_A + V_B)$. Substituting for V_C in eqn. (6.1), the positive sequence component V_{a_1} of vector V_A is therefore given by:-

$$V_{a_1} = \frac{1}{3} \left[V_A (1 - a^2) + a V_B (1 - a) \right]$$

$$= \frac{1 - a^2}{\sqrt{3}} \left[\frac{V_A - a^2 V_B}{\sqrt{3}} \right] \qquad \ldots\ldots (6.2)$$

Eqn. (6.2) is, in fact, the expression of the verbal statement made earlier in this section. Similarly, for the negative sequence component

$$V_{a_2} = \frac{1 - a}{\sqrt{3}} \left[\frac{V_A - a V_B}{\sqrt{3}} \right] \qquad \ldots\ldots (6.3)$$

The vectorial operational instructions given in eqns. (6.2 and 3) can be performed electrically and a large number of circuits have been devised for this purpose[20][27][28][29][30].

The required phase shifts are, of course, provided by resistive elements in conjunction with reactive components. Either capacitive or inductive reactances can, in principle, be used but, in practice there are good reasons for using one or the other. As a broad general statement, capacitors are preferred in voltage segregating circuits and inductors in current circuits.

Voltage segregating networks are usually of a relatively high impedance type, in order to keep the power dissipated in the circuit elements as low as possible. For this type capacitors are most suitable. In current segregating circuits where larger currents have to be handled, inductors are preferred.

Ironless-core C.T.s or linear couplers, as applied with the developed protective scheme, produce 3 phase voltage outputs and therefore their sequence components are given by eqns. (6.1), where V_A, V_B, and V_C are proportional to the primary currents I_A, I_B, and I_C respectively.

Voltage segregating circuits have been developed and an analysis of their behaviour is given in this Chapter.

6.2 Analysis of a Voltage Segregating Network

Referring to the network in Fig. (6.1A) and considering branch "AB" only, Kirchhoff's laws gives:-

$$V_A = I_Z Z_C + I_L Z_L$$

$$V_B = I_R R + I_L Z_L$$

$$\left. \right\} \quad \ldots\ldots \quad (6.4)$$

and

$$I_L = I_Z + I_R$$

where Z_L is the total load reflected impedance across the primary of the output transformer T_C, I_L is the load current referred to the primary of T_C. Fig. (6.1B) gives the complete circuit given for a 3 phase unbalanced system V_A, V_B, and V_C.
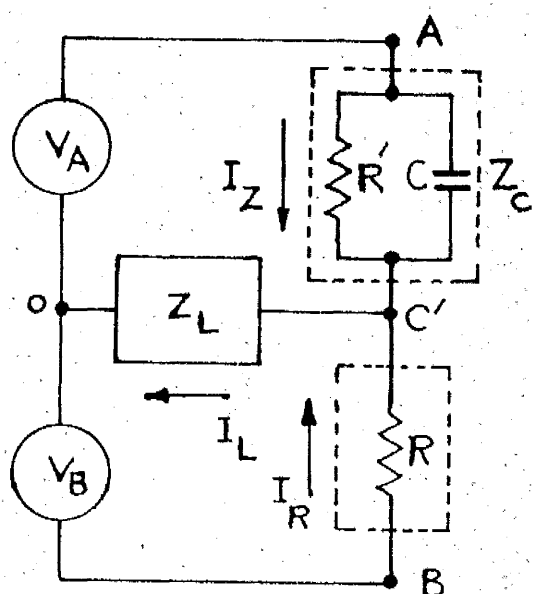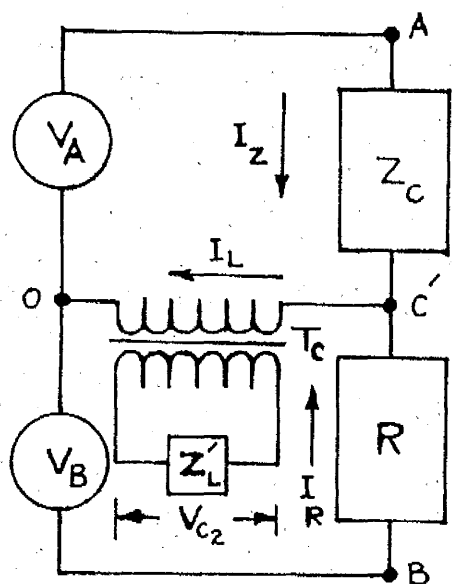
$Z_C = -aR$

Z_L Reflected Load Impedance

T_C Output Transf.

(A) Branch "AB"

(B) Three Phase Arrangement
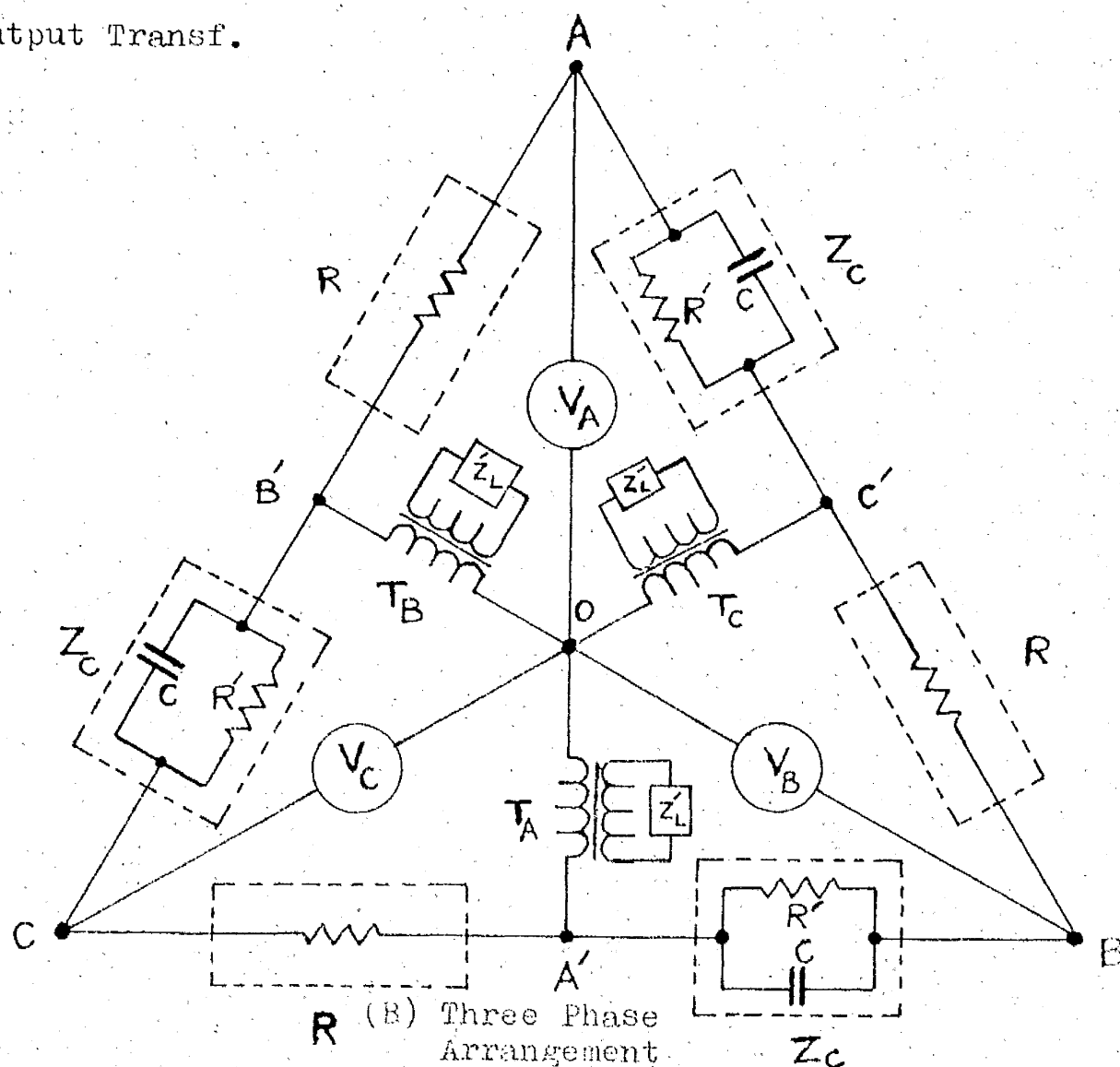
FIG. (6.1) NEGATIVE SEQUENCE SEGREGATING NETWORK.

It is assumed, initially, that the zero sequence component is absent. Its presence will be introduced in a later stage in the analysis in section (6.2.6).

If the impedances R and Z_C are chosen to be equal in magnitude, but differ in phase angle by -60°, i.e. $Z_C = -aR$. Now Z_C can be eliminated from eqns. (6.4) and substituting the values obtained for V_A and V_B in eqn. (6.3), it follows:-

$$V_{a_2} = \frac{1-a}{\sqrt{3}} \left[\frac{-aR.I_L + I_L Z_L(1-a)}{\sqrt{3}} \right] \quad \ldots \ldots \quad (6.5)$$

or $\quad a V_{a_2} = \frac{1-a^2}{\sqrt{3}} . I_L Z_L . \frac{(1-a^2) + R/Z_L}{\sqrt{3}} = V_{b_2} \quad \ldots \ldots \quad (6.6)$

The circuit shown in Fig. (6.1) is, in fact a negative sequence voltage segregating circuit. The corresponding positive sequence circuit is obtained by interchanging the resistive and capacitive impedances R and Z_C.

In a similar manner to that described for the negative sequence circuit, it can be shown by substituting in eqn. (6.2) that the positive sequence component is given by:-

$$V_{a_1} = \frac{1-a^2}{\sqrt{3}} . I_L Z_L . \frac{(1-a^2) + R/Z_L}{\sqrt{3}} \quad \ldots \ldots \quad (6.7)$$

6.2.1 <u>Design Considerations and Calibration</u>

The relation between the negative sequence segregating circuit elements, as stated before, is $Z_C = -aR$, for the

circuit illustrated in Fig. (6.1A).

This relationship defines a 60° capacitive impedance. It may be composed either of a series resistive-capacitive combination or a parallel one. Where these two arrangements differ is in their frequency error behaviour at frequencies different from the normal frequency of the system and the parallel combination has proved to have smaller frequency errors[30].

The logical procedure in designing such a 3 phase negative sequence segregating circuit as in Fig. (6.1B) is to calculate the approximate values of the components for a certain maximum permissible power dissipation. The components could be adjusted separately to the calculated values using bridge measurements or the like. Alternatively, in a more practical and precise way, final adjustment of the pre-settings is achieved experimentally, by employing a genuine balanced 3 phase voltage supply. The method is based on applying a completely balanced 3 phase positive sequence voltage supply to the negative sequence segregating network. The output of the segregating circuit under such conditions would ideally be zero. Consequently the procedure for adjustment is simply to trim either the resistance element R or the capacitive impedance branch Z_c or both until a zero output reading is obtained. The sequence network acts now as its own nil indicator.

This simple and practical method has the advantage that

stray capacitances and leakage resistances are included in the final adjustment, and accumulative errors, which would arise from individual measurement of elements separately, are avoided. The correct adjustment is therefore easily achieved and the accuracy is determined by that of the meter in use, to detect zero output from the circuit terminals.

Considering now one branch of the segregating circuit as "AB", Fig. (6.1A), and for a power dissipation of about 10 watts, with input voltages $V_A = V_B = V_C = 120 V$. The corresponding calculated values for R and Z_C, assuming the load impedance Z_L to be zero, are about 2750 ohms for R and Z_C is made of $C \simeq 1.0 \mu F$ in parallel with a resistance $R' \simeq 5500$ ohms.

These design values have, in fact, taken into consideration the case of maximum power dissipation and if the load impedance Z_L is different from zero, the power dissipation will consequently be reduced.

6.2.2 Conditions for Maximum Output into the Load

Referring to Fig. (6.1A) which represent one branch in the negative sequence segregating circuit, Fig. (6.1B), and applying superposition theorem it gives:-

$$I_L = I'_Z + I'_R \qquad \ldots\ldots (6.8)$$

where I'_Z and I'_R are the currents in Z_L when V_B and V_A

are short-circuited, each in turn, respectively. V_A and V_B are assumed to have zero source impedances.

Hence
$$I_L = \frac{V_A \cdot R + V_B \cdot Z_c}{Z_c \cdot R + Z_L \cdot R + Z_L \cdot Z_c} \qquad \ldots\ldots (6.9)$$

Substituting $Z_c = - aR$, in eqn. (6.9) it follows:-

$$I_L = \frac{(V_A - a\,V_B)}{- a \cdot Z_L \left[(1 - a^2) + R/Z_L \right]} \qquad \ldots\ldots (6.10)$$

Substituting again eqn. (6.5) in eqn. (6.10) it gives:-

$$\frac{3\,V_{a2}}{(1-a)} = - a \cdot Z_L I_L \left[(1 - a^2) + R/Z_L \right]$$

From which the voltage $V_{c'o}$, Fig. (6.1A), can be obtained:-

$$\overline{I}_L \cdot \overline{Z}_L = V_{c'o} = a\,V_{a2} \cdot \frac{\sqrt{3}}{(1-a^2)} \cdot \frac{\sqrt{3}}{(1-a^2) + R/Z_L}$$

If $\overline{Z}_L$ is expressed in a general form by,

$$\overline{Z}_L = |Z_L| \cdot e^{j\theta}$$

therefore,

$$V_{c'o} = V_{a2} \cdot \frac{1}{1 + \dfrac{R}{\sqrt{3}} \cdot \dfrac{e^{-j(\theta+30)}}{|Z_L|}}$$

Hence

$$|V_{c'o}| = |V_{a2}| \cdot \frac{1}{\left[1 + \dfrac{R^2}{3|Z_L|^2} + \dfrac{2R}{\sqrt{3}\,|Z_L|} \cos(\theta + 30) \right]^{1/2}} \qquad \ldots\ldots (6.11)$$

The VA output of the circuit into the load is given by $|I_L|^2 \cdot |Z_L|$ and by substitution from eqn. (6.11), then

The VA output $= |V_{oc}|^2 / |Z_L|$

$$= \frac{|V_{a2}|^2}{|Z_L| + R^2/3|Z_L| + 2R \cos(\theta + 30)}$$

..... (6.12)

Eqn. (6.12) contains two variables namely the magnitude of $|Z_L|$ and its angle "θ".

For a certain value of negative sequence component $|V_{a2}|$, the maximum value of VA is obtained when "θ" attains an optimum value of 60°, i.e. Z_L represents an inductive load for maximum VA output.

If the reflected load impedance Z_L, Fig. (6.1A), is a pure resistance i.e. $\theta = 0$, such cases are generally favoured in protective gear, then the optimum magnitude of $|Z_L|$ could be obtained if eqn. (6.12) is differentiated w.r.t. $|Z_L|$ as a variable and then equating the differential to zero.

$$\frac{d \angle VA \rfloor}{d \angle Z_L \rfloor} = \frac{-|V_{a2}| \angle 1 - R^2/3|Z_L|^2 \rfloor}{\angle |Z_L| + R/3|Z_L| + 2R/\sqrt{3} \rfloor^2} = 0$$

from which, for max. VA,

$$|Z_L| = R/\sqrt{3}$$

..... (6.13)

Eqn. (6.13) gives the matching load impedance for the negative sequence segregating network of Fig. (6.1B).

The magnitude of the reflected load impedance Z_L is controlled by the turns ratio of the output transformers T_A, T_B, and T_C, as will be explained in section (6.2.4), and then Z'_L could be arranged to match $|Z_L| = R/\sqrt{3}$ on the primary side.

6.2.3 Impedance Presented to Supply Source

The circuit shown in Fig. (6.1B) presents on the supply an impedance per phase which is given by the following extremes:-

(a) The reflected load impedance Z_L is zero. Under such a condition the magnitude of the impedance Z_{in} presented by the circuit to the source is given by:

$$Z_{in} = \frac{Z_C \cdot R}{Z_C + R} \,, \quad \text{substituting } Z_C = -aR \text{ then,}$$

$$Z_{in} = \frac{R}{\sqrt{3}} \, \angle -30^\circ$$

hence,

$$|Z_{in}|_{s.c.} = \frac{R}{\sqrt{3}} \qquad \qquad \ldots\ldots \ (6.14)$$

(b) The load impedance Z_L tends to infinity. This extreme case is equivalent to an open circuit on the secondary of the output transformer, Fig. (6.1B), i.e. $Z_L \rightarrow \infty$.

Since the impedances of all the three branches are equal, i.e. $Z_{AB} = Z_{BC} = C_{CA}$, then the impedance per phase presented by the circuit to its supplies is :-

$$Z_{in} = \frac{Z_{AB}}{3} = \frac{R + Z_c}{3}, \quad \text{if} \quad Z_c = -aR \quad \text{then,}$$

$$|Z_{in}|_{o.c} = \frac{R}{\sqrt{3}} \underline{/-30^0} \qquad \qquad \ldots\ldots \quad (6.15)$$

Comparing eqns. (6.14 and 15) it can be seen that $|Z_{in}|_{s.c.} = |Z_{in}|_{o.c.}$. The result obtained is considered fortuitous due to the symmetry of the network on a 3 phase basis, and to the fact that a series combination of Z_c and R is equal to their parallel equivalent for the condition chosen of $Z_c = -aR$.

6.2.4 The Effect of the Load Impedance

Eqn. (6.6) gives the expression for the output of the circuit, shown in Fig. (6.1B), as :-

$$a \, V_{a2} = \frac{1 - a^2}{\sqrt{3}} \cdot I_L \, Z_L \cdot \underline{\bigg/ \frac{(1 - a^2) + R/Z_L}{\sqrt{3}} \bigg]}$$

It is clear that the product $(I_L. \, Z_L)$ is simply the voltage $V_{c'o}$ across the load impedance, referred to the primary side of the output transformer.

If this impedance Z_L, which is determined by Z'_L and the transformer turns ratio, is sufficiently high, then the

ratio R/Z_L may be neglected in eqn. (6.6), and the output
expression can then be reduced to :-

$$a \ V_{a_2} \simeq \frac{(1 - a^2)^2}{\sqrt{3}} \ . \ V_{c'o} \qquad \ldots \ (6.16)$$

The output voltage $V_{c'o}$ is therefore directly equal to
the negative sequence component, since the term $(1 - a^2)^2/\sqrt{3}$ has
a unity magnitude.

On the other hand if the load impedance Z_L is very small,
or it is arranged to be so by controlling the turns ratio of the
output transformer, i.e. if $Z_L << R$ then ,

$$a \ V_{a_2} \simeq \frac{1 - a^2}{\sqrt{3}} \ . \ \frac{I_L \ R}{\sqrt{3}} \qquad \ldots \ (6.17)$$

Expression (6.17) shows, that the current in the load
impedance Z_L is proportional to the negative sequence voltage
component and the constant of proportionality is a fixed factor
given by $R/\sqrt{3}$. This constant is a circuit parameter and does
not depend on the load impedance Z_L , provided it is small, as
assumed earlier.

Generally, if Z_L is not small compared to the circuit
parameter R , then the voltage $V_{c'o}$ will be expressed in a
complex form having a magnitude less than unity compared to V_{a_2}.
This can be further explained by considering the phase
relationship of the output voltage $V_{c'o}$ w.r.t. the applied

voltages.

Eqn. (6.6) can be re-written as follows:-

$$a \, V_{a2} = V_{c'0} \cdot \left[\frac{(1 - a^2) + R/Z_L}{\sqrt{3}} \right] \left[\frac{1 - a^2}{\sqrt{3}} \right]$$

..... (6.18)

As mentioned earlier if $R/Z_L \ll 1$ and can be neglected therefore,

$$a \, V_{a2} \simeq V_{c'0} \frac{(1 - a^2)^2}{3} = V_{c'0} \cdot \angle 60^0$$

or $V_{c'0} = -a^2 \, V_{a2} = -V_{c2}$ ..... (6.19)

where V_{c2} is the negative sequence component voltage of V_c.

Similarly it can be shown that in Fig. (6.1B)

$$V_{B'0} = -V_{b2} \quad \text{and} \quad V_{A'0} = -V_{a2} \quad ..... (6.20)$$

In the case where the load impedance Z_L, referred to the primary of the output transformer, is not small enough to be neglected, there will not only be a reduction in magnitude, but also a certain phase displacement.

This reduction in magnitude can be controlled, or compensated for if desired, by the appropriate choice of the turns ratio of the output transformers T_A, T_B, and T_C of Fig. (6.1B). In other words, if these output transformers

are of the step-down type, then the magnitude of the reflected impedance Z_L on the transformer primary will be reduced by $1/N^2$, where "N" is the transformation ratio. For this case of a step-down transformer "N" is bigger than unity, hence if $1/N^2$ is made small enough that $Z_L << R$ then, the output voltage $V_{c'o}$ will be given by eqn. (6.17).

As mentioned earlier in section (6.2.2), the turns ratio can be chosen to reflect on the primary of the output transformer an impedance Z_L which is given by eqn. (6.13) for max. VA output.

It can be noticed from the previous analysis that the output transformers play an essential part in the design and performance of the segregating circuits of the type shown in Fig. (6.1B). This feature offers flexibility in design, where the only controllable circuit parameter to meet different loading conditions, would be the choice of the appropriate output transformer.

The analysis given before was carried out for the negative sequence voltage segregating circuit, but as mentioned in section (6.2), a similar analysis can be obtained for the corresponding positive sequence segregating circuit by interchanging the branches Z_c and R. The output expression for such circuit is given in eqn. (6.7).

6.2.5 Frequency Response

All symmetrical components segregating networks are pre-adjusted frequency sensitive devices. The departure of frequency from the normal system frequency, or the calibrating one will always cause an error. In practice, the frequency deviations on the British Grid System is generally small and departures of the order + 2% to - 6% are rather unusual nowadays.

The output of any symmetrical component segregating network, at normal system frequency, would respond only to one type of sequence component, e.g. the positive or the negative. Whereas at other frequencies both sequence components play a part, i.e. both are present in the output of the segregating circuit.

When the frequency of the supply applied to a segregating circuit of the type discussed in section (6.2), is different from the normal frequency, the impedance of the capacitive branch Z_C would suffer changes both in magnitude and in phase. As a consequence of this, the simple relation given by $Z_C = - aR$ will no longer hold true and a modified form must be used.

The relation $Z_C = - aR$ can be written as :-

$$Z_C = R \cdot e^{-j60} = \frac{R}{2} (1 - j \sqrt{3}) \qquad \dots \dots (6.21)$$

If "α" represents the applied frequency as a fraction of the normal, or calibrating, system frequency then eqn. (6.21) can be rewritten in a general form :-

$$Z_c = \frac{R}{2}\left(1 - j\frac{\sqrt{3}}{\alpha}\right) \qquad \ldots\ldots (6.22)$$

where "α" will ordinarily be little different from unity for all practical applications in protection of power systems.

Following the same steps as in section (6.2), by eliminating Z_c, in eqns. (6.4) then:-

$$V_B + \frac{2\,V_A}{(1 - j\,\sqrt{3}/\alpha)} = I_L \underline{/R} + Z_L\left(1 + \frac{2}{(1 - j\,\sqrt{3}/\alpha)}\right)\underline{/}$$

$$\ldots\ldots (6.23)$$

Substituting V_A and V_B by their symmetrical components in eqn. (6.23), gives :-

$$a\,V_{a_1}(1-\alpha) + V_{a_2}(\alpha+1) = \frac{a^2}{\sqrt{3}}\left(\sqrt{3} + j\alpha\right).\,I_L\underline{/R} + Z_L\left(1 + \frac{2}{1 - j\,\sqrt{3}/\alpha}\right)\underline{/}$$

$$\ldots\ldots (6.24)$$

Now considering as before the two extreme cases for the load impedance Z_L namely :-

(a) If Z_L can be neglected compared to R then,

$$a\,V_{a_1}(1-\alpha) + V_{a_2}(\alpha+1) \simeq a^2\left(\sqrt{3} + j\alpha\right).\,I_L\,\frac{R}{\sqrt{3}}$$

$$\ldots\ldots (6.25)$$

(b) If R/Z_L is small enough, i.e. $R/Z_L \ll 1$, then

$$a V_{a_1}(1-\alpha) + V_{a_2}(\alpha+1) \simeq \frac{a^2}{\sqrt{3}} (\sqrt{3} + j\alpha) \cdot I_L Z_L \cdot \left\{ 1 + \frac{2}{(1 - j \sqrt{3}/\alpha)} \right\}$$

$$= a^2 \cdot (1 + j \sqrt{3} \alpha) \cdot I_L Z_L \qquad \ldots\ldots (6.26)$$

Eqn. (6.24) shows that the output voltage $V_{a'_2}$ depends on both the negative and positive sequence components of the input voltage V_A, for for a negative sequence segregating circuit this will be interpreted as an apparent negative sequence output only. This apparent value is given by eqn. (6.17) for the case when $Z_L \ll R$,

$$\therefore \quad V'_{a_2} = I_L \cdot \frac{R}{\sqrt{3}} \cdot \angle 30^\circ \qquad \ldots\ldots (6.27)$$

Comparing eqns. (6.27) with its corresponding one, eqn. (6.25), then V_{a_1} and V_{a_2} can be expressed in terms of V'_{a_2} as follows :-

$$a V_{a_1}(1-\alpha) + V_{a_2}(\alpha+1) = a^2 \cdot V'_{a_2} \left[2 + a^2(1-\alpha) \right] \qquad \ldots\ldots (6.28)$$

Considering now the case of a balanced positive sequence supply, having a frequency different from the normal frequency applied to the circuit in question, then putting $V_{a_2} = 0$ in eqn. (6.24) it follows:-

$$a V_{a_1}(1-\alpha) = \frac{a^2}{\sqrt{3}} (\sqrt{3} + j\alpha) \cdot I_L Z_L \cdot \left[R/Z_L + 1 + \frac{2}{1 - j \sqrt{3}/\alpha} \right]$$

$$\ldots\ldots (6.29)$$

Following the same argument as before there are two particular cases corresponding to high, and low load impedance Z_L in comparison with R.

For $R/Z_L \ll 1$ then, it follows that :-

$$a\, V_{a_1}(1 - \alpha) = a^2 \cdot I_L Z_L \cdot (1 + j\sqrt{3}\,\alpha) \qquad \ldots\ldots (6.30)$$

Therefore

$$\frac{I_L Z_L}{V_{a_1}} = \frac{a^2(1 - \alpha)}{1 + j\sqrt{3}\,\alpha} \qquad \ldots\ldots (6.31)$$

From eqn. (6.31) and putting $V_{oc}' = I_L Z_L$ then ,

$$\left| \frac{V_{oc}'}{V_{a_1}} \right| = \frac{1 - \alpha}{\sqrt{1 + 3\alpha^2}} \qquad \ldots\ldots (6.32)$$

Similarly the effect of a balanced negative sequence supply, with a frequency different from normal, can be obtained by putting $V_{a_1} = 0$ in eqn. (6.24), thus getting a general expression for the negative sequence component. This is,

$$V_{a_2}(\alpha + 1) = \frac{a^2}{\sqrt{3}} \cdot (\sqrt{3} + j\alpha) \cdot I_L Z_L \quad R/Z_L + 1 + \frac{2}{1 - j\sqrt{3}/\alpha}$$

$$\ldots\ldots (6.33)$$

For $R/Z_L \ll 1$ then,

$$V_{a_2}(\alpha + 1) = a^2(1 + j\sqrt{3}\,\alpha) \cdot I_L Z_L \qquad \ldots\ldots (6.34)$$

Hence $\qquad \dfrac{I_L Z_L}{V_{a_2}} = \dfrac{(\alpha + 1)}{a^2 (1 + j \sqrt{3}\, \alpha)}$

and $\qquad \left| \dfrac{V'_{oc}}{V_{a_2}} \right| = \dfrac{1 + \alpha}{\sqrt{1 + 3\alpha^2}}$ $\qquad \ldots\ldots$ (6.35)

In a general case when the 3 phase voltages V_A , V_B , and V_C represent an unbalanced supply (i.e. both positive and negative sequence components are present) having a different frequency from the normal.

The output voltage V'_{oc} , of the negative sequence segregating circuit Fig. (6.1B), will then attain a value within the range,

$$\dfrac{1 + \alpha}{\sqrt{1 + 3\alpha^2}} \; |V_{a_2}| \; \pm \; \dfrac{1 - \alpha}{\sqrt{1 + 3\alpha^2}} \; |V_{a_1}| \qquad \ldots\ldots (6.36)$$

Expression (6.36) will be a maximum when the two sequence components are equal in magnitude. This gives the upper and lower limits of the output voltage as,

$$\dfrac{2}{\sqrt{1 + 3\alpha^2}} \; |V_{a_2}| \quad \text{and} \quad \dfrac{2\alpha}{\sqrt{1 + 3\alpha^2}} \; |V_{a_2}| \qquad \ldots\ldots (6.37)$$

The fractional error, therefore, due to frequency departure from normal, will not exceed the larger of the expressions

$$A = 1 - \dfrac{2}{\sqrt{1 + 3\alpha^2}} \quad \text{or} \quad B = 1 - \dfrac{2\alpha}{\sqrt{1 + 3\alpha^2}} \qquad \ldots\ldots (6.38)$$

It is expected that the two expressions given in eqn. (6.38)

should give zero fractional errors at normal frequency. This can be easily verified by putting "α" = 1.0.

A frequency departure of - 10%, f = 45 c/s and α = 0.9, for a supply with an unbalance factor "k" of 100%, i.e. of equal positive to negative sequence component, give rise to an error of not more than - 8%. Smaller values of the unbalance factor "k" will result in a corresponding decrease of error.

Fig. (6.2) gives the limits of the fractional error due to the departure of frequency from the normal system frequency as determined by expressions (A) and (B) of eqn. (6.38). It also shows that the maximum percentage error in the output voltage is less than the percentage deviation in frequency.

A similar procedure can be followed for the case when the reflected load impedance Z_L is small compared to R, thus giving eqn. (6.25) for the output voltage, namely:-

$$a\,V_{a_1}(1 - \alpha) + V_{a_2}(\alpha + 1) = a^2\left(\sqrt{3} + j\alpha\right)I_L \cdot \frac{R}{\sqrt{3}}$$

$$\cdots\cdots (6.39)$$

Following the same agrument, as before, for applying a balanced positive sequence or negative sequence supply alone having a frequency different from the normal system frequency then in the case of a balanced negative sequence supply when applied alone, the positive sequence component V_{a_1} = 0 in eqn. (6.39) thus giving :-

$\alpha = f/f_n$

f_n System normal frequency

FIG. (6.2)   LIMITS OF FREQUENCY ERROR FOR
NEGATIVE-SEQUENCE CIRCUIT.
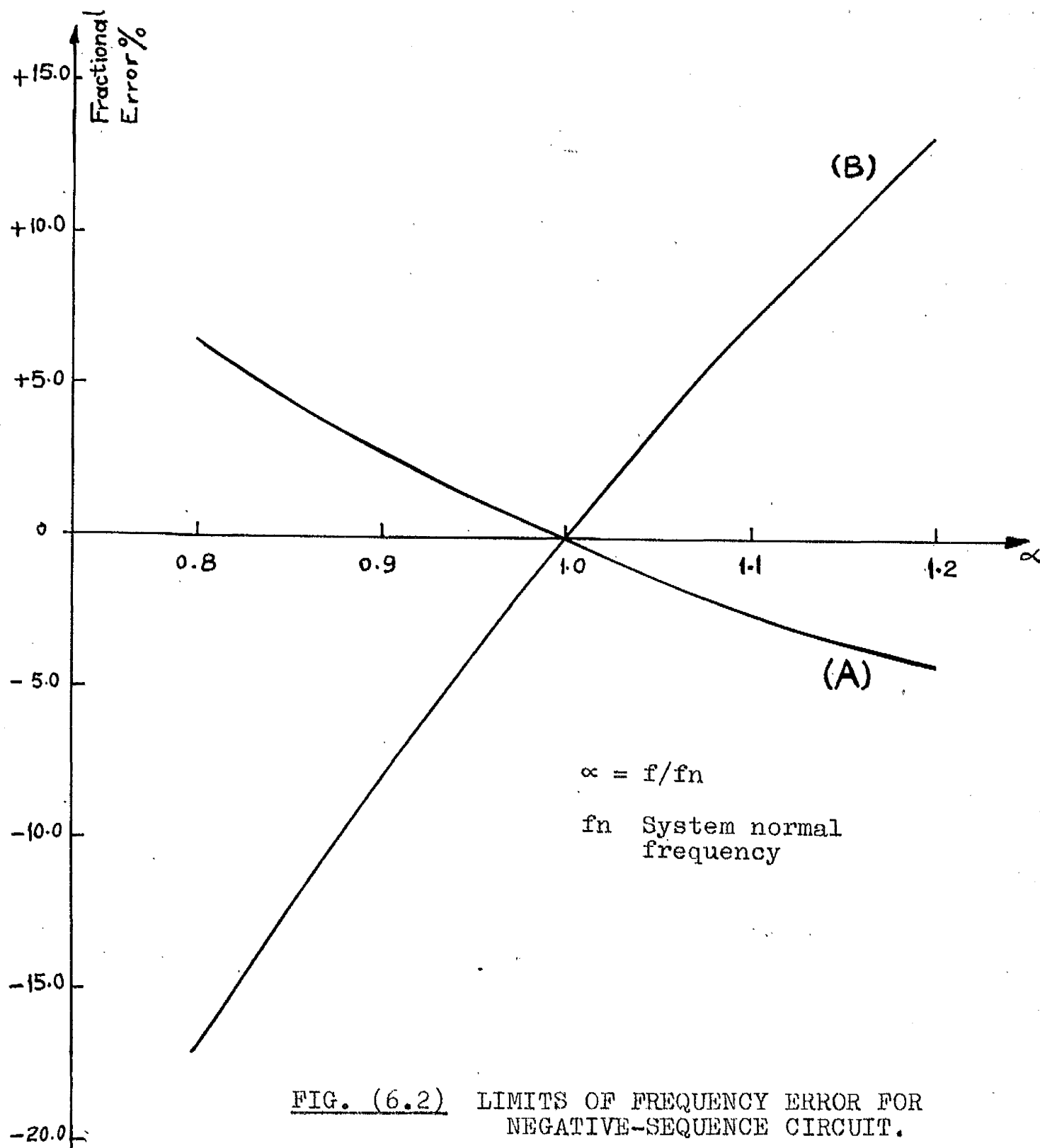
$$V_{a_2} (1 + \alpha) = a^2 (\sqrt{3} + j\alpha) . I_L \frac{R}{\sqrt{3}} \qquad \ldots\ldots \quad (6.40)$$

Therefore

$$\frac{I_L}{V_{a_2}} = \frac{(1 + \alpha) \sqrt{3}}{a^2 . (\sqrt{3} + j\alpha) R} \qquad \ldots\ldots \quad (6.41)$$

hence

$$\left| \frac{I_L}{V_{a_2}} \right| = \frac{\sqrt{3} (1 + \alpha)}{\sqrt{3 + \alpha^2} \ R} \qquad \ldots\ldots \quad (6.42)$$

Similarly, for the case of a balanced positive sequence supply, it can be proved that :-

$$\left| \frac{I_L}{V_{a_1}} \right| = \frac{\sqrt{3} (1 - \alpha)}{\sqrt{3 + \alpha^2} \ R} \qquad \ldots\ldots \quad (6.43)$$

Following the same procedure as before, the output will attain a value within the range given by :-

$$\frac{\sqrt{3} (1 + \alpha)}{\sqrt{3 + \alpha^2} \ R} \left| V_{a_2} \right| \pm \frac{\sqrt{3} (1 - \alpha)}{\sqrt{3 + \alpha^2} \ R} \left| V_{a_1} \right| \qquad \ldots\ldots \quad (6.44)$$

This expression is a maximum when the magnitude of the two sequence components are equal, i.e. when the unbalance factor "k" of the applied voltages is 100%. In such a case the limits for the load current I_L are given by

$$\frac{2 \sqrt{3} \ V_{a_2}}{\sqrt{3 + \alpha^2} \ R} \qquad \text{and} \qquad \frac{2 \sqrt{3} \alpha \ V_{a_2}}{\sqrt{3 + \alpha^2} \ R} \qquad \ldots\ldots \quad (6.45)$$

Eqn. (6.17) gives the output load current at normal system frequency for the same loading conditions. From eqns. (6.17 and 45) the fractional error due to frequency deviation will not exceed the larger of the following expressions,

$$A = 1 - \frac{2}{\sqrt{3} + \alpha^2} \quad \text{or} \quad B = 1 - \frac{2\alpha}{\sqrt{3} + \alpha^2} \quad \ldots \ldots \quad (6.46)$$

Expressions (6.46) are in fact the same as those given before in eqn. (6.38) and therefore Fig. (6.3) also shows their variation w.r.t. α.

It can be seen that these maximum fractional errors depend in fact only on the frequency deviation, i.e. it cannot be modified by a rechoice of circuit parameters.

The analysis given above discusses the case of a negative sequence segregating circuit, Fig. (6.1B). The corresponding positive sequence segregating circuit is obtained by interchanging the capacitive branch Z_C with R, the output voltage of which is given in eqn. (6.7). A similar analysis can easily be made for its frequency response in exactly the same manner as for the case of the negative sequence circuit.

6.2.6 The Effect of Zero Sequence Component

In the previous analysis the zero sequence component was so far assumed to be absent from the voltage inputs V_A, V_B, and V_C of the unbalanced 3 phase system.

Primary currents of a power system would generally contain
zero sequence components, under fault conditions involving earth,
and therefore their presence in secondary quantities, currents or
voltages, should also be considered.

The circuit previously described has been developed further,
to give an output, even in the presence of zero sequence components,
equal or proportional to either the positive or the negative
sequence component of the applied unbalanced 3 phase voltages.

The modified circuit is shown in Fig. (6.3) where the outputs
are taken in the form of line quantities instead of as phase
quantities in the earlier design.

The 3 phase unbalanced voltages V_A, V_B, and V_C are
related to their sequence component by the general known equations,

$$V_A = V_0 + V_{a_1} + V_{a_2}$$

$$V_B = V_0 + a^2 V_{a_1} + a V_{a_2} \qquad \dots\dots (6.47)$$

$$V_C = V_0 + a V_{a_1} + a^2 V_{a_2}$$

Therefore

$$V_A - a V_B = (1 - a)V_0 + V_{a_2}(1 - a^2)$$

$$\text{and} \quad V_B - a V_C = (1 - a)V_0 + V_{a_2}(a - 1) \qquad \dots\dots (6.48)$$

Subtracting eqns. (6.48) gives:-

$$(V_A - a V_B) - (V_B - a V_C) = 3 V_{a_2} \qquad \dots\dots (6.49)$$
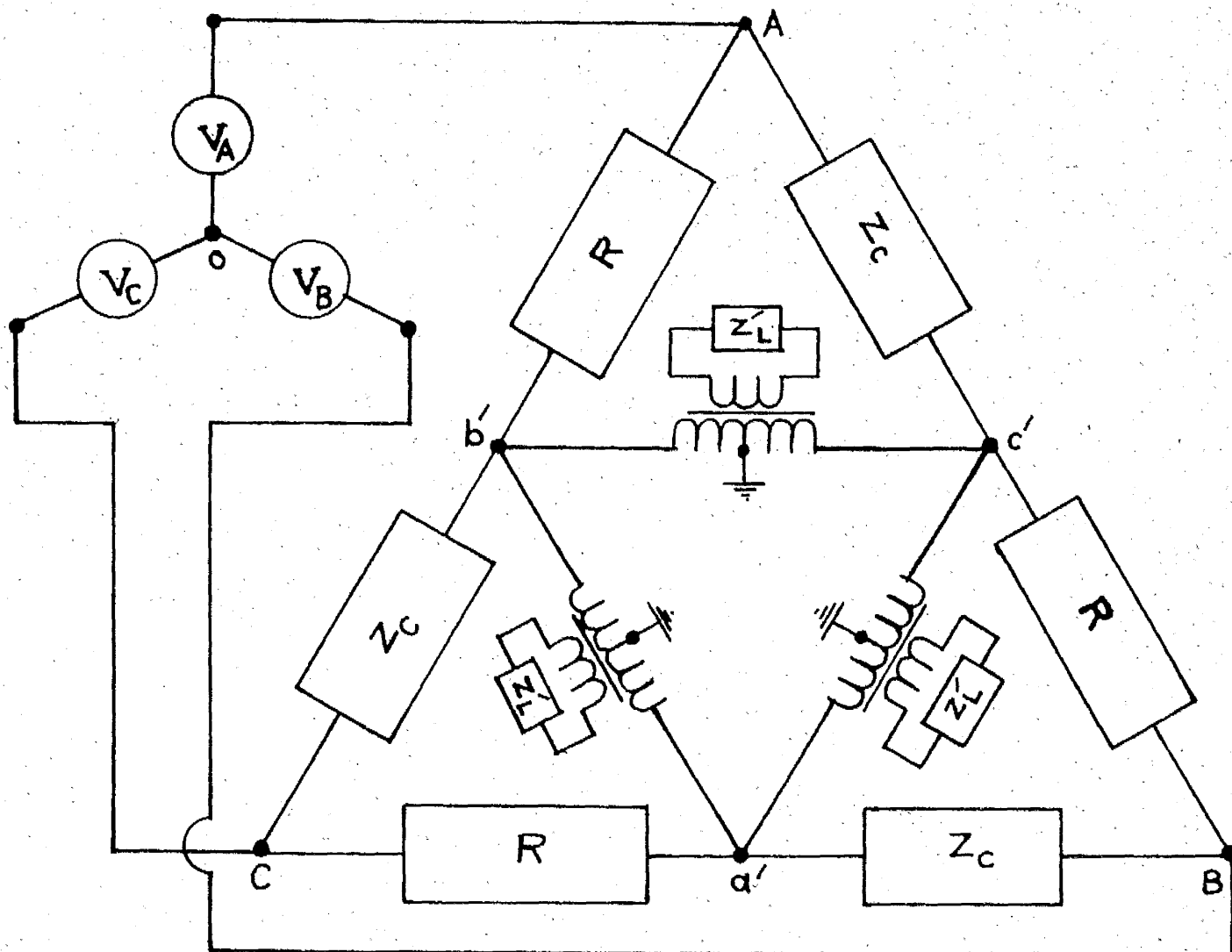
FIG. (6.3) MODIFIED NEGATIVE-SEQUENCE SEGREGATING CIRCUIT.
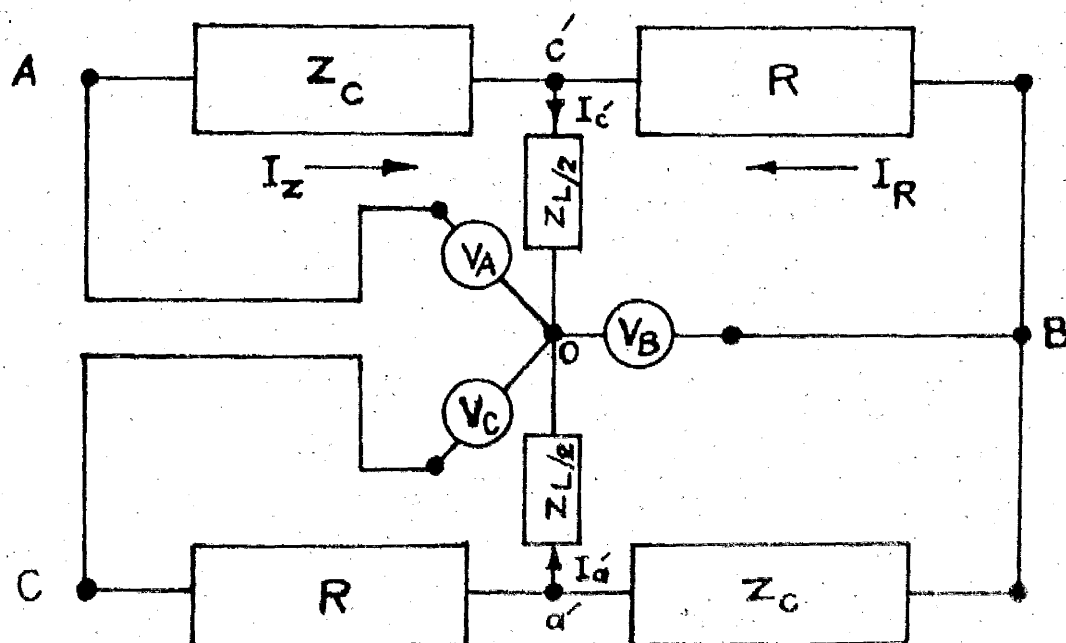
FIG. (6.4) BRANCHES "AB and BC" OF NEGATIVE-SEQUENCE CIRCUIT.

Eqn. (6.49) gives in fact $\sqrt{3}$ times the value of the negative sequence component of the line voltage V_{AB} say.

For the negative sequence segregating circuit shown in Fig. (6.3), assume the same relationship as in section (6.2) between the circuit elements, i.e. $Z_C = - aR$. Following the same analysis, as in section (6.2), by considering branches "AB" and "BC" Fig. (6.4) and applying superposition theorem, it can be proved that :-

$$I_{c'} = \frac{V_A - a\,V_B}{- a\,Z_L\left[\frac{R}{Z_L} + (1 - a^2)\right]} \qquad \ldots\ldots (6.49)$$

and

$$I_{a'} = \frac{V_B - a\,V_C}{- a\,Z_L\left[\frac{R}{Z_L} + (1 - a^2)\right]} \qquad \ldots\ldots (6.50)$$

where Z_L is an equivalent load impedance referred to the primary side of the output transformers. The current in the primary of the output transformer is given by :-

$$I_{a'c'} = I_{a'} - I_{c'} \qquad \ldots\ldots (6.51)$$

Substituting from eqns. (6.49) and (50) in (6.51), it gives:-

$$I_{a'c'} = \frac{(V_B - a\,V_C) - (V_A - a\,V_B)}{- a\,Z_L\left[\frac{R}{Z_L} + (1 - a^2)\right]} \qquad \ldots\ldots (6.52)$$

From eqns. (6.49) and (6.52) it follows that :-

$$I_{a'c'} \cdot Z_L = V_{a'c'} = a^2 \cdot \sqrt{3}\, V_{a2} \cdot \frac{\sqrt{3}}{\left[\frac{R}{Z_L} + (1 - a^2)\right]} \qquad \ldots\ldots (6.53)$$

It can be seen from eqn. (6.53) that the product $(I_{a'c'}.Z_L)$ is the voltage across the primary of the output transformer and $\sqrt{3}\ V_{a_2}$ is the magnitude of the negative sequence voltage component of the line voltages.

6.2.7 Performance of the Segregating Network
Associated with Ironless-Core C.T.s

A set of three ironless-core C.T.s (linear couplers), each having an output rating of 9.8 V/KA primary current, are used as supply sources for the negative sequence segregating circuit, Fig. (6.3), and its corresponding positive sequence one.

The current in the primary circuit of the linear couplers is supplied from a protective gear test bench designed to simulate a transmission line under healthy and faulty conditions. The maximum rated current for this bench is about 50 A for a duration of a few minutes.

Ironless-core C.T.s are suitable for operating from a primary-bar as well as a wound one.

In order to obtain a reasonable output from the available linear couplers, a 20 turn primary winding was used, thus giving about 10 V output at the maximum rated current of the test bench.

These ironless-core C.T.s are not ideal voltage sources and therefore have internal impedances. The magnitude of the average internal impedance of the linear couplers is about 20Ω and is

composed of almost equal resistive and inductive parts, at 50 c/s.
The resistances of the toroids differ a little between the 3
couplers on the three phases but the difference was, however, less
than 5% in this case.

This difference in resistance does not have any effect on
the output of the toroids since it is governed by the mutual
inductance "m" of the individual toroids, as explained in section
(3.2). If the primary currents on the 3 phases are assumed to be
balanced, then the couplers output voltages are also balanced, within
an error almost equal to that existing on the primary current.

In order to evaluate this error, due to the accuracy of the
winding of each toroid, a current was passed in the primary circuit
of the couplers connected in series, and their open-circuit output
voltages $V_{o.c.}$ were measured by an accurate valve-voltmeter.
The following results are recorded :-

$I_{primary}$ = 14.3 A.

$V_{o.c.}$ "A"	2.72 V
$V_{o.c.}$ "B"	2.73 V
$V_{o.c.}$ "C"	2.72 V

From the above results, it can be seen that the accuracy
of the mutual inductance to which the individual coils are wound

is less than 0.4%.

This error is important in determining the stability limit
of any summation scheme operating from ironless-core C.T.s as
explained in section (4.4.1).

The three secondaries of the ironless-core C.T.s were then
connected in a star configuration, while their primaries were each
in series with one phase of the transmission line of the test bench.

The secondaries are connected in turn as supply inputs to
the segregating circuit, Fig. (6.3). The impedance reflected by
this circuit on each phase of the supply is given by eqns. (6.14
and 15). For the circuit designed with the particulars given in
section (6.2.1), the input impedance is about 1.5 K ohms. Comparing
this value with the internal impedance of a coupler (about 20 ohms)
it can be seen that the couplers are operating almost at open-
circuit conditions.

The output transformers, of the circuit of Fig. (6.4), were
disconnected, or alternatively assumed to have a unity transformation
ratio. The following tests were carried out on the couplers/
(positive and negative) sequence segregating circuits:-

(a) 3 Phase fault.

A 3 phase fault was applied on the transmission line of the
test bench. A resistive load of 82 ohms was connected across
the output terminals of the positive sequence segregating circuit
of the type shown in Fig. (6.3). The following table gives the

recorded measurements.

	Phase "A"	Phase "B"	Phase "C"
I_p (A)	22.1	22.15	22.0
$V_{o.c.}$ (v)	4.3	4.3	4.28
$V_{sec.}$ (v)	4.26	4.23	4.23
I_L (m.A.)	4.54	4.50	4.50

<u>"ABC" Fault</u>

Since the load impedance in this case is very small compared to R of the circuit, then the output current in the load I_L as given by eqn. (6.53) can be calculated by putting $R/Z_L \gg 1$. From the results it can be seen that $V_{sec.}$ (which is the secondary output of voltage of the couplers when connected to the segregating network) does not differ much from the $V_{o.c.}$, i.e. the couplers are operating near enough to open-circuit conditions.

The overall error in the load currents, including an unbalance of about 1% in primary current, is less than 1.5%.

The whole circuit arrangement, with such loading conditions, has an equivalent sensitivity of 1.0 m.A/100A bar-primary current.

(b) Double phase faults (not involving earth)

The results mentioned in this case refer to the negative

sequence segregating circuit shown in Fig. (6.3). The loads to the circuit were 3 measuring instrument having an input impedance of 1.0 KΩ, on that particular range of measurement. For an "A - B" fault, the recorded values are shown in the table below. Measurements were carried out with only one instrument to avoid the effects of different accuracies and errors.

	Phase "A"	Phase "B"	Phase "C"
I_p (A)	18.55	18.55	0
$V_{sec.}$ (v)	3.76	3.75	0
V_L (v)	1.39	1.4	1.38

"A - B" Fault

Since the load impedance Z_L is now comparable to the circuit element R , the output voltage V_L across the load impedance, is given by eqn. (6.53). Under this fault condition, the negative sequence outputs of the line voltages should be equal, but a small error in V_L due to the accuracy of the measuring instrument can be noticed, this error is, however, within $\pm$ 1.0%.

This circuit arrangement has an equivalent sensitivity, under the prevailing loading conditions, of 350 m.V/100 A bar-primary current.

(c) Double phase to earth faults

The same negative sequence circuit, Fig. (6.3), has undergone these tests having two different loading conditions. In one case the load was the same measuring instruments described in the above test and in the 2nd case an electronic valve-voltmeter was used to simulate the case of $Z_L \longrightarrow \infty$. For "B - C/E" fault case on the transmission line of the test bench, the following results were observed:-

		Phase "A"	Phase "B"	Phase "C"
I_p	(A)	0	21.8	21.45
$V_{sec.}$	(v)	0	4.23	4.18
V_L	(i)	1.85	1.82	1.8
(v)	(ii)	2.32	2.32	2.3

"B - C"/E Fault

Under this fault condition, and with the available settings of the simulated transmission line constants on the test bench, closer accuracy of primary currents was not possible due to a slight unbalance in the supply to the test bench. With an error in the primary currents of $\pm$ 1%, the sequence network output voltage, in case (ii) of high load impedance, was within $\pm$ 1.2%. The error was a little higher in the case (i) with the lower load

impedance, this was attributed to the primary current error and
the accuracy of the measuring instrument.

The overall sensitivity of the circuit, under cases (i) and
(ii) of loading conditions, was equivalent to 400 m.v. and 500 m.v/
100 A bar-primary current, respectively. Such outputs make the
circuit arrangement suitable for application with transistorised
relaying circuits.

(d) Single phase to earth faults.

The same negative sequence network was tested under a single
phase to earth fault on phase "A" of the simulated transmission line.
The loading condition was, as mentioned earlier, such that $Z_L \rightarrow \infty$.
The measurements are recorded in the following table :-

		Phase "A"	Phase "B"	Phase "C"
I_p	(A)	22.0	0	0
$V_{o.c.}$	(v)	4.27	0	0
$V_{sec.}$	(v)	4.24	0	0
V_L	(v)	2.36	2.4	2.36

<u>"A"/E Fault</u>

Under this fault condition it is well known that the fault
current is 3 times the value of any of the sequence components,

since $I_0 = I_1 = I_2$. The output voltage V_L is in fact the negative sequence component of the line current, i.e. $\sqrt{3}\, I_2$.

From the table above it can be easily verified that $V_L \simeq V_{o.c.}/\sqrt{3}$, also the difference between $V_{o.c.}$ and $V_{sec.}$ shows that the couplers are near enough to o.c. conditions. The error between the calculated value of the negative sequence of the line voltage and the measured one does not exceed 4%, including the loading effect on the couplers as well as measurement errors.

The overall sensitivity of total circuit arrangement, for such a loading condition, is equivalent to about 550 m.V./100 A bar-primary current. This sensitivity is satisfactory for transistorized relaying circuits where amplification may be considered if required.

In all the above tests the ironless-core C.T.s (linear couplers) used have a transfer impedance of about 10 V/KA primary current, i.e. the sensitivity is about 1000 m.V/100 A on open-circuit.

If the 1000 m.V are obtained under, say single phase/E fault, then for a sequence voltage segregating circuit the sensitivity available will be 330 m.V./100 A. Comparing this with the corresponding sensitivity obtained above for similar fault conditions, the advantage of producing the output of the segregating circuit in the form of line voltages rather than phase components can be easily seen.

6.3 Simple Circuits for Extraction of Sequence Currents Associated with Linear Couplers

6.3.1 General Considerations

For the segregating circuits previously discussed it is clear that the output transformers play an essential part in the design and in the output characteristics of the circuit. This has rather a two sided point of view, on one hand it is advantageous since it is the only variable element in the design of the segregating network to meet different loading conditions. On the other hand, the presence of the transformer was considered as a rather expensive item thus contributing a large sum of the cost of the segregating network.

On economical grounds, other circuits, of a more simpler nature, have been developed to extract sequence component currents from ironless-core C.T.s (linear couplers) and as far as possible iron core chokes have been eliminated on grounds of cost as well as space economy.

In designing these circuits simplicity and lower cost, without sacrificing a great deal in performance characteristics, are the two main aims to be achieved. The fact of associating the output of these circuits with transistorised relaying circuitry was also kept in mind.

Linear couplers have, in general, low VA output but sufficient enough for application with transistorised relaying schemes where the input would be of the order of a few milliamps.

Fig. (6.5) shows a schematic diagram for the way suggested to extract, e.g. negative sequence current, from the secondaries of three linear couplers (V_A , V_B , and V_C) connected in star. The negative sequence voltage of the reference phase "A" is given by eqn. (6.1). This arrangement is a direct representation of eqn. (6.1) assuming that the shifting network produce a voltage phase shift for the angle indicated inside the squares. It can, therefore, be seen that i_L is proportional to the sequence component voltage V_{a_2} :-

$$i_L = \frac{1}{R_L} (v_a + v_b + v_c) = \frac{C}{R_L} (V_A + a^2 B_B + a V_C)$$

$$= \frac{3C}{R_L} \cdot V_{a_2} = k_2 \cdot V_{a_2} \qquad \ldots \ldots (6.54)$$

where k_2 is a constant, and "C" is the attenuation factor of any of the phase shifting circuits.

Circuits to provide a voltage phase shift of the order of $\pm 120^{\circ}$ are rather complicated as well as expensive and to some extent impractical to design avoiding the use of transformers.

Eqn. (6.1), for the negative sequence component, can be re-written as follows :-

$$- V_{a_2} = \frac{1}{3} (- V_A + V_B \underline{/60^{\circ}} + V_C \underline{/- 60^{\circ}}) \qquad \ldots \ldots (6.55)$$

Fig. (6.6) shows a circuit, in a schematic form, to give a representation of eqn. (6.54). From the figure it can be shown
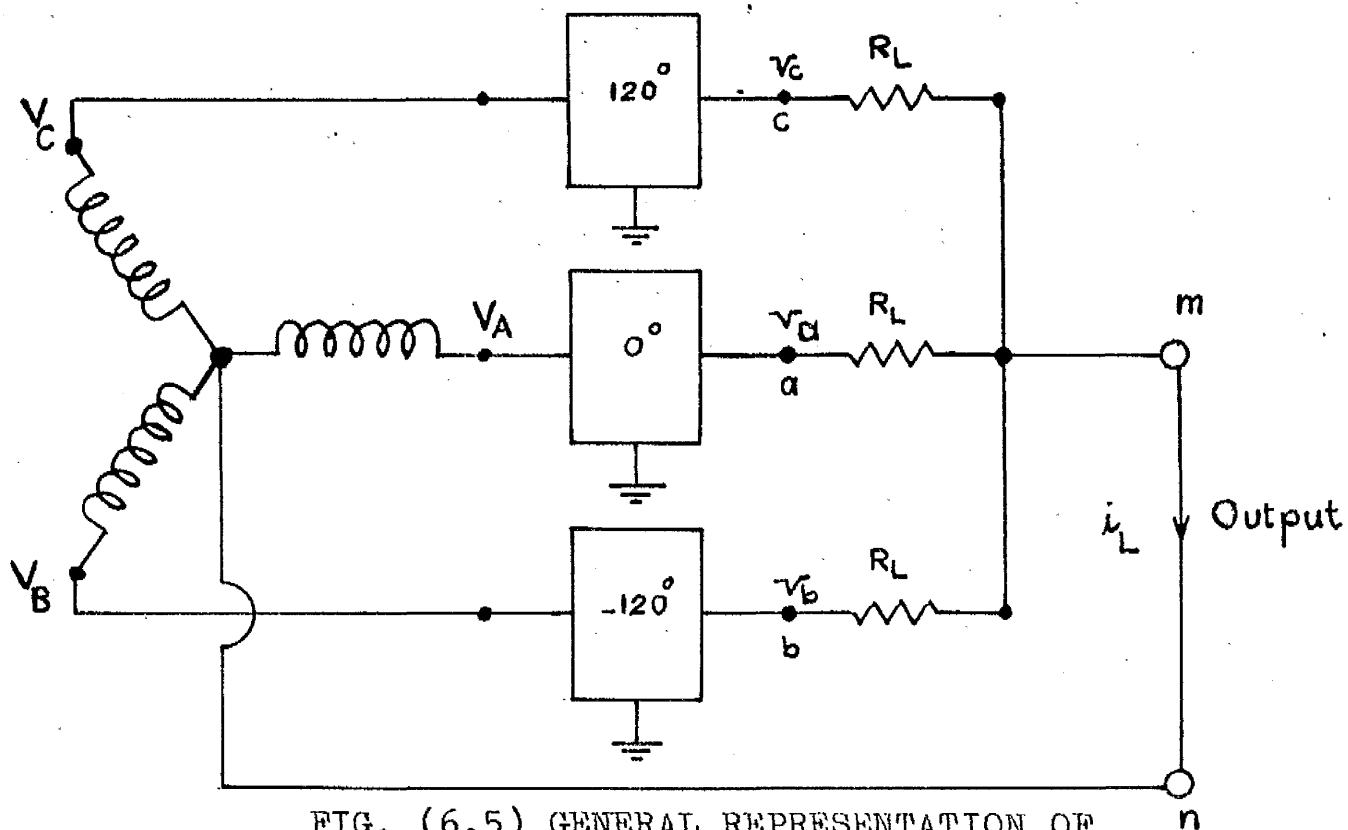
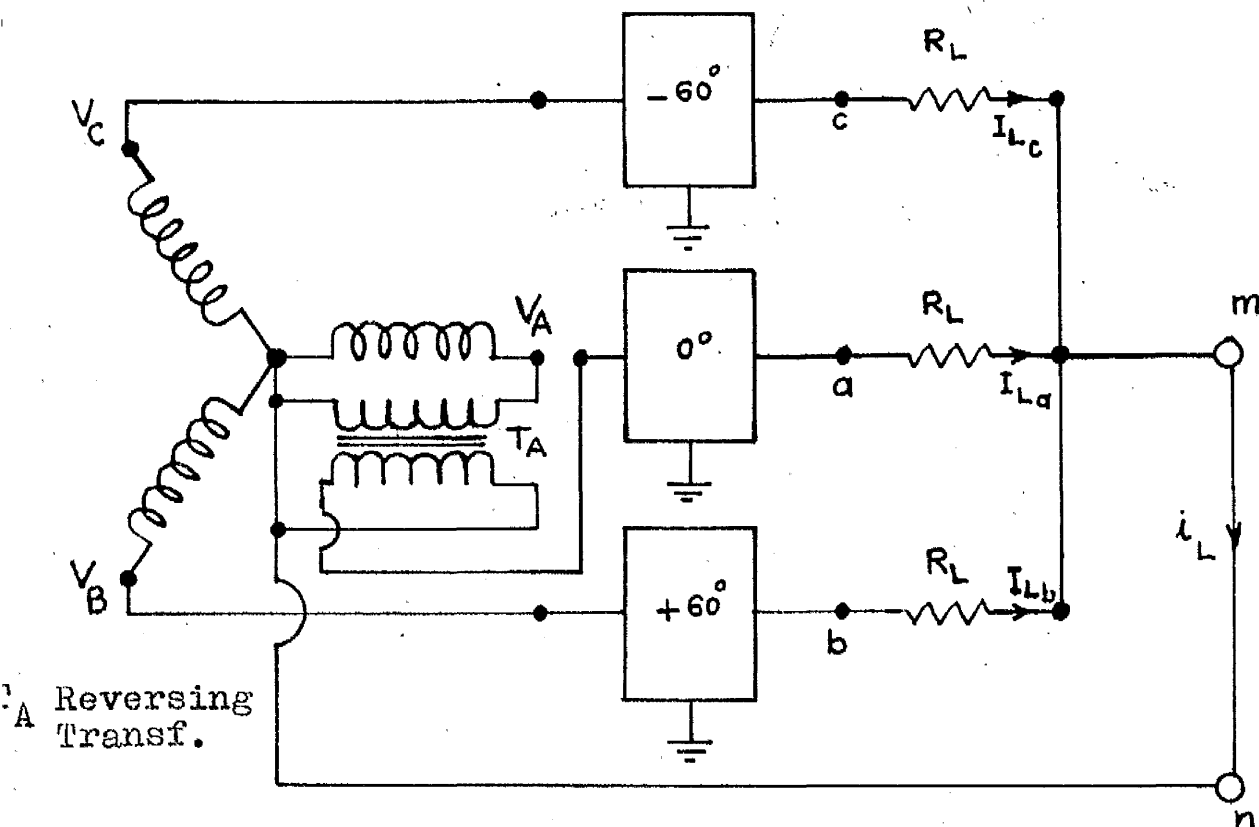FIG. (6.5) GENERAL REPRESENTATION OF
NEGATIVE SEQUENCE CIRCUIT

FIG. (6.6)   ALTERNATIVE REPRESENTATION OF
NEGATIVE SEQUENCE CIRCUIT

that the output current i_L is proportional to $(- V_{a_2})$.

Fig. (6.6) is in fact a direct representation for eqn. (6.55) and it is noticed that only one transformer is needed on the reference phase "A". This can be further eliminated by turning the connections of the linear coupler of that particular phase, thus providing $(- V_A)$ instead of V_A. The presence of transformers in the circuit can therefore be avoided completely if the set of linear couplers are only used for supplying this segregating circuit. If the linear couplers are used simultaneously for other purposes, then two identical linear coupler windings on phase "A" to produce V_A as well as $(- V_A)$ may be used or alternatively one linear coupler on phase "A" with a reversing transformer.

The phase shifting circuits shown in Fig. (6.6) are required to provide voltage shifts of $\pm 60^o$, which can be easily achieved in practice without further complications.

There is, of course, a similar circuit for extracting the positive sequence component as given by the following expression :-

$$- V_{a_1} = \frac{1}{3}(- V_A + V_B. \underline{/- 60^o} + V_C. \underline{/+ 60^o}) \quad \ldots\ldots \quad (6.56)$$

Such circuits are designed to produce output currents, between terminals "m and n", which can be used as a relaying quantity. The only condition to be noticed is that the relay input impedance as seen between the terminals "mn" should be very small compared to R_L, i.e. $R_r \lessless R_L$. A transistor amplifier in a common

base configuration would be ideal for such conditions.

To implement the instructions given in eqns. (6.55 and 56), voltage phase shifts of $\pm 60^{o}$ are required to be performed electrically. Such phase shifts could be achieved by the use of merely resistive capacitive circuits, thus avoiding the use of bulky and expensive iron-cored inductors.

6.3.2 Circuit Design

In the previous section it has been shown that the current $"i_L"$, Fig. (6.6), is proportional to the negative sequence component of $"V_A"$. This current is the sum of the voltages at points a, b, and c divided by R_L.

Assuming that the phase shifting circuits in Fig. (6.6) introduce no magnitude attenuation, and cause just a vector rotation of the phase voltages, then the voltages at a, b, and c will be equal to the phase voltages $-V_A$, V_B, and V_C respectively.

In general, phase shifting circuits would also cause an inherent magnitude attenuation. Two types of phase shifting circuits are examined and analysed for their magnitude attenuation and frequency response.

6.3.3 Single and Double Stage Circuits

It has been mentioned in section (6.3.1) that circuits designed to produce $\pm 60^{o}$ voltage shifts are required for segregating circuits of the type shown in Fig. (6.6).

In a single stage circuit, the phase shift θ^o is produced by one basic circuit (stage). The same phase shift may be obtained by a composite circuit of two or more identical stages in tandem each providing a phase shift $\theta_1^o = (\theta/\text{no. of stages})$. The following discussion will be devoted to single and double stage circuits only.

Fig. (6.7A and B) show two RC circuits to produce -60° and -30° voltage shifts respectively. It can be proved that:-

$$\omega C_1 R = \sqrt{3} \, , \, |V_{ot}/V_{in}| = 0.5$$
$$\omega C_2 R = {}^1/\sqrt{3} , |V_{c_2}/V_{in}| = 0.866 \qquad \ldots\ldots (6.57)$$

For a two stage circuit of the type shown in Fig. (6.7B) each stage has to provide a phase shift of -30°, assuming that the loading effect of the second stage on the first is negligible, then the total shift will be -60°. Such a circuit is shown in Fig. (6.8D), where "n" is a scalar factor equal to the ratio of the resistive branches of the second stage to that of the first.

For the first stage V_{o_2}/V_{in} is given by eqn. (6.57) and provided $n \gg 1$, then the loading effect of the second stage on the first can be neglected, and consequently

$$|V_{ot}/V_{in}| \simeq (0.866)^2 = 0.75 \qquad \ldots\ldots (6.58)$$
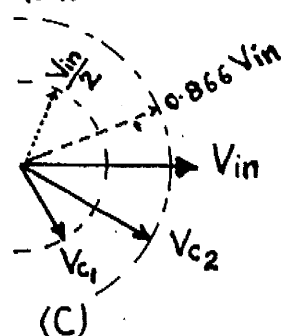
Comparing eqn. (6.57 and 58) it can be noted that a two stage
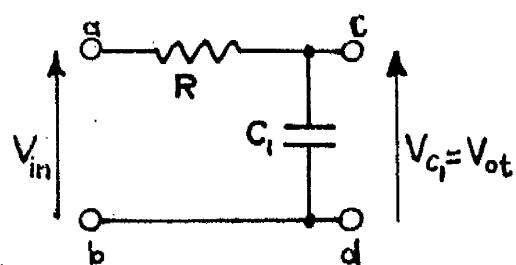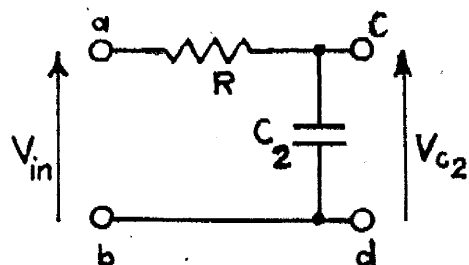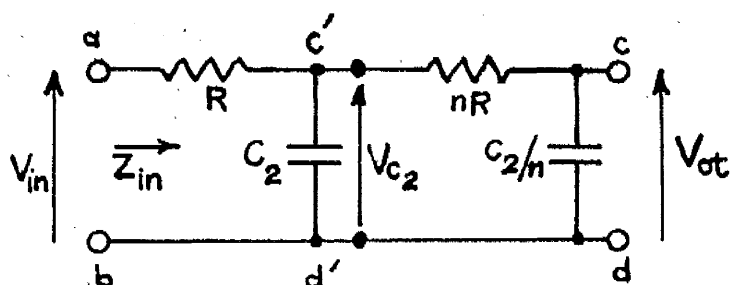
FIG. (6.7)   SINGLE AND DOUBLE STAGE PHASE SHIFTING CIRCUITS.
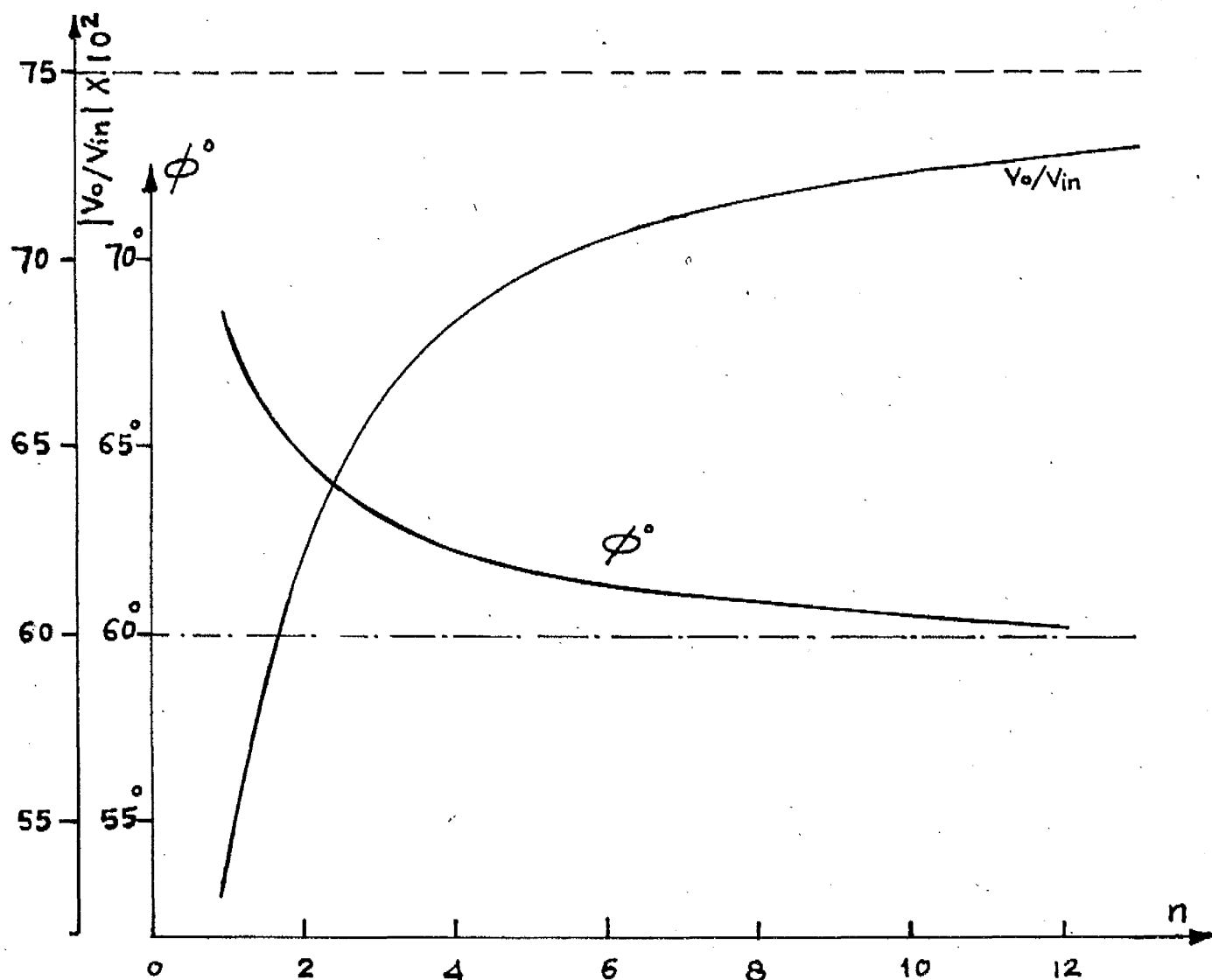
FIG. (6.8)   OUTPUT VOLTAGE AND PHASE ANGLE OF
COMPOSITE CIRCUIT

circuit, has a larger output voltage for the same phase shift and input voltage V_{in}, i.e. offers less attenuation. On the other hand, for a general case, the loading effect of the second stage on the first should be taken into consideration.

For a -30° phase shift/stage, the relation between the circuit elements are:

$$\omega C_2 R = {}^1\!/\!\sqrt{3} \quad \text{and} \quad \omega \cdot \frac{C_2}{n} \cdot nR = {}^1\!/\!\sqrt{3} \quad \ldots\ldots (6.59)$$

The impedance Z_{in} presented by the circuit to its input terminals ab, Fig. (6.7D), assuming terminals cd are open circuited, is given by :-

$$Z_{in} = \frac{n(R - j/\omega C_2)^2 - jR/\omega C_2}{nR - j(n+1)/\omega C_2} = \frac{R\left[-2n - j\sqrt{3}(1+2n)\right]}{n - j\sqrt{3}(1+n)}$$

$$\ldots\ldots (6.60)$$

From which it can be shown that :-

$$V_{ot}/V_{in} = \frac{3n}{2n + j\sqrt{3}(2n+1)} = \frac{3n}{\left[16n^2 + 12n + 3\right]^{1/2}}\angle-\emptyset^{\circ}$$

where

$$\emptyset = \tan^{-1}\sqrt{3}(1 + {}^1\!/\!2n)$$

$$\ldots\ldots (6.61)$$

or

$$\left|V_{ot}/V_{in}\right| = \frac{3n}{\left[16n + 12n + 3\right]^{1/2}} \qquad \ldots\ldots (6.62)$$

Fig. (6.8) gives the variation of expression (6.62) against "n". The value of $\left|V_{ot}/V_{in}\right|$ reaches the limit of 0.75 given by eqn. (6.58) as "n" $\rightarrow \infty$, and also the figure shows the variation of $\underline{/\phi^{o}}$ the phase shift with "n". The angle $\underline{/\phi^{o}}$ approaches -60° as "n" tends to infinity, which corresponds to the case when the loading effect of the second stage is negligible.

Fig. (6.9A and B) show a voltage phase shifting circuit for shifts of 60° and 30° respectively. For such phase shifts it can be easily shown that:-

$$\omega C_1 R = {}^{1}/\sqrt{3} \quad \text{and} \quad \left|V_{ot}/V_{in}\right| = 0.5$$

$$\text{and} \quad \omega C_2 R = \sqrt{3} \quad \text{and} \quad \left|V_R/V_{in}\right| = 0.866$$

$$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad \ldots\ldots (6.63)$$

The two stage circuit shown in Fig. (6.9D) comprises two circuits, similar to that of Fig. (6.9B), connected in tandem. Each stage provides for a 30° phase shift and, provided that the loading effect of the second stage on the first is negligible:-

$$\left|V_{ot}/V_{in}\right| \simeq (\sqrt{3}/2)^{2} = 0.75 \qquad\qquad \ldots\ldots (6.64)$$

This composite circuit gives therefore, a larger output voltage than the circuit shown in Fig. (6.9A), for the same input voltage.

For the circuit shown in Fig. (6.9C), and assuming that the terminals cd are open-circuited, $\underline{/}$ the effect of the load at "od" will be introduced in a later stage, sec. (6.3.5) $\underline{/}$, the input impedance Z_{in} presented by the circuit between terminals "ab"
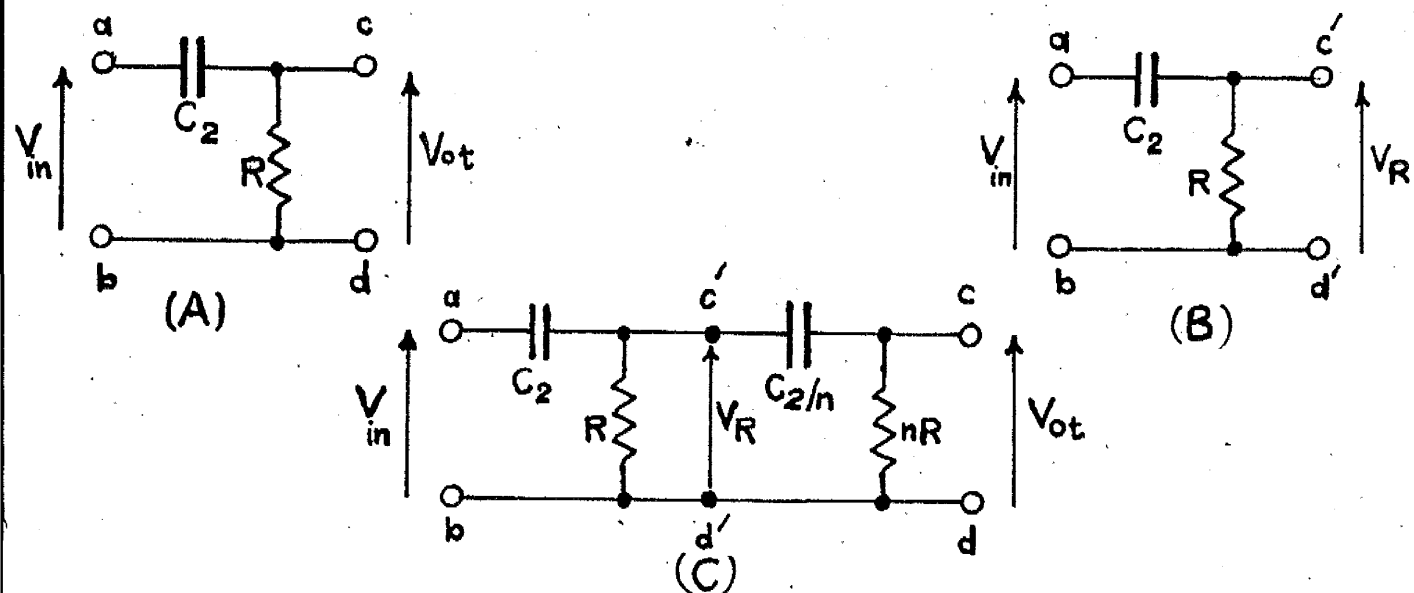
FIG. (6.9)   SINGLE AND DOUBLE STAGE PHASE SHIFTING CIRCUITS.
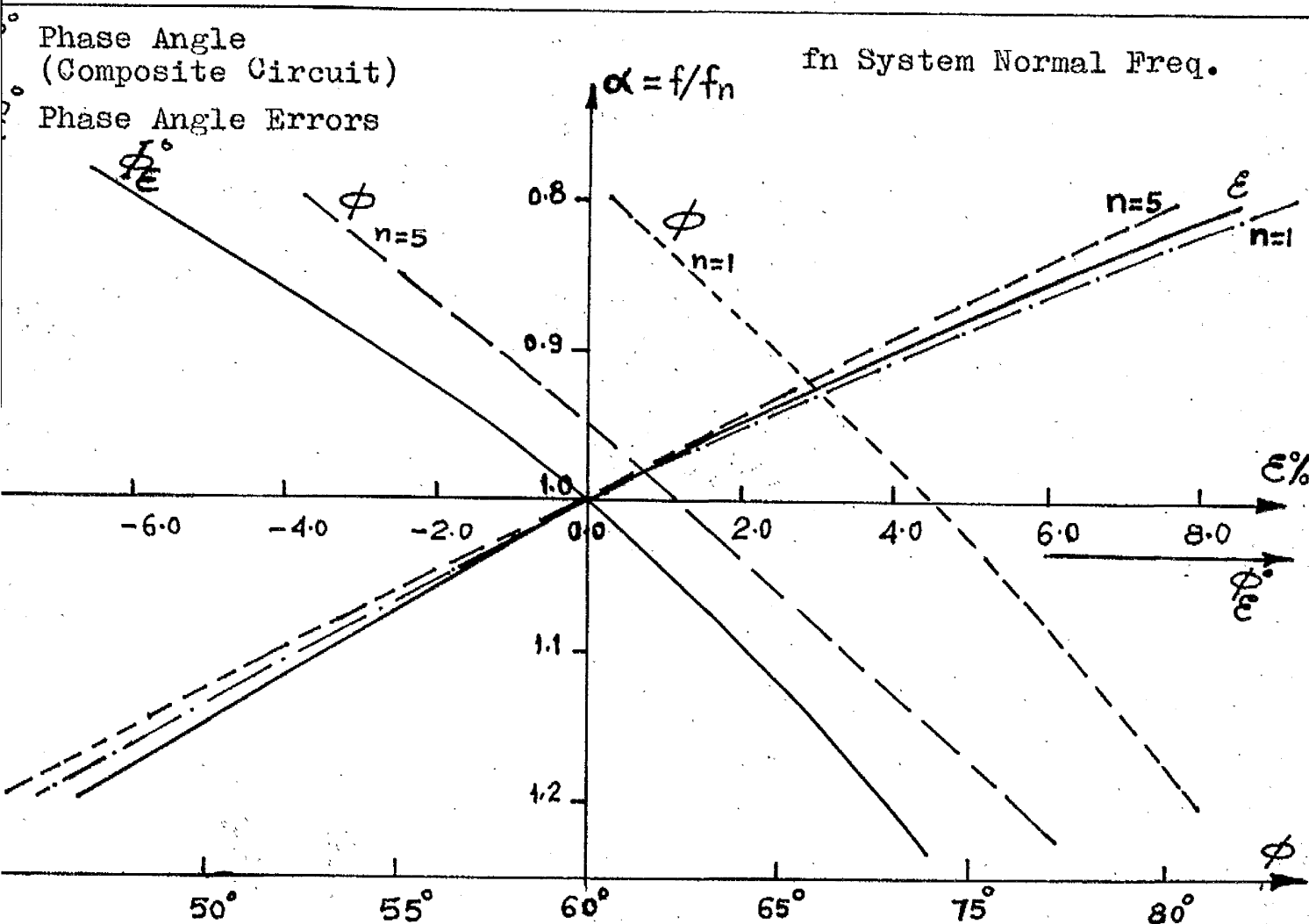
FIG. (6.10)   FREQUENCY DEVIATION ERRORS
(FOR CIRCUITS FIG. 6.7)

is given by:-

$$Z_{in} = \frac{n(R - 1/\omega^2 C_2^2) - jR/\omega C_2 (1 + 2n)}{R(1 + n) - j/\omega C_2} = \frac{R \angle 2n - j\sqrt{3}(2n + 1) \rfloor}{\sqrt{3} \angle \sqrt{3}(n + 1) - j \rfloor}$$

$$\ldots\ldots (6.65)$$

Hence it can be proved that,

$$V_{ot}/V_{in} = \frac{3n}{2n - j\sqrt{3}(1 + 2n)} = \frac{3n}{\angle 16n^2 + 12n + 3 \rfloor^{1/2}} \angle + \phi$$

where

$$\phi = \tan^{-1} \sqrt{3}(1 + 1/2n)$$

$$\ldots\ldots (6.66)$$

Therefore

$$\left| V_{ot}/V_{in} \right| = \frac{3n}{\angle 16n + 12n + 3 \rfloor^{1/2}} \qquad \ldots\ldots (6.67)$$

Eqns. (6.62) and (6.66) give the same expressions, except that the angle ϕ was negative in the first case and positive in the second, i.e. a lagging and a leading phase shift respectively. Consequently Fig. (6.8) would also represent the variations of expression (6.67) with n.

6.3.4 Frequency Response and Error

All segregating circuits are frequency sensitive devices and the departure of the system frequency from its normal value will cause an error in the output of the segregating circuit.

The open circuit secondary voltage of a linear coupler is

given by $V_{o.c.} = - j\omega m I_p$, where I_p is the primary current. When the frequency of the system deviates from its normal value the output voltage of the linear coupler will vary in direct proportion to frequency.

If "α" represents the actual frequency as a fraction of the normal value, the open circuit output voltage of the linear coupler will be given by :-

$$V'_{o.c.} = - j\omega\alpha m I_p = \alpha V_{o.c.} \qquad \ldots\ldots (6.68)$$

Segregating circuits fed from linear couplers would therefore have a varying input voltage with frequency and such an effect, added to the change in the value of the reactive impedance elements, have to be considered as sources of frequency errors.

In practice the effect of frequency errors has to be considered only at high load currents approaching low fault settings, e.g. earth faults in resistance earthed system.

For the circuit Fig. (6.7A) the output V_{ot} is related to the input voltage V_{in} by :-

$$V_{ot}/V_{in} = \frac{1}{1 + j\omega C_1 R} \qquad \ldots\ldots (6.69)$$

If the frequency of the system deviates from the normal value, then the output V_o' of the circuit fed from a linear coupler V_{in}' would be given by:-

$$V_{ot}'/V_{in}' = V_{ot}'/\alpha \cdot V_{in} = \frac{1}{1 + j\omega C_1 \alpha R} = \frac{1}{\left[1 + \alpha^2 \omega^2 R^2 C_1^2\right]^{1/2}} \underline{/-\phi^o}$$

where

$$\phi = \tan^{-1}(\alpha \omega C_1 R)$$

$$\ldots \ldots (6.70)$$

For a phase shift of -60°, $\omega C_1 R = \sqrt{3}$. Substituting this in (6.70) it follows:-

$$\left|V_{ot}'/V_{in}'\right| = \frac{1}{\sqrt{1 + 3\alpha^2}} \qquad \ldots \ldots (6.71)$$

Under normal frequency conditions, $\left|V_o/V_{in}\right| = 0.5$ and, therefore, the increment "$\mathcal{E}$" due to frequency deviation can be expressed as :-

$$\mathcal{E} = -0.5 + \frac{1}{\sqrt{1 + 3\alpha^2}}$$

"α" will generally be little different from unity for practical applications.

Fig. (6.10) shows the percentage increment $\mathcal{E}$ % against the frequency departure over the range of $\alpha = 0.8$ to 1.2, i.e. $40 - 60$ c/s. It is clear that expression (6.72) gives zero increment at $\alpha = 1.0$, i.e. at 50 c/s.

It can be seen from Fig. (6.10) that $\mathcal{E}$ % is always smaller than the percentage deviation in the frequency itself. The figure also illustrates the phase angle error $\phi_{\mathcal{E}}^o$, in degrees, due to frequency deviation. For the practical range over which the

frequency of the British grid system varies, i.e. between $f = 48$ to 52 c/s, ϕ_3^0 does not exceed $\pm 1^0$.

The input impedance of the two stage circuit, Fig. (6.7D), as seen between terminals ab is given by eqn. (6.60) and therefore a general relationship for V_{ot}/V_{in} can be obtained, namely :-

$$V_{ot}/V_{in} = \frac{n}{n(1 - \omega^2 C_2^2 R^2) + j\omega C_2 R(1 + 2n)} \quad \ldots\ldots (6.74)$$

If "α" gives the actual frequency of the system as a fraction of the normal value, (as the linear coupler output V'_{in} varies with frequency, as mentioned earlier), then :-

$$V'_{ot}/V'_{in} = V'_{ot}/\alpha \cdot V_{in} = \frac{n}{n(1 - \alpha^2 \omega^2 C_2^2 R^2) + j(2n + 1)\alpha} \quad \ldots\ldots (6.75)$$

Substituting for $\omega C_2 R = 1/\sqrt{3}$, for the required phase shift then,

$$V'_{ot}/V'_{in} = \frac{3n}{n(3 - \alpha) + j\sqrt{3}\,\alpha(2n + 1)} = |V'_{ot}/V'_{in}| \cdot \underline{/- \phi^0} \quad \ldots\ldots (6.76)$$

where

$$|V'_{ot}/V'_{in}| = \frac{3n}{[(3 + \alpha^2)^2 n^2 + 12\alpha^2 n + 3\alpha^2]^{1/2}}$$

and

$$\phi = \tan^{-1}\frac{\sqrt{3}\,\alpha(1 + 2n)}{n(3 - \alpha^2)}$$

$$\ldots\ldots (6.77)$$

Fig. (6.10) shows the increment $\mathcal{E}$ in the output voltage for the two cases of $n = 1$ and 5, against the frequency deviation as well as the variation of the angle ϕ as given by eqns. (6.77). It is noticed that for frequencies less than the normal value, i.e. $\alpha < 1$, the curve for the case of $n = 1$ gives higher errors than that of $n = 5$ while for $\alpha > 1$ the $n = 5$ case gives a little higher error. However, for a practical range of frequency deviation, i.e. from $f = 48$ to 52 c/s, all three types of circuits give incremental errors of almost the same magnitude. They are a great deal less than the frequency deviation itself, e.g. the increments are within $\pm 2\%$ for a frequency deviation of $\pm 5\%$.

The error in the phase angle ϕ for a two stage circuit decreases as "n" increases and the limit would be that of a single stage circuit and, in this respect, a single stage circuit to produce the phase shift would be preferred.

For the circuit shown in Fig. (6.9A), for a 60° voltage phase shift, the output voltage V_{ot}, when "cd" are open circuited is related to input voltage V_{in} by :-

$$V_{ot}/V_{in} = \frac{1}{1 - j/\omega C_1 R} \qquad \ldots\ldots (6.78)$$

When the frequency of the system deviates from normal, the output V_{ot}' related to a linear coupler input V_{in}' would be :-

$$V_{ot}'/V_{in}' = V_{ot}'/\alpha \cdot V_{in} = \frac{1}{1 - j/\omega C_1 \alpha R} = \frac{1}{\sqrt{1 + 1/\omega^2 C_1^2 \alpha^2 R^2}} \; \underline{/+ \phi^0}$$

where

$$\phi = \tan^{-1}\left(\frac{1}{\alpha \; \omega C_1 R}\right)$$

$$\ldots \ldots \; (6.79)$$

For a voltage phase shift of $+ 60^0$, $\omega C_1 R = 1/\sqrt{3}$ and by substitution in eqn. (6.79) gives :-

$$\left| V_{ot}'/V_{in}' \right| = \frac{\alpha}{\sqrt{3 + \alpha^2}} \qquad \ldots \ldots \; (6.80)$$

From eqns. (6.63 and 80), the increment $\mathcal{E}$ in the output voltage due to a frequency deviation is given by :-

$$\mathcal{E} = - 0.5 + \frac{\alpha}{\sqrt{3 + \alpha^2}} \qquad \ldots \ldots \; (6.81)$$

where "α" will generally be a little different from unity. Eqn. (6.81) gives $\mathcal{E} = 0$ for $\alpha = 1.0$, i.e. at normal frequency.

Fig. (6.11) gives $\mathcal{E} \%$ due to a frequency variation over the range from 40 to 60 c/s. It also shows the error in the phase angle ϕ^0 . This error does not exceed $\pm 1^0$ for the practical range of 48 to 52 c/s. It can be seen that generally the increment $\mathcal{E} \%$ due to frequency deviation is always smaller than the frequency departure itself.

If the two stage circuit, Fig. (6.9C), has been employed to produce a voltage phase shift of $+ 60^0$, i.e. $\omega C_2 R = \sqrt{3}$, then its
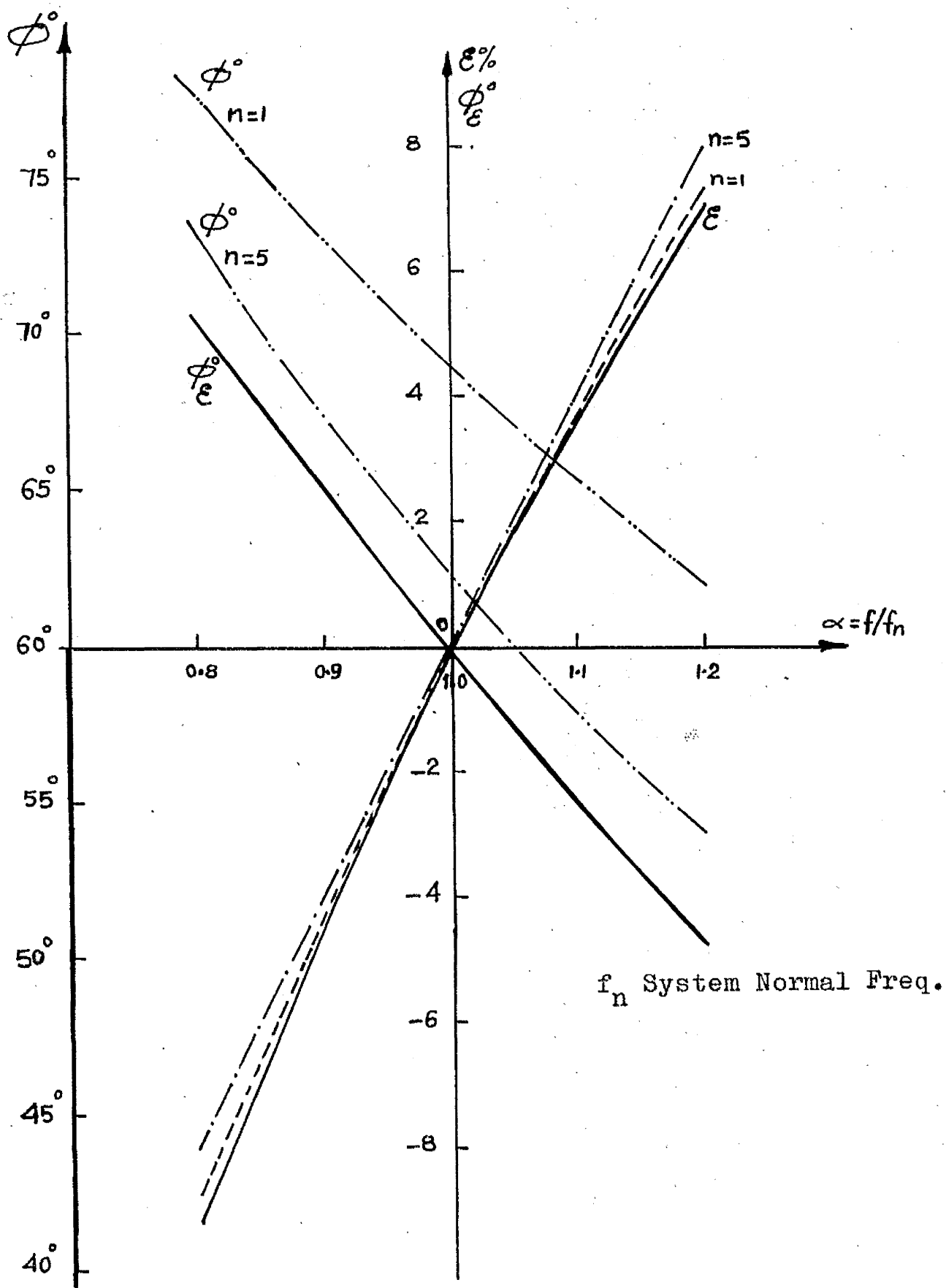
FIG. (6.11)   FREQUENCY DEVIATION ERRORS
(FOR CIRCUITS FIG. 6.9)

behaviour under frequency departure can be analysed, in a similar fashion to that stated before, as follows:—

$$V_{ot}/V_{in} = \frac{n R^2 \omega^2 C_2^2}{n(R^2\omega^2 C_2^2 - 1) - j\omega C_2 R(1 + 2n)} \qquad \ldots \ldots (6.82)$$

If the frequency changes to αf_n then the output V_o'/V_{in}' is given by :—

$$V_{ot}'/V_{in}' = \frac{n R^2 \alpha^2 \omega^2 C_2^2}{n(R^2\alpha^2\omega^2 C_2^2 - 1) - j\omega\alpha C_2 R(1 + 2n)}$$

$$= \frac{3n\,\alpha^2}{n(3\alpha^2 - 1) - j\sqrt{3}\,\alpha(2n + 1)} \qquad \ldots \ldots (6.83)$$

Hence

$$V_{ot}'/V_{in}' = \frac{3\alpha^2 n \quad \angle + \phi^o}{\left[n(3\alpha^2 + 1)^2 + 3\alpha^2(4n + 1) \right]^{1/2}}$$

where

$$\phi = \tan^{-1}\frac{\sqrt{3}\,\alpha(2n + 1)}{n(3\alpha^2 - 1)}$$

$$\ldots \ldots (6.84)$$

Therefore

$$\left| V_{ot}'/V_{in}' \right| = \frac{3\,\alpha^2 n}{\left[n^2(3\alpha^2 + 1)^2 + 3\alpha^2(4n + 1) \right]^{1/2}} \qquad \ldots \ldots (6.85)$$

Fig. (6.11) gives the increment $\mathcal{E}$ due to frequency deviations of $\pm 20\%$, for two cases of $n = 1$ and 5. In this case " $\mathcal{E}$ " increases as "n" increases for both cases of "α" bigger or smaller than unity. For the practical range of frequency departure

between 48 to 52 c/s single stage as well as double stage circuits having n = 1 or 5 , have incremental errors of almost the same order namely less than 2%.

The error in the phase angle ϕ , eqn. (6.84), decreases in a two stage circuit as "n" increases, reaching the limit as a single stage circuit as "n" tends to infinity.

From the previous analysis and from Figs. (6.10 and 11), it is clear, however, that the incremental errors due to frequency departures are substantially less than the deviation in the frequency itself. Such a criterion is accepted for circuits which are not seriously frequency sensitive.

It has been mentioned earlier that the voltage output of a linear coupler is in direct proportion with the frequency of the system. Therefore a phase shifting circuit of the type discussed supplied from a linear coupler, assuming a constant primary current, would show an overall frequency error different from those obtained in Fig. (6.10 and 11). The overall error may be higher or smaller than that of the circuit alone, depending on the sign of the frequency deviation.

Such cases may be better illustrated in the following two examples :-

(a) Taking the case of the composite 2 stage circuit, Fig. (6.7D), for a 60° voltage shift and having n = 5. This circuit gives $\mathscr{E}$ = + 3.6 % at a frequency of 45 c/s. At this frequency

the output voltage of the linear coupler, assuming a constant primary current, would be α times V_n at normal system frequency, i.e. $0.9 \, V_n$.

The overall error $\mathcal{E}_c$ is given by

$$\mathcal{E}_c\% = 100 \left[\alpha(V_n \pm \mathcal{E}/100) - V_n \right] = 100 \left[V_n(\alpha - 1) \pm \frac{\alpha}{100} \right]$$

$$\cdots\cdots \quad (6.86)$$

Hence $\mathcal{E}_c\% = -3.76$ for a frequency deviation of -10%.

(b) On the other hand for circuit, Fig. (6.9C) and for the case of $n = 5$, $\mathcal{E} = -4.2\%$ at 45 c/s. Then the overall error $\mathcal{E}_c\%$ as given by eqn. (6.84) would be

$$\mathcal{E}_c\% = -10.7\% \text{ for } -10\% \text{ frequency deviation.}$$

This last circuit would give an overall error of the same order as the frequency deviation. This effect and the way to overcome it, in the design of the final selected circuit, will be discussed in section (6.3.5).

From eqn. (6.86) it can be seen that the overall error $\mathcal{E}_c\%$ increases or decreases w.r.t. "$\mathcal{E}$", depending on the sign of "$\mathcal{E}$" and on whether the value of "α" is larger or smaller than unity.

6.3.5 The Effect of Loading

In the previous sections no consideration has been given

to the effect of the load on the performance of the phase shifting circuits. It has been assumed that the output terminals "cd" , Figs. (6.7 and 9), are open circuited or, in other words, the loading effect is negligible. This effect can be considered further and may be analysed in the following manner :-

The circuit, Fig. (6.12A), viewed from its output terminals "cd" represent an impedance $Z\phi_L$ when the voltage source V_{in} is equal to zero, i.e. short-circuited. It is also assumed that the internal impedance of the source is zero, or it is included in the circuit behind "ab". Fig. (6.12B) shows, therefore, the equivalent circuit, where V_{ot} is an equivalent source being determined by the no load conditions, i.e. equal to the open circuit voltage V_{ot} between "cd" when $Z_L = \infty$.

The load current I_L and voltage V_L can be determined from,

$$I_L = \frac{V_{ot}}{Z_L + Z\phi_L} \qquad \ldots\ldots (6.87)$$

and

$$V_L = I_L \cdot Z_L = \frac{V_{ot}}{Z\phi_L + Z_L} \cdot Z_L \qquad \ldots\ldots (6.88)$$

The voltage V_L can be expressed by the short-circuit current I_{cd} which flows when the terminals "cd" are short-circuited. Therefore

$$V_{ot} = I_{cd} \cdot Z\phi_L \qquad \ldots\ldots (6.89)$$
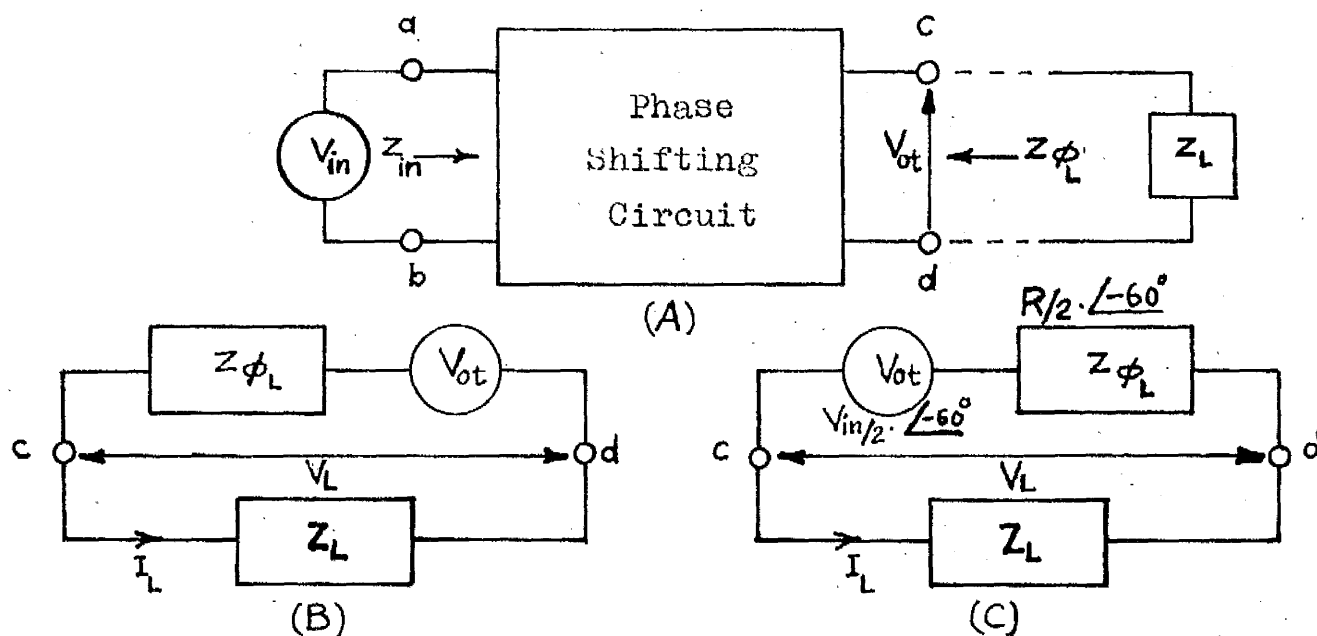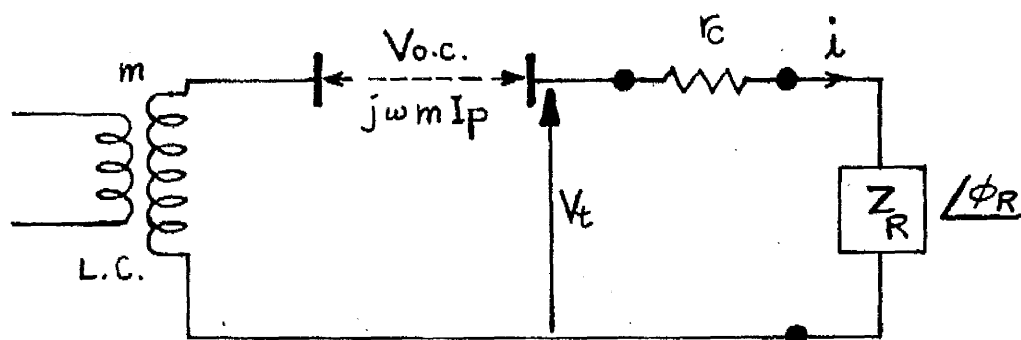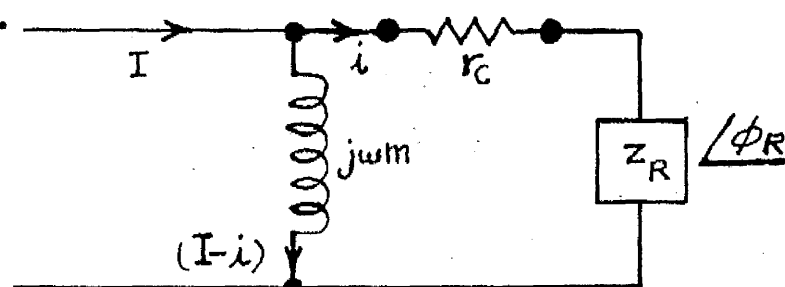
Substituting in eqn. (6.88), it gives:-

FIG. (6.12)   EFFECT OF LOAD ON PHASE SHIFTING CIRCUITS.

L.C. Linear Coupler

m = Mutual inductance
  = secondary induct.

(A) Thevenin's Equivalent

(B) Norton's Equivalent

FIG. (6.13)   EQUIVALENT CIRCUITS OF LINEAR COUPLERS.

$$V_L = I_{cd}/(Y_L + Y_{\phi L}) \qquad\qquad \dots\dots (6.90)$$

where Y_L is the load admittance

$Y_{\phi L}$ is the admittance of the equivalent source V_o.

Consequently the load current is given by :-

$$I_L = \frac{I_{cd}}{1 + (Z_L/Z_{\phi L})} \qquad\qquad \dots\dots (6.91)$$

The method of analysis described above is important from the practical point of view because both the open-circuit voltage V_{ot} as well as the short-circuit current I_{cd} can be measured easily and hence $Z_{\phi L}$ and I_L can be determined from eqns. (6.89 and 91) respectively. This method would eliminate any tedious calculations to determine $Z_{\phi L}$ for complicated circuits already available, thus providing an easier way of studying the effect of the nature of the load on the circuit.

Applying the analysis mentioned above on the circuit of Fig. (6.7A) ,

$$Z_{\phi L} = \frac{R}{1 + j\omega C_1 R} \qquad\qquad \dots\dots (6.92)$$

Since the circuit is designed to give a voltage shift of -60° , then $\omega C_1 R = \sqrt{3}$ and therefore,

$$Z_{\phi L} = \frac{R}{2} \cdot \underline{/-60^\circ} \qquad\qquad \dots\dots (6.92a)$$

The voltage of the equivalent source V_{ot} is given by eqn. (6.69)

as,

$$V_{ot} = \frac{V_{in}}{2} \cdot \underline{/- 60^\circ} \qquad \ldots\ldots (6.93)$$

In evaluating V_{ot} , calculations are simplified by taking V_{in} as reference.

The equivalent circuit is therefore as shown in Fig. (6.12C) and the short-circuit current

$$I_{cd} = V_{in}/R \cdot \underline{/0^\circ} \qquad \ldots\ldots (6.94)$$

The load current I_L as given by eqn. (6.91) is therefore,

$$I_L = \frac{I_{cd}}{1 + (2Z_L/R \underline{/-60})} = \frac{V_{in}}{R(1 + \frac{2Z_L}{R} \underline{/60})} \qquad \ldots\ldots (6.95)$$

The voltage V_L across the load given by eqn. (6.88) will therefore be ,

$$V_L = V_{ot}/(1 + \frac{R \underline{/- 60^\circ}}{2 Z_L}) \qquad \ldots\ldots (6.96)$$

Eqns. (6.95 and 96) give the relationship between the input voltage V_{in} , of the linear coupler, and the load current and voltage, I_L and V_L respectively. Thus the output of the phase shifting circuit could be stated in terms of voltage or current as the case may require.

Linear couplers are considered as voltage sources having an output, on open circuit, proportional to the primary current.

It would, therefore, be preferred to state the output of the segregating circuits associated with linear couplers in terms of output load current than output voltage. A relationship between the primary currents and the segregating network output load current could then be easily established as in section (6.4.2).

It can be shown that if Z_L is resistive, say R_L , and if,

$$R_L \ggg R \quad \text{or} \quad 2R_L/R \gg 1 \qquad \qquad \ldots\ldots \text{(6.97)}$$

then eqns. (6.95 and 96) give :-

$$I_L \simeq \frac{V_{in} \angle{-60^o}}{2\,R_L} = V_{ot}/R_L \quad \text{and} \quad V_L \simeq V_{ot} \ldots\ldots \text{(6.98)}$$

The magnitude and the phase of the output current in the load R_L are the main factors in assessing the behaviour of these phase shifting circuits which form a part of the segregating network, Fig. (6.6). On the other hand there are other factors, e.g. sensitivity to harmonics and frequency errors which also have to be taken into consideration.

For the circuit of Fig. (6.9A), the output voltage V_{ot} is given, taking V_{in} as reference, by eqn. (6.78), namely

$$V_{ot} = V_{in}/1 - j\omega C_1 R$$

For a $+ 60^o$ voltage phase shift $\omega C_1 R = 1/\sqrt{3}$, thus its open-circuit output voltage is ,

$$V_{ot} = \frac{V_{in}}{2} \underline{/\pm 60^{\circ}} \qquad \qquad \cdots \cdots \text{ (6.99)}$$

If a resistive load R_L is connected, as in Fig. (6.12A), between the output terminals "cd" and by following the analysis given in the previous case, it can be shown that :-

$$I_L \simeq \frac{V_{in}\underline{/\!+60^{\circ}}}{2\,R_L} = V_{ot}/R_L$$

$$\cdots \cdots \text{ (6.100)}$$

where $R_L/R \gg 1$

Eqn. (6.100) shows that this current I_L is in phase with V_{ot}, and makes an angle $+60^{\circ}$ w.r.t. the input voltage V_{in}.

Such a phase shifting circuit, Fig. (6.9A) is more vulnerable to harmonics present in the supply source than those of Fig. (6.7). With linear couplers, as voltage sources, the output voltage (V_{ot}) wave shape was severely distorted from being sinusoidal.

It is worth noting in this respect that the output voltage of a linear coupler V_{in}, on open-circuit is $= j\omega m I_p$, and in the case of presence of harmonics in the primary current I_p, the output voltage V_{in} will have a higher harmonic content than I_p. Each harmonic will be multiplied by a factor equal to the order of the harmonic, i.e. 3 for third, 5 for fifth harmonic and so on.

It is reasonable therefore to assume that the presence of these harmonics may be significant only in cases of maximum loads

associated with low fault settings, e.g. an earth fault on
resistive earthed systems accompanied by heavy load currents,
having a large harmonic content. In other fault cases this is
not the case, as fault currents would be almost free from harmonics.
However, it is favourable to choose circuits which are less
sensitive to harmonics than that shown in Fig. (6.9A). A circuit
of the type shown in Fig. (6.7A) offers attenuation to harmonics
present in the input voltage V_{in} , and the output wave shape would
therefore be very much less distorted than the previous case.

Fig. (6.7B) shows a circuit of the same nature as that of
Fig. (6.7A), but designed to introduce a voltage phase shift V_{c_2}
of $- 30^\circ$, see Fig. (6.7C). The output voltage, on open-circuit
V_{c_2} , taking V_{in} as reference, is given by :-

$$V_{c_2} = V_{ot} = V_{in}/(1 + j\omega C_2 R) \qquad \dots\dots \text{ (6.101)}$$

but $\omega C_2 R = 1/\sqrt{3}$, thus

$$V_{ot} = V_{c_2} = \sqrt{3} \cdot \frac{V_{in} \angle{-30^\circ}}{2} \qquad \dots\dots \text{ (6.102)}$$

If a load Z_L is connected to the terminals "cd" in the way
shown in Fig. (6.12A), then the load current I_L , following
the same steps as the previous analysis, given by eqn. (6.91)
will be:-

$$I_L = \frac{V_{in}}{R(1 + \frac{2 Z_L}{\sqrt{3}\, R} \angle{30^\circ})} \qquad \dots\dots \text{ (6.103)}$$

If Z_L is composed of a capacitance C_L , therefore $Z_L = - j/\omega C_L$ and if $|Z_L| \gg R$, i.e. $\dfrac{1}{\omega C_L R} \gg 1$, then the current I_L is given by :-

$$I_L \simeq \frac{\sqrt{3}}{2} V_{in}. \ \omega C_L. \ \underline{/60} \ = \ \frac{|V_{ot}|}{|Z_L|} . \ \underline{/+ 60^o} \qquad \ldots\ldots (6.104)$$

From eqn. (6.104) it can be easily seen that the magnitude of the load current is given by dividing the value of the open-circuit V_{ot} by the magnitude of the load impedance Z_L , and that I_L leads the reference voltage V_{in} by 60°.

Comparing eqn. (6.100) with eqn. (6.104) it can be seen that they give the same result as far as the angle of the load current is concerned and the magnitude of the current is given by $|V_{ot}|/|Z_L|$ in each case. It is also noticed that the value of V_{ot} in the first case is $V_{in}/2$ while in the second case it is $\dfrac{\sqrt{3}}{2} V_{in}$, i.e. the current I_L in the second case is $\sqrt{3}$ times the other if $R_L = |Z_L|$.

As a consequence of this analysis, the second circuit discussed can be used satisfactorily in place of the previous one thus avoiding harmonic sensitivity, particularly with linear couplers as voltage sources. If equal load currents I_L in the two cases are required, for the same input voltage V_{in} , then $|Z_L|$ should be $\sqrt{3} R_L$. This can be seen, at once, by comparing eqns. (6.100 and 104). By doing so and referring to the 3 phase segregating circuit Fig. (6.6), where two types of phase shifting

circuits for $\pm 60^{o}$ shifts are used on phases "B and C", this
ensures equal sensitivity or equal settings on phases "B and C".
The circuit on phase "A" has to produce no phase shift and in order
to obtain a setting equal to the other two phases this circuit has
to be a resistive potential divider giving an output voltage at
point "a", Fig. (6.6), equal to V_{ot} of the phase shifting circuit
on phase "C". As a result of the nature of the design of this
segregating network, Fig. (6.6), the impedance presented to the
linear coupler on each phase, i.e. the burden/phase, is a complex
one having different phase angles.

Nevertheless, equal magnitudes of the burden/phase can be
obtained by the proper scaling of the impedance elements of the phase
shifting circuits.

6.4 Practical Design Considerations

It has been mentioned earlier that the segregating circuits,
fed from linear couplers, are designed to produce an output signal
which will serve as a relaying quantity. The different relaying
quantities adopted in the present scheme and their function are
described in section (4.2). The coefficient M in the relaying
combination $(MI_2 \pm NI_1)$ eqns. (5.1), can be evaluated from the
segregating circuit constants as explained in section (6.3.1).
The ratio of the coefficients $(M/N) = \alpha$, is made variable over
a wide range to meet different choices other than the recommended

---

$\alpha = 6.$

6.4.1 Linear Couplers Output

Linear Couplers have in general low VA output, but, as mentioned earlier, sufficient enough for transistorised schemes of the type described in this work. The linear couplers outputs are applied to segregating networks which in turn produce relaying signals fed to transistorised relays where input signals of the order of a few milliamps are considered quite adequate. It is demonstrated here that linear couplers are suitable for such schemes.

The maximum fault current level in England and Wales for the new 400 K.V. super-grid may reach 60 KA[12], but for most of the other grid and distribution systems a fault level ranging from 20 – 40 KA is quite normal.

The output of the linear couplers incorporated in the developed scheme, or their transfer impedance, is approx. 10 V/KA primary current. Assuming a through fault level of the order of 40 – 50 times full rated current of say 0.5 KA, then the output voltage of the linear couplers, on open circuit, would reach under such fault conditions 200 – 250 Volts. Such high voltage outputs would have very short duration, of the order of few secs., and therefore a much lower value could be adopted as a design value for the continuous rating of the segregating circuit elements.

The linear couplers used, in conjunction with the developed scheme, are constructed from 22 or 20 S.W.G. wire which can stand a steady state current of 0.5A. Under fault conditions, assuming an open-circuit voltage output of 200 V/phase, a maximum output power of 100 VA could be supplied, from the linear couplers. When the linear couplers are operating with load burdens in the secondary circuits, the output power is greatly reduced[21], unless they are operating near open-circuit conditions.

The eqn. governing the relationship between the open-circuit secondary voltage $V_{o.c.}$ of the coupler and the primary current I_p is,

$$V_{o.c.} = j\omega m I_p \qquad \qquad \ldots\ldots (6.105)$$

where "m" is the mutual secondary reactance.
Under any particular load burden condition the coupler output can be written as:-

$$V_t = K \cdot I_p \qquad \qquad \ldots\ldots (6.106)$$

where K is a constant depending on the load and the coupler impedance.

Let the secondary impedance of the coupler be

$$Z_o \underline{/\phi_o} = r_o + j\omega m \qquad \qquad \ldots\ldots (6.107)$$

where r_o is the secondary resistance and it should include the leads, if any.

For the particular couplers used here, Z_O is assumed to be 30Ω, for design purposes, composed of equal resistive and reactive parts each about 21Ω, in fact Z_C was around 22Ω, section (6.2.7).

If "Z_R" is the load impedance, then the coupler secondary current, Fig. (6.13A), is

$$i = \frac{j\omega m I_p}{r + j\omega m + Z_R \underline{/\phi_R}} \qquad \cdots\cdots (6.108)$$

The secondary voltage V_t across the total burden is therefore given by :-

$$V_t = i\, Z_R \underline{/\phi_R} \qquad \cdots\cdots (6.109)$$

Substituting from eqn. (6.108) into eqn. (6.109) gives :-

$$V_t = i\, Z_R \underline{/\phi_R} = \frac{j\omega m I_p}{(1 + \frac{Z_C}{Z_R} \underline{/\phi_O - \phi_R})} \qquad \cdots\cdots (6.110)$$

From eqns. (6.105) and (6.106), eqn. (6.110) can be put in the form :-

$$V_t = V_{o.c.}/(1 + \frac{Z_C}{Z_R} \underline{/\phi_O - \phi_R}) = K.I_p$$

$$\cdots\cdots (6.111)$$

where $\quad K = j\omega m/(1 + \frac{Z_C}{Z_R} \underline{/\phi_O - \phi_R})$

In order to obtain a rather appreciable output from a coupler it should work near open-circuit conditions, i.e. $Z_C/Z_R \lessdot\lessdot 1$. For such a case eqn. (6.111) becomes :-

$$V_t = i \cdot Z_R \cdot \underline{/\phi_R} \qquad V_{o.c.} \qquad \qquad \ldots\ldots (6.112)$$

From eqns. (6.111), it can be shown that :-

$$|V_t| = |V_{o.c.}| / \underline{\big[} 1 + (\frac{Z_c}{Z_R})^2 + 2 \frac{Z_c}{Z_R} \cos \theta \underline{\big]}^{1/2}$$

where $\quad \theta = \phi_c - \phi_R$

$$\ldots\ldots (6.113)$$

Eqns. (6.113) show that due to the fact that the segregating networks present different impedances/phase on the linear couplers, and assuming, as mentioned in the previous section, that the amplitudes of the coupler loads/phase are made equal, then due to the different burden angles ϕ_R an error will be introduced in the settings of the different phases. This may be illustrated in a better manner by evaluating the variation in the factor K of eqns. (6.111), for the different phases.

The particulars of the linear couplers are :-

$$Z_c \simeq 30\Omega \underline{/45^{\circ}} , \quad V_{o.c.} \simeq 10V/KA \quad \text{primary current,}$$

and a design value of Z_R about 450Ω.

There are three different cases for the phase angle of the input impedance of the segregating network namely,

$\phi_{R_A} = 0 \quad$, i.e. $\theta = 45^{\circ}$, for resistive circuit on phase A

$\phi_{R_C} = -30^{\circ}$, i.e. $\theta = 75^{\circ}$, for phase shifting circuit on

phase C

$\phi_{R_B} = -60^o$, i.e. $\Theta = 105^o$, for phase shifting circuit on

phase B.

Evaluating the values of V_t as given in eqn. (6.113),

taking $|Z_{R_A}| = |Z_{R_B}| = |Z_{R_C}| = 450 \, \Omega$, for the different

values of Θ^o given above therefore,

$$|V_t|_A = 0.96 \, V_{o.c.}$$

$$|V_t|_B = 1.018 \, V_{o.c.} \qquad \qquad \dots\dots \, (6.114)$$

$$|V_t|_C = 0.98 \, V_{o.c.}$$

Eqns. (6.114) show that the difference between V_t for

the three phases is quite small, in fact the difference on primary

earth fault settings, taking an average $V_t = 0.99 \, V_{o.c.}$, would

be less than $\pm 3\%$.

6.4.2 Circuit Arrangements for Relaying Combinations

It has been mentioned in the introduction of this chapter

that three relaying quantities are required in the developed

protection scheme namely quantities proportional to the positive

sequence component, the negative, and the zero sequence component

of the fault current. Fig. (6.6) shows a circuit to extract the

negative sequence component of the fault current. The positive

sequence component can also be extracted in a similar manner.

Eqns. (6.1) for the positive sequence can be rewritten as:-

$$V_{a_1} = \frac{1}{3}(V_A - V_B \underline{/-60^\circ} - V_C \underline{/+60^\circ}) \qquad \ldots\ldots (6.115)$$

Fig. (6.14) shows the circuit which represents eqn. (6.115) and in a similar way to that of eqn. (6.54) it can be easily shown that :-

$$i_{L_1} = k_1 . V_{a_1}$$

$$\ldots\ldots (6.116)$$

where k_1 is a constant $= \frac{3C}{R_{L_1}}$

and "C" is the attenuation factor of the phase shifting circuits.

The reversing transformers on the phases "B and C" can be eliminated, by reversing the connection of the couplers to obtain the vector $(- V_B$ and $- V_C)$. This can be done when the couplers supply only this segregating circuit, or couplers with two windings have to be used.

Fig. (6.15) shows the circuit to extract the zero sequence current as given in eqns. (6.1).

It can be easily seen that

$$i_{L_0} = k_0 . V_0$$

$$\ldots\ldots (6.117)$$

where k_0 is a constant $= \frac{3}{R_0}$

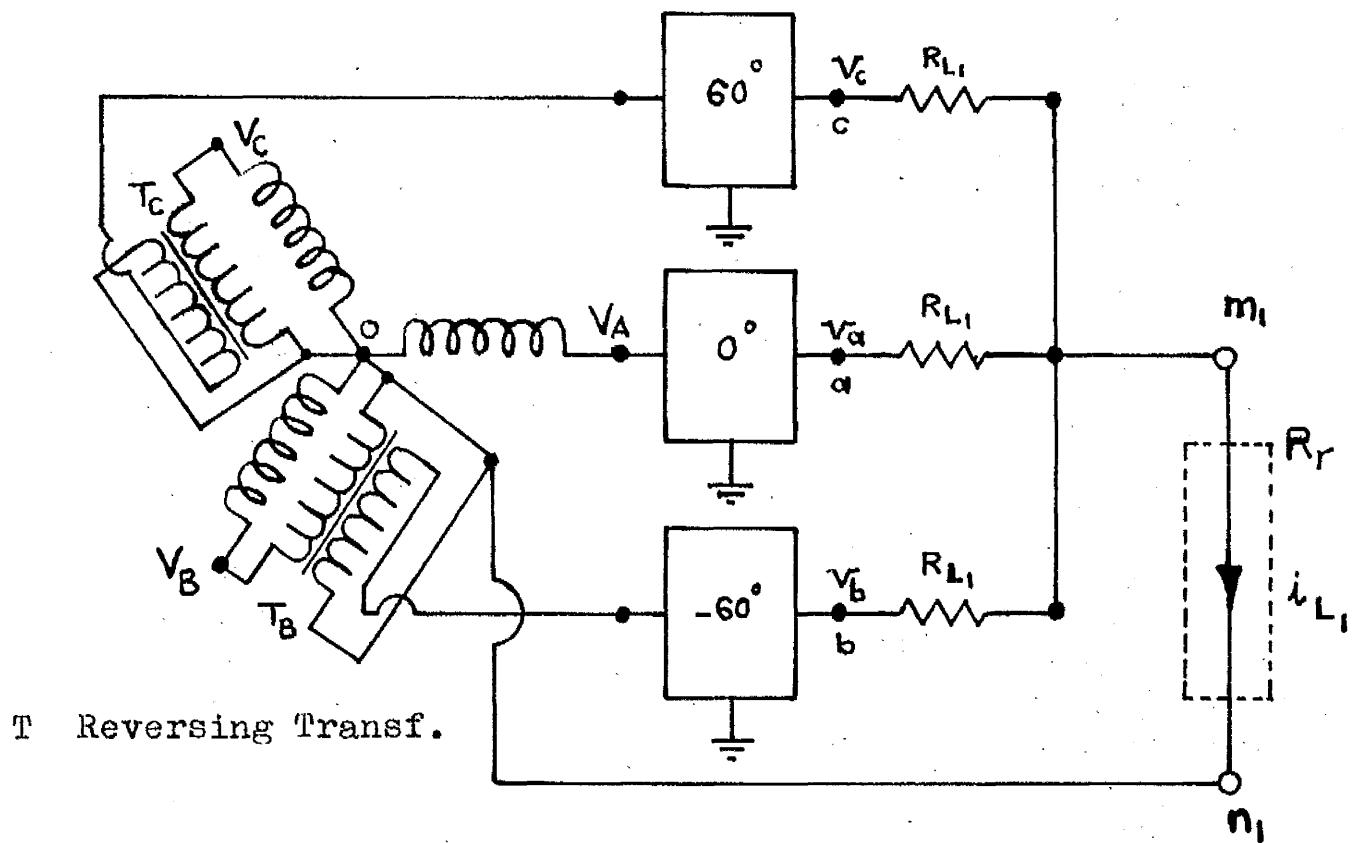For all the 3 segregating networks shown in Figs. (6.6,

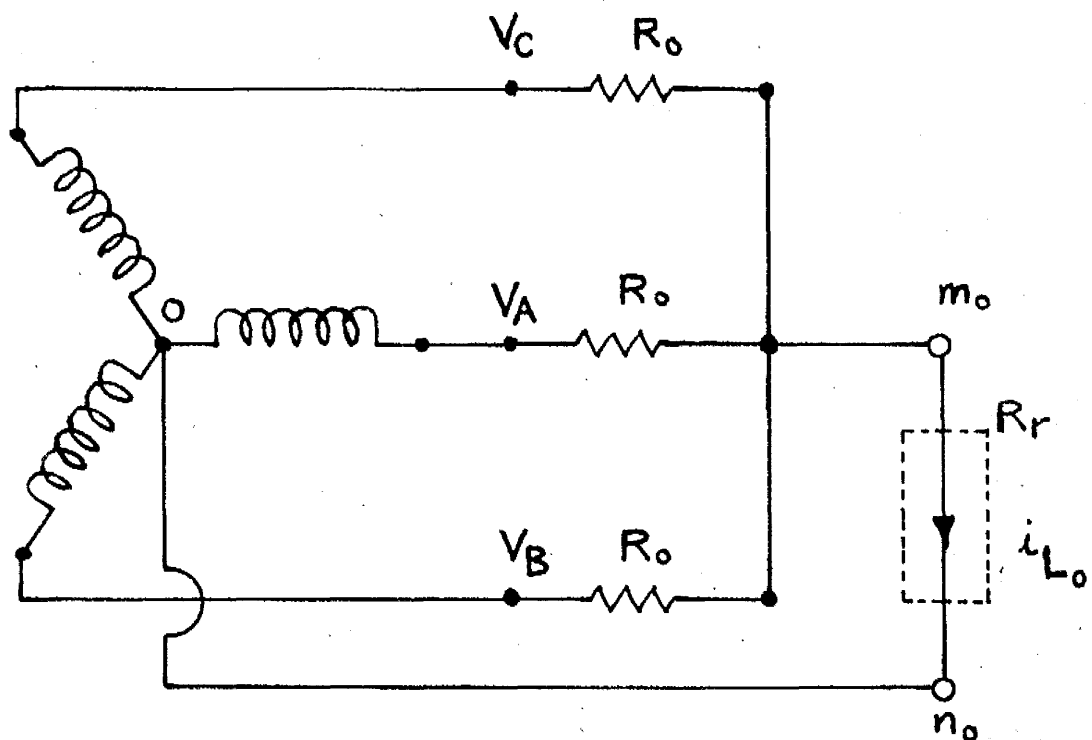FIG. (6.14)   POSITIVE SEQUENCE SEGREGATING CIRCUIT.

FIG. (6.15)   ZERO SEQUENCE EXTRACTING CIRCUIT.

14, and 15) the output currents i_{L_2} , i_{L_1} and i_{L_0} respectively are proportional to the negative, positive and zero sequence component voltages of the coupler secondary output voltage V_A .

According to eqns. (6.45, 105 and 106), it can be seen that i_{L_2} , i_{L_1} , and i_{L_0} are proportional to the sequence components of the primary current "I_p" , of phase "A".

If the sequence component currents of any phase other than "A" is required to be present in the relaying quantity combinations, e.g. as in Chapter (5) eqns. (5.1), this can be achieved by the proper vector rotation of the input voltages either by a or a^2, i.e. simply by interchanging the phases.

In Figs. (6.6, 14 and 15) the three output currents i_{L_2} , i_{L_1} and i_{L_0} are flowing in the relay impedance R_r connected across the terminals "mn" , "$m_1 n_1$", and "$m_0 n_0$" respectively.

The relay input impedance R_r should be very small e.g. compared to R_L or R_0 , i.e. $R_r \ll R_L$. The value of the input current to the relay, for a transistorized amplifying stage, would be only a few milliamps.

In order to obtain a relaying quantity, from the segregating circuits, in the form given by eqns. (5.1), it is therefore necessary to feed both the positive sequence current plus the negative sequence current into the relay. This can be easily achieved by paralleling the output terminals "mn" and "$m_1 n_1$", Figs. (6.6 and 14), across the relay impedance R_r and

therefore the current flowing in the relay I_m would be the sum of i_{L_2} and i_{L_1}. By substitution from eqns. (6.54 and 116) it gives :-

$$I_m = i_{L_2} + i_{L_1} = -(- k_1 V_{a_1} + k_2 V_{a_2}) \quad \ldots \ldots \quad (6.118)$$

Substituting from eqns. (6.105 and 106) in eqns. (6.54 and 116), hence

$$I_m = - j\omega m(- k_1 I_{a_1} + k_2 I_{a_2})$$

$$= - (M I_2 - N I_1) \qquad \ldots \ldots \quad (6.119)$$

where $M = \omega m k_2$ and $N = \omega m k_1$

From Figs. (6.6 and 14) and eqns. (6.54 and 116) it can be seen that $(M/N) = k_2/k_1 = \dfrac{R_{L_1}}{R_L}$, and therefore by changing the ratio of these two resistances different values of $\alpha = (M/N)$ can be obtained. This arrangement of feeding into the relay a current, I_m, having a variable negative/positive sequence component by changing R_L and R_{L_1} may be a little difficult for practical purposes. By changing either of these resistances the settings change, i.e. current in relay for certain I_p, also the change of R_L and R_{L_1} affects the behaviour of the phase shifting circuits as can be seen from eqns. (6.97 and 100), therefore another method of combining the sequence currents in the relaying element has been developed as explained later in section (6.4.4).

However, this arrangement of choosing a certain value for (R_{L_4}/R_L) is very practical for schemes which operate at constant α, e.g. the recommended value of $\alpha = 6$. This fixed value of α can then be taken into consideration from the start in designing the phase shifting circuits.

6.4.3 Calibration and Adjustment

The procedure followed in calibrating these segregating networks is similar to that mentioned in section (6.2.1). This method is simply summarized in applying an accurately balanced 3 phase supply to the segregating network but with an opposite sequence of rotation. e.g. positive sequence voltages to the negative sequence segregating network, Fig. (6.6) and vice-versa for the circuit, Fig. (6.14). Then by trimming the resistive branches, rather than the capacitive ones a zero output current (i_L) can be ideally obtained, and the circuit would therefore act as its nil indicator. In practice a zero output is only obtainable when the supply is purely sinusoidal and generally a very small output composed mainly of harmonics, e.g. mostly 5th harmonic for a negative sequence segregating circuit as it has negative sequence rotation.

Fig. (6.17 A and B) show the output of the negative sequence segregating circuit, for $R_T = \infty$ and $100 \, \Omega$, when a three phase positive sequence supply is applied to it. The voltage

of phase A $(-V_A)$ is also shown in Fig. (6.17A) for comparison.
The harmonic content is enlarged about 25 times to the voltage
scale of phase "A". It is also noticed that this harmonic
output increases with the increase of the supply voltage.

From Fig. (6.17) it can be seen that the harmonic output
is superposed on a small component of 50 cycle fundamental wave.
In fact this was traced to be due to a small error of unbalance
in the applied voltages and the reversing of the voltage of
phase A introduced also another error in the angle between the
phases. Fig. (6.17 A and B) show that the magnitude of this
output due to the harmonics and the errors in the supply does
not exceed 1.5% , when R_r = 100 Ω. However, the fault current
may well be assumed harmonic free and therefore the outputs of
the linear couplers would have a degree of unbalance not more
than that existing between the primary currents.

The positive and negative sequence segregating circuits
were adjusted in the manner mentioned above. The performance
of the zero sequence segregating circuit, Fig. (6.15), depends
on the accuracy of the 3 resistive branches R_0 and therefore
it is preferred to have the tolerance between them as small
as possible. High stabilised resistances with a tolerance of
$\pm$ 0.5% are used to ensure higher accuracies.

The third harmonic in the supply appears in the output of
this circuit, as shown in Fig. (6.17 C and D) for R_r = ∞ ,

(V_A, V_B, V_C)
Linear Couplers

(a) To Starting Circuit (2)
(b) To Starting Circuit (1)
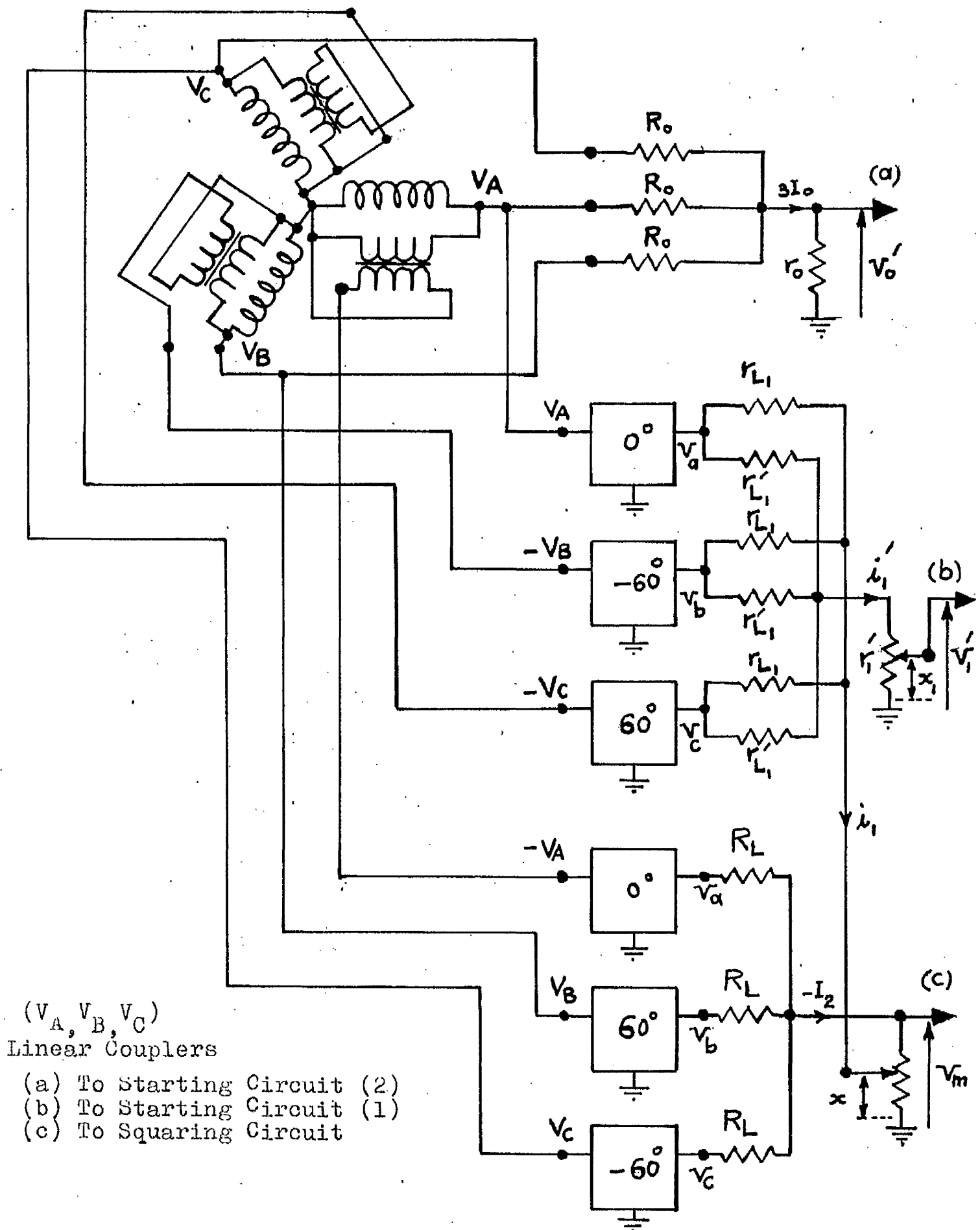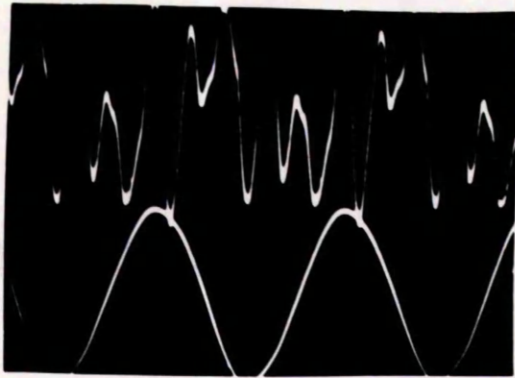(c) To Squaring Circuit

FIG. (6.16)   COMBINED CIRCUIT ARRANGEMENT
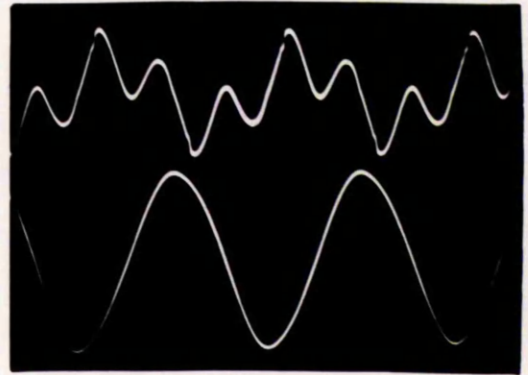FOR RELAYING QUANTITIES.

FIG. (6.17) CALIBRATION OF SEGREGATING NETWORKS

(A) and (B) Negative Sequence Segregating
Circuit Output
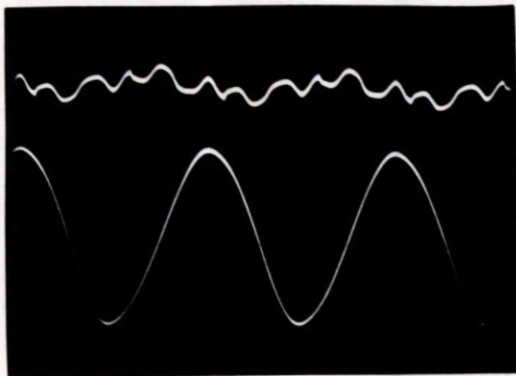at $R_r = \infty$, 100 Ω , respectively.

(C) and (D) Zero-Sequence Segregating
Circuit Output
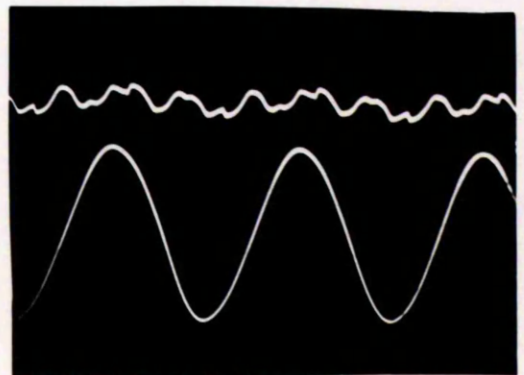at $R_r = \infty$, 50 Ω , respectively.

A

C

B

D

FIG. 6.17.

50 Ω respectively. The harmonic scale is 25 times as large as that of the phase voltage shown in the oscillograms.

6.4.4 Combined Circuit

The final segregating circuit arrangement for the relaying scheme is shown in Fig. (6.16). Three output quantities are derived from the circuit and supplied as relaying quantities.

(a) A quantity in the form $(MI_2 - NI_1)$ is used as an input to the squaring circuit, sec. (8.2), representing the phase angle of the fault current.

(b) Two starting signals proportional to the positive and zero sequence component of the fault current, fed as inputs to starting circuits (1) and (2), section (8.3).

Each of the two fault detecting circuits, fed by a signal from the circuit Fig. (6.16), has a transistorised amplifying input stage of the common emitter configuration. Such a circuit is characterised by a high input impedance in the order of Kilo ohms. Another factor contributing to the increase of this impedance was the practice of inserting the resistance R_2 in the emitter circuit, Fig. (8.3).

The voltage inputs to the starting circuits. i.e. the starting signals are given, as shown in Fig. (6.16) by

$$v_0' = 3I_{oro} \quad \text{and} \quad v_1' = i_1' \cdot x_1 \cdot r_1' \qquad \ldots \ldots \ (6.120)$$

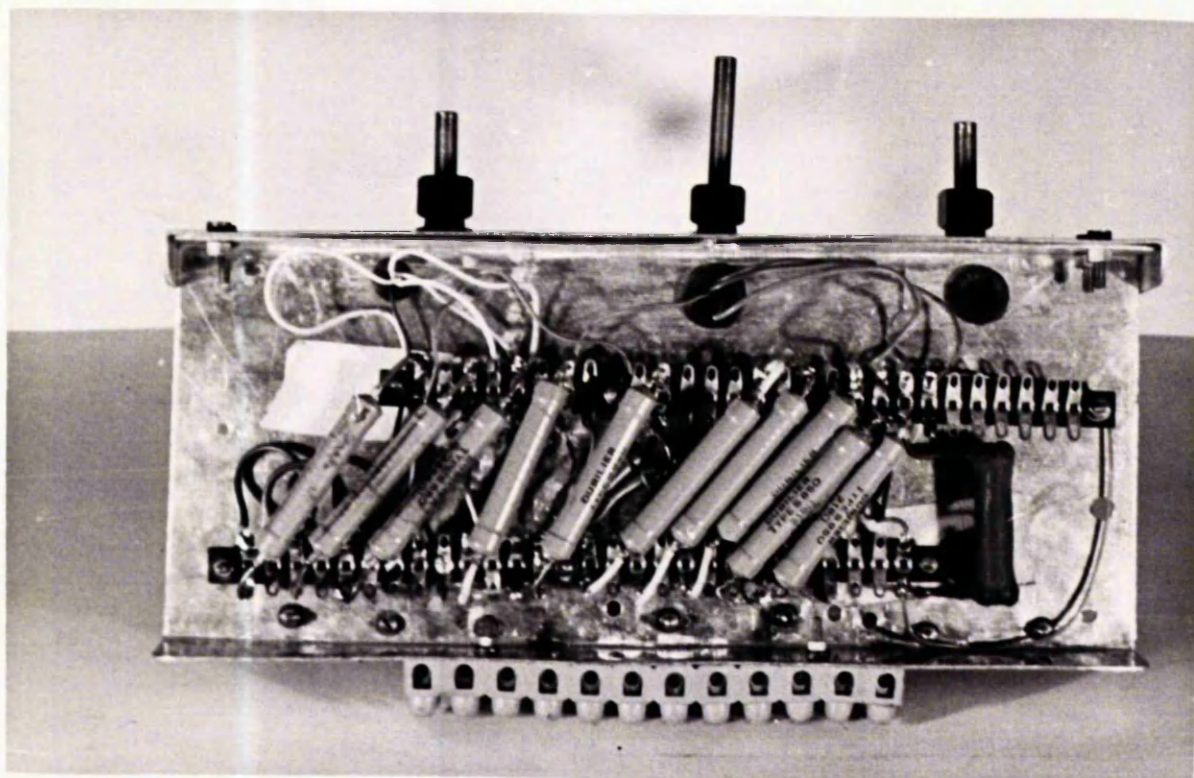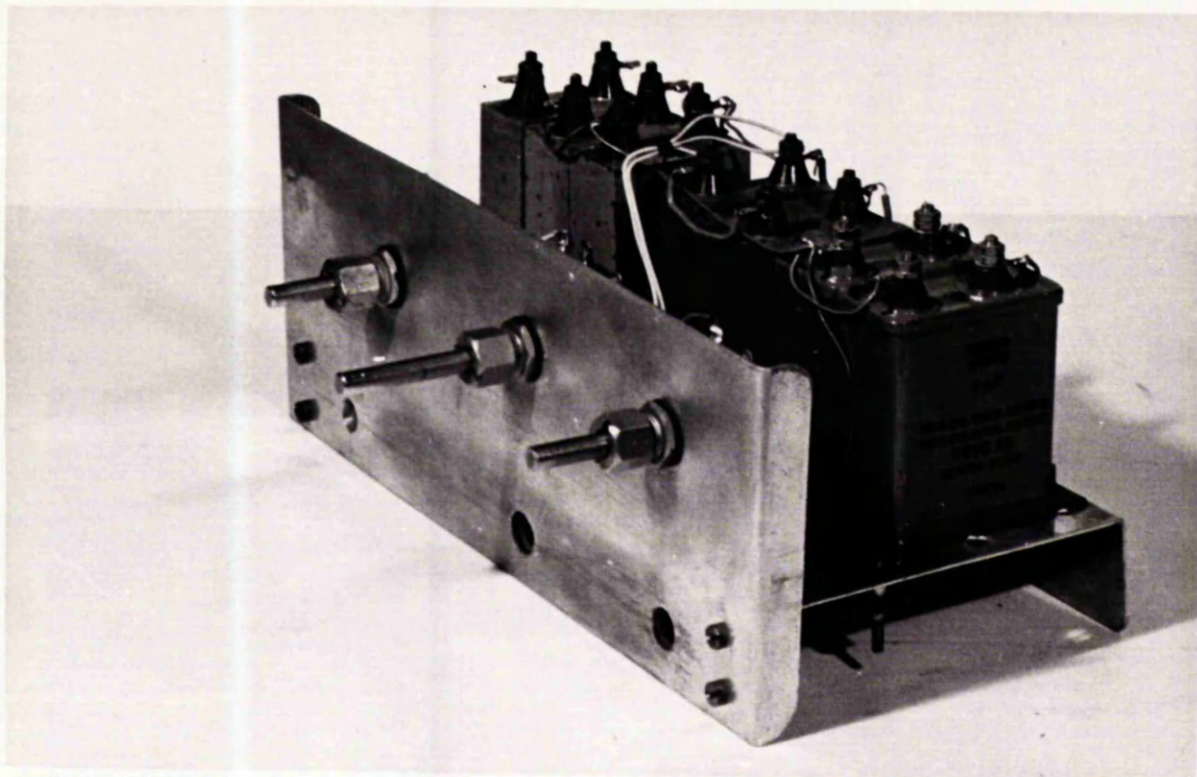where x_1 is the setting of the divider r_1'. The value

FIG. 6.18.

of r_0 is fixed theoretically by the criterion that the appearance of any zero-sequence indicates a fault. In practice, a minimum pick-up level is always considered to avoid initiation of starting signals due to small load unbalance, or capacitive currents of feeders, which have a zero-sequence nature and third harmonic content, if any, under heavy loading conditions. In the relaying scheme, however, even the initiation of the starting circuit would not cause maloperation under healthy feeder conditions as the currents at the two ends are almost 180° out of phase, section (8.4).

The input signal v_m shown in Fig. (6.16) to the squaring circuit of Fig. (8.1), can be seen to be in the form $(MI_2 - NI_1)$. The ratio $\alpha = (M/N)$ can be varied by the setting x of the divider r_2 in addition to the design factor of R_{L_1}/R_L , as explained earlier, section (6.4.2), where R_{L_1} is the parallel combination of r_{L_1} and r_{L_1}' , Fig. (6.16).

Fig. (6.18) shows the front and the back views of the negative sequence segregating network.

CHAPTER 7

CHARACTERISTICS AND SIMULATION

OF PILOT-WIRE CIRCUITS

7.1 Introduction

The previous chapters have dealt with power system characteristics and their associated problems as far as relaying quantities and their derivation are concerned.

The aspect of pilot circuits must also be considered in order to arrive at a satisfactory design for any pilot-wire scheme. Subsequently, it is therefore necessary to study the characteristics of pilot circuits and to construct artificial circuits to simulate practical pilot circuits conditions. The provision of such circuits facilitates the study of the performance of protective schemes and leads to some more design details.

Pilot circuits fall broadly into two categories, privately owned and rented.

The privately owned circuits are in general more reliable than rented circuits, since they are less exposed to outside interference. They are usually shorter than rented circuits, since it is uneconomical to run private pilot circuits over long distances.

Pilot wire feeder protection schemes for lines, between 30 - 40 miles, are more attractive economically than carrier

current or distance protection schemes. This has led to the development of protective schemes suitable for use with G.P.O. rented circuits and, as mentioned in Chapter (1), their use introduced special problems.

In general, the most complicated and cumbersome type of pilot circuits used for protection purposes are those rented from G.P.O. A protective scheme which provides successful performance over a long rented G.P.O. circuit will, in principle, be satisfactory over private pilot circuit and perhaps with considerable simplification.

7.2 Some Problems Associated with G.P.O. Pilot Circuits

As mentioned earlier, the use of G.P.O. rented circuits introduces some problems and imposes limitations on associated protective schemes.

The G.P.O. stipulates that the peak core to core pilot voltage shall not exceed, under maximum fault current, 100 V peak. In some cases special dispensation has been granted and the highest figure so far approved is 135 V peak. These are, however, short time rating values applicable to fault conditions. The permissible continuous voltage levels are much less than these. All equipment connected to the G.P.O. pilot circuits shall have an insulation barrier of 15 kV (for 132 kV systems) between the pilots and all equipment associated with the power system, including the

station or substation earth. This is usually achieved by the use of isolating transformers.

Another consequence to the use of rented circuits for protection purposes is that the equipment shall not be capable of being operated by "G.P.O. Personnel" when testing circuits for fault location. Although the G.P.O. agree to take special precautions with rented circuits as far as possible, they reserve the right to have access and interfere with the pilot circuits at any time during testing or fault locating. During this procedure they may apply test signals of d.c., 17 c/s or audio frequency, to the pilots. Any pilot wire scheme must, in consequence, be incapable of being operated from the pilot circuit side. This is achieved by incorporating current operated fault detectors or starting elements.

Due to the possibility of human interference it is therefore required that the G.P.O. pilot circuits shall be supervised continuously and all modern pilot-wire schemes include a d.c. pilot supervision equipment to detect pilot open circuit, short circuit and cross over. At each end polarised relays detect these conditions and give a time delayed alarm, as given in section (1.2.1). The d.c. for supervision must not, under any conditions, be capable of operating the protective relays. It is desirable that the supervision current flow shall be interrupted as soon as a fault condition is detected by the fault detectors so

that the protection scheme cannot be mislead by combined a.c.
and d.c. signals.

The most important practical feature of G.P.O. circuits is
that they comprise different conductor sizes connected in series
with, and in most cases, without matching arrangements between
the different sections. A practical circuit is, in fact, a
complex (RCL) four terminal network. The resistance and capacitance
are the normal properties and the inductance being mainly due to
loading coils added to trunk circuits in order to facilitate speech
transmission.

A typical pilot circuit will comprise loaded and unloaded
sections and may well contain different conductor sizes on each
side. This practice results in completely unsymmetrical pilot
circuits, i.e. the open and short circuit impedances at both
ends are different, although for a linear circuit, the ratios of
the two impedances will be the same at the two ends.

7.2.1 Loading of G.P.O. Circuits

Inductances are added to cable pilot circuits mainly to
eliminate transmission distortion at audio frequencies. Three
different loading methods are practiced.

(a) By means of inductance coils inserted in series at regular
intervals along the line.

(b) By the provision of one or more layers of iron, or some sort

of an iron alloy, wire wound on each core of the pilot circuit.
This method is known as continuous or uniform loading.

(c) By "patch" loading which is an arrangement whereby the pilot
cores are continuously loaded for 200 yards, unloaded for the next
200 yards and so on, throughout the length of the cable.

However, the presence of inductance (loading) on G.P.O. circuits
adds another hazard to the protective gear designer where the pilot
circuit is considered a pure resistive/capacitive circuit.

7.3 Derivation of Equivalent Circuits for G.P.O. Pilots

From the previous section it is seen that G.P.O. pilot circuits
are by no means symmetrical, i.e. a considerable degree of
unbalance is usually present between the pilot circuit as viewed
from its two ends. This may be attributed to, one or more, of the
following causes:-

(a) the use of a number of different conductor sizes to form one
circuit,

(b) the use of different loading coils spacings and sizes, over
the pilot route,

(c) The use of paralleled cores on some sections of the pilot
circuit.

It is clear that the amount of unbalance depends on the
pilot-circuit constants and whether this is tolerable or not

depends on the particular scheme of protection concerned.

With an unbalanced pilot circuit the compensating (replica) impedances etc., in a differential scheme, will require different settings at the two ends and therefore in order to determine the suitability of any pilot circuit for its intended application it is desirable to measure the degree of unbalance present. The method usually adapted is the calculation of π-equivalent circuit of the line from the measurements of open-circuit and short circuit impedances.

7.3.1. Measurements on G.P.O. Pilot Circuits

In order to obtain the pilot circuit constants and hence to find the π-equivalent of a certain line it is necessary to determine first the open-circuit and short-circuit impedances, measured from each end. These impedances are usually measured by an A.C. bridge method. The π-equivalent circuit obtained from these measurements would be the equivalent at the frequency of the bridge supply, which should be truly sinusoidal to avoid any errors due to harmonics.

The four impedances of the pilot circuit to be determined are:-

$Z_{o.c.}(1)$ = input impedance measured at end (1) with end
(2) open-circuited

$Z_{o.c.}(2)$ = input impedance measured at end (2) with end (1) open-circuited

$Z_{s.c.}(1)$ = input impedance measured at end (1) with end (2) short-circuited

$Z_{s.c.}(2)$ = input impedance measured at end (2) with end (1) short-circuited.

Some indication of the accuracy of the results can be obtained by checking that the ratios $Z_{o.c.}(1)/Z_{s.c.}(1)$ and $Z_{s.c.}(1)/Z_{s.c.}(2)$ are identical, provided the measurements are correct and no non-linear components are present in the line circuit.

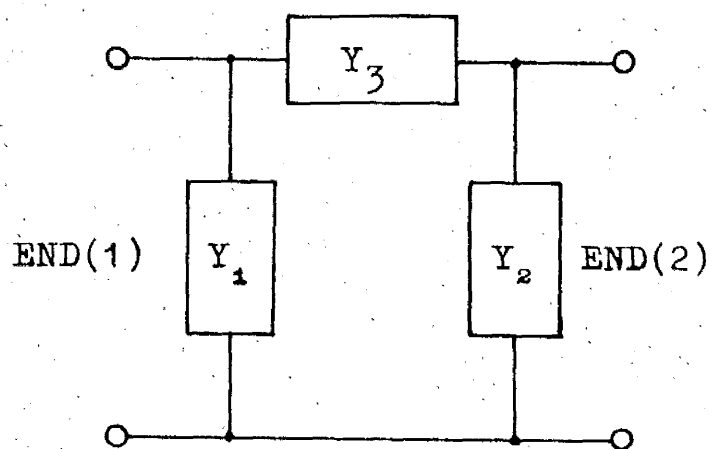The π-equivalent circuit of the line is obtained from the following equations:-

$$Y_3 = \left[Y_{s.c.\ 2} \left\{ Y_{s.c.}(1) - Y_{o.c.}(1) \right\} \right]^{1/2} \text{mhos}$$

..... (7.1)

$$Y_1 = Y_{s.c.}(1) - Y_3 \qquad \text{mhos} \qquad \qquad ..... (7.2)$$

and $Y_2 = Y_{s.c.}(2) - Y_3 \qquad \text{mhos} \qquad \qquad ..... (7.3)$

where Y_3 = the admittance of the series arm of the π-equivalent circuit

Y_1 and Y_2 are the admittances of the shunt arms of the π-equivalent at end (1) and (2) respectively as shown in Fig. (7.1)
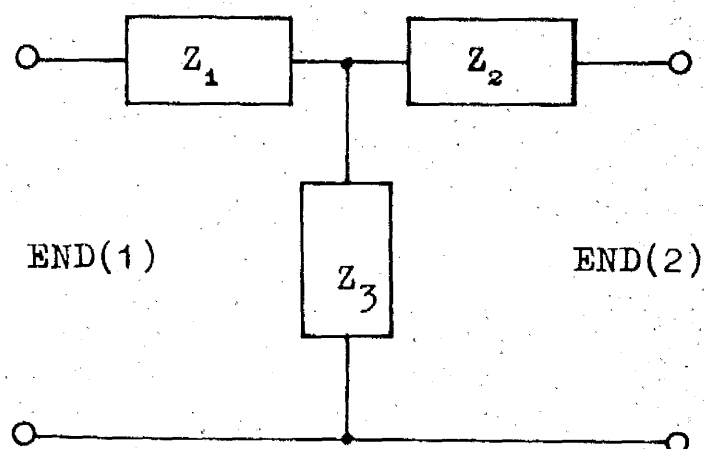
(A) π - Equivalent

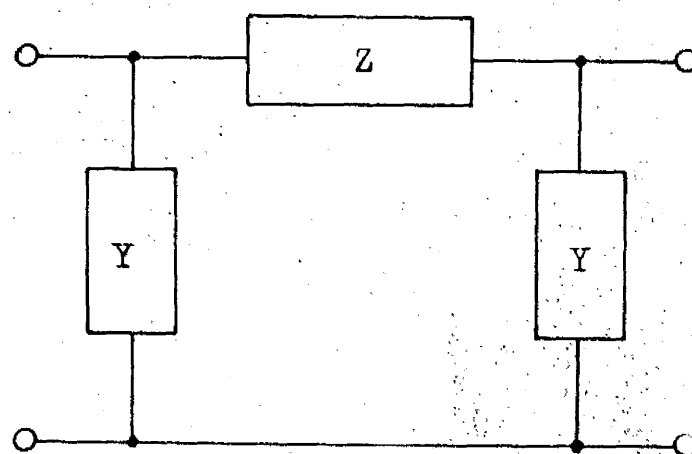$Y_3 = 1/B$

$Y_2 = \dfrac{D-1}{B}$

$Y_1 = \dfrac{A-1}{B}$

(B) T - Equivalent

$Z_3 = 1/C$

$Z_2 = \dfrac{D-1}{C}$

$Z_1 = \dfrac{A-1}{C}$

(C) π - Equivalent of a Symmetrical Long Pilot.

FIG. (7.1) π and T EQUIVALENTS FOR PILOT CIRCUITS.

The relation between the π-equivalent, or its dual the T-equivalent, circuit and the constants A, B, C and D of the complex four terminal network is given in Appendix (i).

It is clear that this π-equivalent circuit represents the pilot-circuit only at the frequency at which the measurements were carried-out. For short lines the π-equivalent components approximate to the values expected from the known line constants, but for longer lines this state of affairs is no longer true. For long lines, e.g. 30 miles and over, the series arm admittance would represent an effective admittance, a fictitious one, which differs considerably from that calculated from the line constants. These equivalent impedances are such that π-equivalent circuit characteristics are identical to those of the line, at the frequency concerned, regarding attenuation and phase shift.

7.3.2 Determination of the π-Equivalent Circuit from the Line Constants

As mentioned earlier most G.P.O. circuits are composed of several section of different conductor core sizes both loaded and unloaded, but where the core size and loading conditions are constant throughout, the π-equivalent circuit can be calculated from the line constants.

Thus, let R' = loop resistance ohms/mile

L' = inductance in H/mile

C' = shunt capacitance in F/mile

G' = shunt conductance in mhos/mile.

The characteristic impedance of the line is given by:-

$$Z_0 = \left[(R' + j\omega L')/(G' + j\omega C') \right]^{1/2} \text{ohms} \quad \ldots\ldots \text{(7.4)}$$

and the propagation constant " " is given by:-

$$\gamma = \left[(R' + j\omega L')/(G' + j\omega C') \right]^{1/2} = \alpha + j\beta \quad \ldots\ldots \text{(7.5)}$$

If Z represents the series arm impedance of the π-equivalent circuit, Y is the admittance of the two shunt arms Fig. (7.1C), and the length of the line is ℓ miles. Then it can be shown that:-

$$Z = Z_0 \sinh (\gamma \ell)$$

or $\quad Z = Z_0 \left[\sinh \alpha \ell \cdot \cos \beta \ell + j \cosh \alpha \ell \cdot \sin \beta \ell \right] \text{ ohms}$

$$\ldots\ldots \text{(7.6)}$$

and $\quad Y = \dfrac{\left[\sinh \alpha \ell - j \sin \beta \ell \right]}{Z_0 \left[\cosh \alpha \ell + \cos \beta \ell \right]} \text{ mhos} \quad \ldots\ldots \text{(7.7)}$

Applying this to a practical G.P.O. circuit of 20 lb/mile conductor for the following cases:-

(a) Unloaded 20 lb/mile conductor.

The theoretical 50 c/s π-equivalent circuit components are given in Fig. (7.2) for a length up to 30 miles. The line

FIG. 7.2. THEORETICAL "π" DIAGRAM COMPONENT COMPONENT VALUES AT 50 C/S. FOR 20 LB/MILE UNLOADED POST OFFICE LINE.
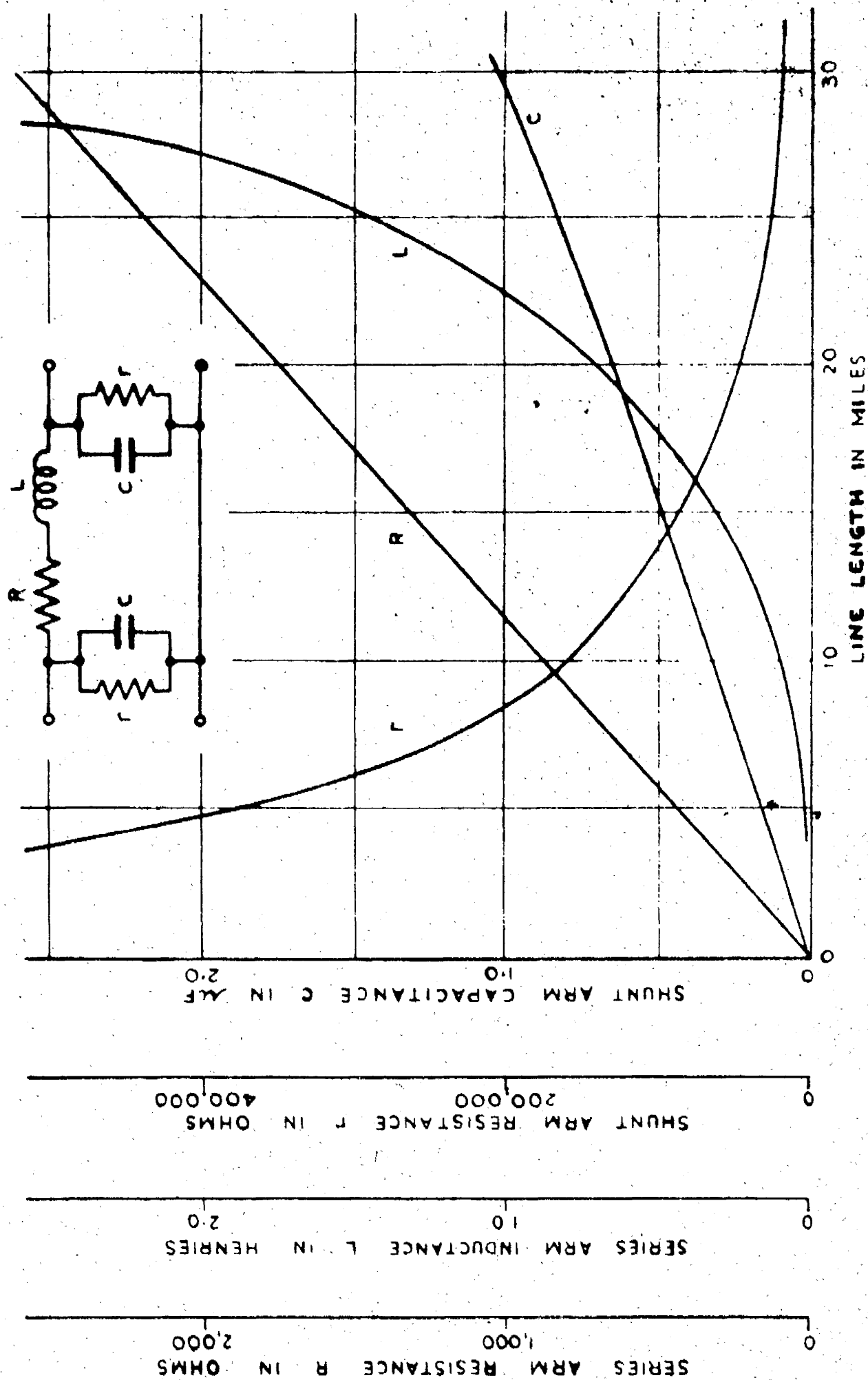
constants, on which these components are evaluated, are as follows:-

$$R' = 88 \text{ ohms/mile}, \quad L' = 0.001 \text{ H/mile}$$
$$C' = 0.065 \text{ μF/mile}, \quad G' = 10^{-6} \text{ mho/mile}$$

(b) Loaded 20 lb/mile Conductor.

The line is assumed to be loaded with 88 mH per 2000 yards and the circuit constants, including the loading coils, are:-

$$R' = 92 \text{ ohms/mile}, \quad L' = 0.0785 \text{ H/mile}$$
$$C' = 0.065 \text{ μF/mile}, \quad G' = 10^{-6} \text{ mho/mile}.$$

Fig. (7.3) gives the components of the π-equivalent circuit for line length up to 30 miles.

7.3.3 T-Equivalent Circuit

Referring to Fig. (7.1b), it is sometimes more convenient to represent the line in its T-equivalent circuit. The values of components can be evaluated from the line input impedances $Z_{o.c.}(1)$, $Z_{o.c.}(2)$ and $Z_{s.c.}(1)$, $Z_{s.c.}(2)$ as follows:-

$$Z_3 = \left[Z_{o.c.}(2) \left\{ Z_{o.c.}(1) - Z_{s.c.}(1) \right\} \right]^{1/2} \quad \ldots\ldots \quad (7.8)$$

$$Z_1 = Z_{o.c.}(1) - Z_3 \quad \ldots\ldots \quad (7.9)$$

and $Z_2 = Z_{o.c.}(2) - Z_3$ $\quad \ldots\ldots \quad (7.10)$

FIG. 7.3. THEORETICAL π DIAGRAM COMPONENT VALUES FOR 20 LB/MILE G.P.O. LINE LOADED 88 mH PER 2000 YDS.
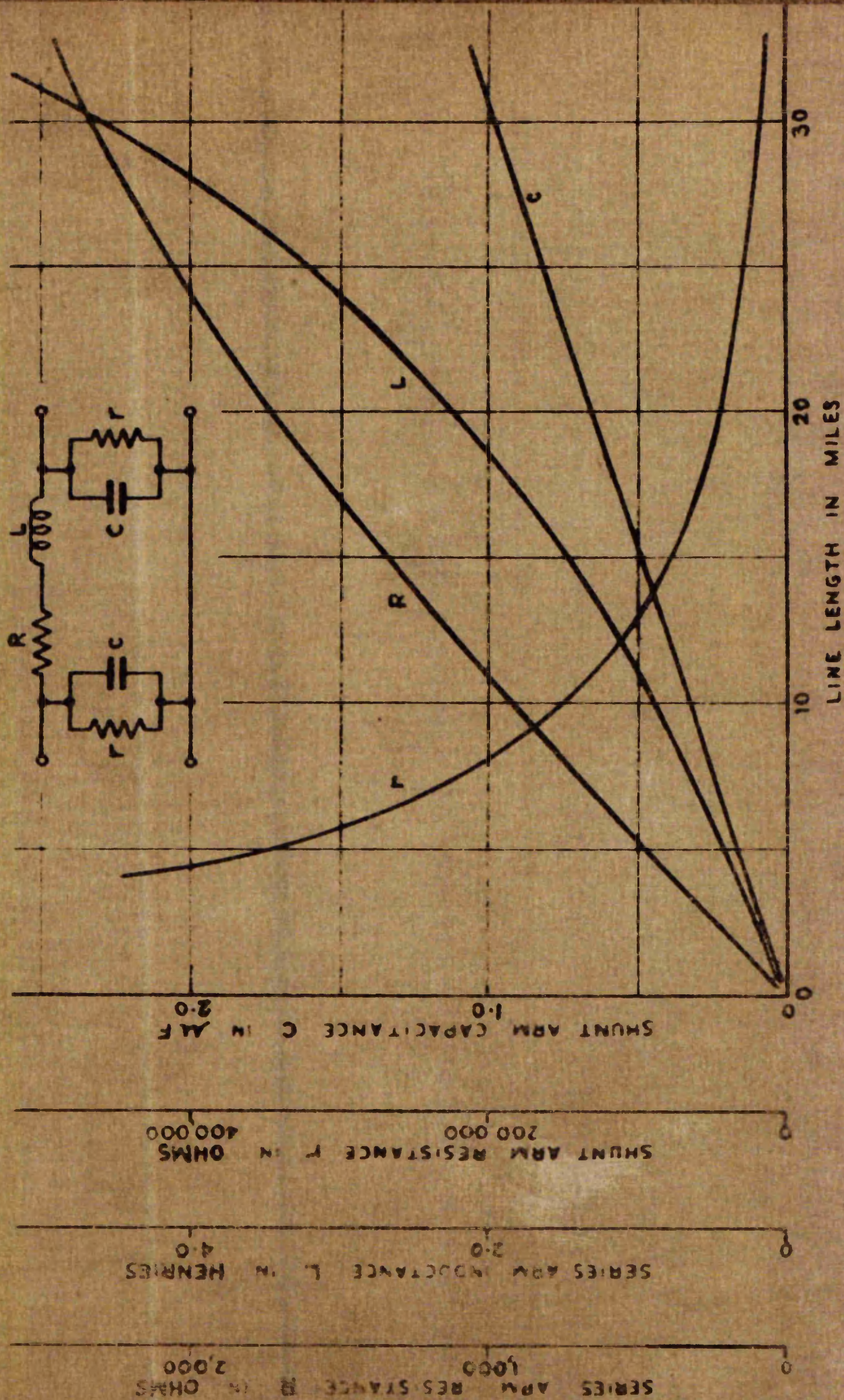
7.4 Infinite Line Approach for G.P.O. Relaying Circuits

The use of G.P.O. circuits for pilot-wire protection schemes has been treated, in some applications[23][24], on the basis of the classical infinite line theory. This philosophy presupposes that the pilot circuit may be represented by its characteristic impedance. It also implies the use of impedance matching devices and in one application[24] of equal terminating end to end symmetry.

Matching between different lines, can be affected by the use of the image impedance concept. The image impedances, by definition[25], of a network are those impedances such that when one of them is connected across the appropriate pair of terminals of the network; the other is presented by the other pair.

In case of asymmetrical network the two image impedances are different. This can be better seen from Fig. (7.4A), where the input impedance at terminals ab of the network is $Z_0(1)$ when terminals cd are terminating in $Z_0(2)$, and the input impedance at terminals cd is $Z_0(2)$ when terminals ab are terminating in $Z_0(1)$. When the two image impedances are equal, as in the case of symmetrical networks, their common value is equal to the characteristic impedance Z_0 of the network. An asymmetrical network is said to be properly terminated when it is terminated in its image impedances.
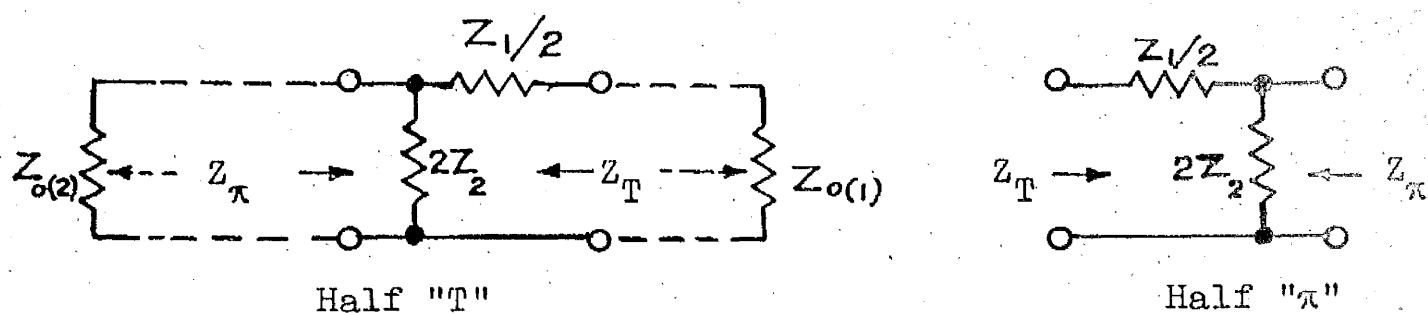
Advantage can be taken from the properties of half-sections to be interposed between the lines whose characteristic impedances
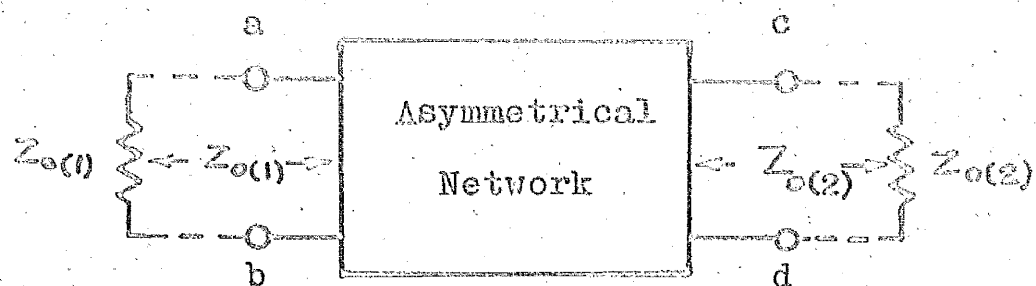
(A) Image Impedances

(B) Full "T and π" Sections

Half "T"

Half "π"
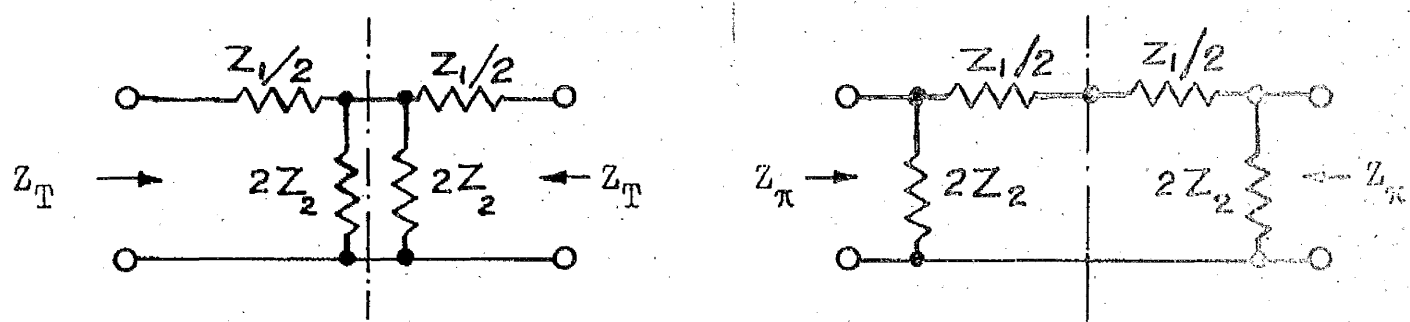
(C) Half "T and π" Sections

FIG. (7.4) IMAGE IMPEDANCES.

conform the image impedances of the half-section.

Referring to Fig. (7.4B and C), it can be proved that, for the full sections:-

$$Z_T = \left[Z_1 Z_2 + \frac{Z_1^2}{4} \right]^{1/2} \qquad \dots\dots (7.11)$$

$$Z_\pi = Z_2 Z_1 / \left[Z_1 Z_2 + \frac{Z_1^2}{4} \right]^{1/2} = Z_2 Z_1 / Z_T \qquad \dots\dots (7.12)$$

The image transfer constant "Θ", which corresponds to the propagation constant in symmetrical circuits, is

$$\cosh \Theta = 1 + Z_1 / 2Z_2 \quad \text{and} \quad \sinh \Theta/2 = \left[Z_1 / 4Z_2 \right]^{1/2}$$

$$\dots\dots (7.13)$$

The half sections, Fig. (7.4C), have an image transfer constant exactly $1/2$ of that of a full section.

The image impedances of the two sides of the half sections differ, being Z_T on one side and Z_π on the other side.

If the two pilot circuit lines to be connected together have characteristic impedances $Z_0(1)$ and $Z_0(2)$ respectively, then the components of a properly terminating (or matching) half-section may then be determined.

Referring to Fig. (7.4C), then the condition for matching is,

$$\therefore \quad Z_0(1) = Z_T \quad \text{and} \quad Z_0(2) = Z_\pi \qquad \dots\dots (7.14)$$

Substituting from eqns. (7.11 and 12) in eqn. (7.14) it gives,

$$Z_T \cdot Z_\pi = Z_0(1) \cdot Z_0(2) = Z_1 Z_2 \qquad \ldots \ldots (7.15)$$

From eqns. (7.11, 12 and 15) it can be proved that :—

$$Z_1/2 = \left[Z_0(1) \left\{ Z_0(1) - Z_0(2) \right\} \right]^{1/2} \qquad \ldots \ldots (7.16)$$

and $2 Z_2 = Z_0(1) \cdot Z_0(2) / \left[Z_0(2) \left\{ Z_0(1) - Z_0(2) \right\} \right]^{1/2}$

$$\ldots \ldots (7.17)$$

Eqns. (7.16 and 17) give the components of the matching impedance half-section. The insertion of such matching networks is always associated with power loss and this may be made a minimum by incorporating a transformer to make the moduli of the two characteristic impedances of the two lines equal.

Two half-sections are also required, for proper termination, one at each end of the line.

For the case of unloaded G.P.O. circuit, the effective parameters are the resistance and capacitance and therefore the characteristic impedance, as given by eqn. (7.4), would be

$$Z_0 \simeq \left[\frac{R'}{j\omega C'} \right]^{1/2} = \left[\frac{R'}{2\omega C'} \right]^{1/2} (1 - j) \qquad \ldots \ldots (7.18)$$

Eqn. (7.18) shows that the characteristic impedance of an unloaded line has an angle of $- 45^o$. In cases where the moduli are made equal then,

$$Z_0(2) = R_e (1 - j) \qquad \text{and} \qquad Z_0(1) = \sqrt{2} \, R_e \quad ,$$

where R_e is an equivalent resistance equal to $\left[R'/2\omega C' \right]^{1/2}$.

In cases of loaded lines an expression can be obtained for the characteristic impedance of the line, in the form of a series resistance/capacitive combination. If the conductance G' can be neglected in eqn. (7.4) then the characteristic impedance Z_0 is given by

$$Z_0 \simeq \left[(R' + j\omega L')/j\omega C' \right]^{1/2} = \left(L/C - j \, R/\omega C \right)^{1/2}$$

$$= (R_0 + j X_0) \qquad\qquad \ldots\ldots (7.19)$$

where $R_0^2 - X_0^2 = L'/C'$ and $2 R_0 X_0 = - R'/\omega C'$

By expressing the characteristic impedance in the above form proper terminating sections can be determined by eqns. (7.16 and 17).

7.4.1 Practical Limitations of the Infinite Line Approach

The G.P.O. accept no obligations when renting circuits for protection purposes. In fact they impose conditions on the users. No special provisions are made other than providing an efficient speech circuit. Special arrangements or facilities may not be easy to obtain or may be obtainable at high cost.

It is not the practice of the G.P.O. to provide impedance matching at different points of connection in mid route. Some sort of impedance matching may be provided at the line terminating points. Furthermore, the normal standard impedance matching devices may introduce undesirable non-linear features at power-

levels, similar to those encountered for protection purposes.

It is now clear that it is the task of the protective scheme designer to produce a relaying scheme which can operate satisfactorily on practical G.P.O. circuits without demanding any special equipment to be fitted by the G.P.O. personnel. However, the practice of terminating the pilot circuit is quite acceptable.

7.5 Simulation of Pilot Circuits

Pilot circuits are effectively composed of distributed capacitance and resistance, when the shunt conductance can be regarded as negligible. Loaded pilot circuits have, of course, a much greater inductance than unloaded circuits. The pilot circuit has, therefore, to be considered, from the protection point of view, as a transmission line with distributed parameters rather than of lumped ones.

Simulation of pilot circuits must be composed of a large number of sections in order that an accurate assessment of the protective scheme behaviour may be obtained. The π or T-equivalent networks give a fairly true representation, at a single frequency only, of the pilot-circuit and therefore may be useful in the initial design stages of the protective scheme. However, testing of pilot-wire schemes should reproduce practical pilot-circuit conditions, as far as possible.

Practical pilot-circuits are, in general, unsymmetrical at

the two ends and simulation of pilot-circuits should also include this feature. The simulation of pilot lines is done by artificial pilot-circuits.

7.5.1 Artificial Pilot-Circuits

It is understood that the best way of testing a pilot-wire protection scheme, would be carried out on practical G.P.O. lines, preferably starting and ending in the same laboratory, where comprehensive bench tests can be conducted.

As a second best, where this facility is not available, tests of protective schemes can be performed on artificial pilot-circuits which have electrical characteristics similar and close to practical G.P.O. circuits. Several artificial pilot circuits have been constructed, for this purpose, to simulate the following:-

(a)   25 miles of 20 - lb/mile, unloaded, G.P.O. cable.

This line is constructed of ten sections, each representing 2.5 miles pilot length.

The line parameters are assumed $R' = 88$ ohms/mile, $C' = 0.065$ µF/mile, and G' and L' were neglected.

The total loop resistance, for 25 miles, is 2200 ohms giving $R/section = 220$ ohms. The capacitance $C/section$ is $= 0.1625$ µF.
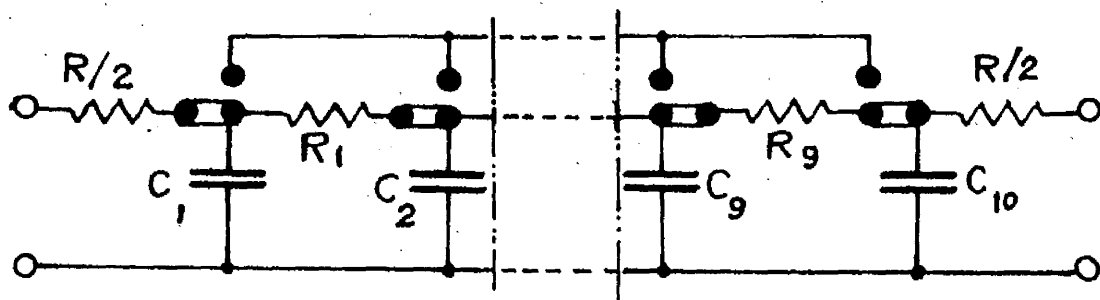
(b) 15 miles of 6.5 lb/mile, unloaded cable.

The parameters are $R' = 272$ ohms/mile and $C' = 0.065$ µF/mile. This artificial line comprises six sections each representing also 2.5 mile pilot length. The total pilot-circuit loop resistance is 4080 ohms, thus giving a resistance $R/\text{section} = 680$ ohms. The capacitance $C/\text{section} = 0.1625$ µF.

(c) Unloaded 40 lb/mile G.P.O. cable circuit of 20 miles length.

For a $R'/\text{mile} = 44$ ohms, and $C' = 0.065$ µF/mile, thus giving a total loop resistance of 880 ohms for 20 miles. This line comprises four sections each representing 5 mile pilot length and having a resistance $R/\text{section} = 220$ Ω and $C/\text{section} = 0.325$ µF.

This group of artificial lines, to simulate unloaded G.P.O. pilot circuits, is constructed from half-sections connected in tandem by a plug-in arrangement which allows the short-circuiting of any one or more of the sections. This arrangement provides the facility of connecting different pilot lengths from 2.5 to 25 miles of 20 lb/mile cable and from 2.5 - 15 miles of the 6.5 lb/mile pilot circuits, varying in steps of 2.5 miles each. The third artificial line of the 40 lb/mile cable provides simulation over a range of 5 - 20 miles pilot length in steps of 5 miles. These artificial line circuits are illustrated in Fig. (7.5), which shows also the sections of the
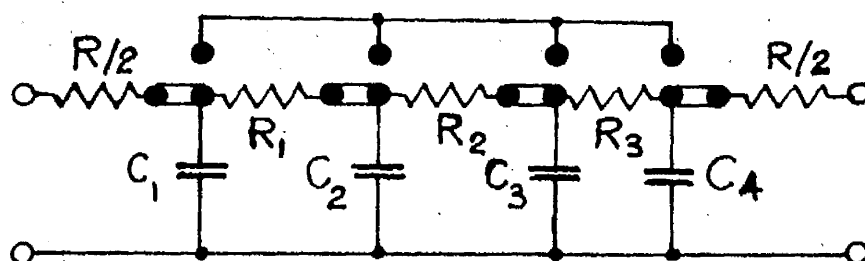
$$R = R_1 \rightarrow R_9 = 220 \, \Omega \quad , \quad C = C_1 \rightarrow C_{10} = 0.165 \, \mu F.$$

(a) 25 Miles of 20 lb/Mile Pilot Cable
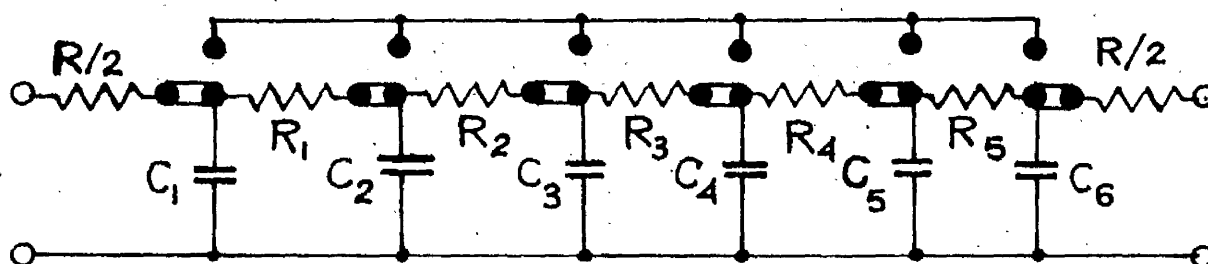
$$R = R_1 \rightarrow R_5 = 680 \, \Omega \, , \, C = C_1 \rightarrow C_6 = 0.165 \, \mu F.$$

(b) 15 Miles of 6.5 lb/Mile Cable

$$R = R_1 \rightarrow R_3 = 220 \, \Omega \quad , \quad C = C_1 \rightarrow C_4 = 0.35$$

(c) 20 Miles of 40 lb/Mile Pilot Cable

Fig. (7.5)   ARTIFICIAL PILOT CIRCUITS (UNLOADED CIRCUITS)

plug-in arrangement as well as the values of the capacitance

and resistance for the different components.

Table (7.1) gives the total capacitance and resistance of

each artificial circuits, together with the calculated values of

a practical homogeneous G.P.O. pilot-circuit.

	Artificial Circuits			G.P.O. Practical Circuits		
	(a)	(b)	(c)	(a)	(b)	(c)
R Ω	2300	4050	860	2200	4080	880
C μF	1.65	0.99	1.4	1.625	0.975	1.3
L m.H.	-	-	-	2.5	15	20

Table (7.1)   Comparison between Artificial and Practical
              G.P.O. Circuits (Unloaded)

(d)   20 lb/mile G.P.O. circuits loaded with 88 m.H.

coils/2000 yards. Two artificial circuits are con-

structed to simulate 5 miles each. Each circuit in turn

comprises 3 sections.

(e)   10 miles of a 20 lb/mile cable loaded with 88 m.H./

2000 yards. This circuit is composed of six sections

of the same type mentioned in (d).

The above three artificial line circuits simulate a

20 lb/mile G.P.O. loaded circuit for pilot-lengths from 5 - 20 miles,

in three steps of 5 miles each.

These artificial circuits are constructed using small air core inductors, resistances, and capacitances. The air reactors are constructed of 38 S.W.G. wire wound on bobbins illustrated in Fig. (7.6). The figure shows also the characteristics of the inductor coils. These inductors simulate the effect of loading coils, their inherent resistance has to be accounted for in the total resistance of the line.

Fig. (7.7) illustrates these three circuits and gives the values of the components.

Table (7.2) shows a comparison between the total capacitance, resistance, and inductance of the artificial lines and the values of calculated practical G.P.O. circuits.

	Artificial lines			Practical G.P.O. Circuits		
	(d)		(e)	(d)		(e)
R Ω	576.3	576	1170	460	460	920
C μF	0.315	0.315	0.6	0.325	0.325	0.65
L m.H.	354.5	342	694	392.5	392.5	785

Table (7.2) Comparison between Artificial and Loaded
G.P.O. Lines
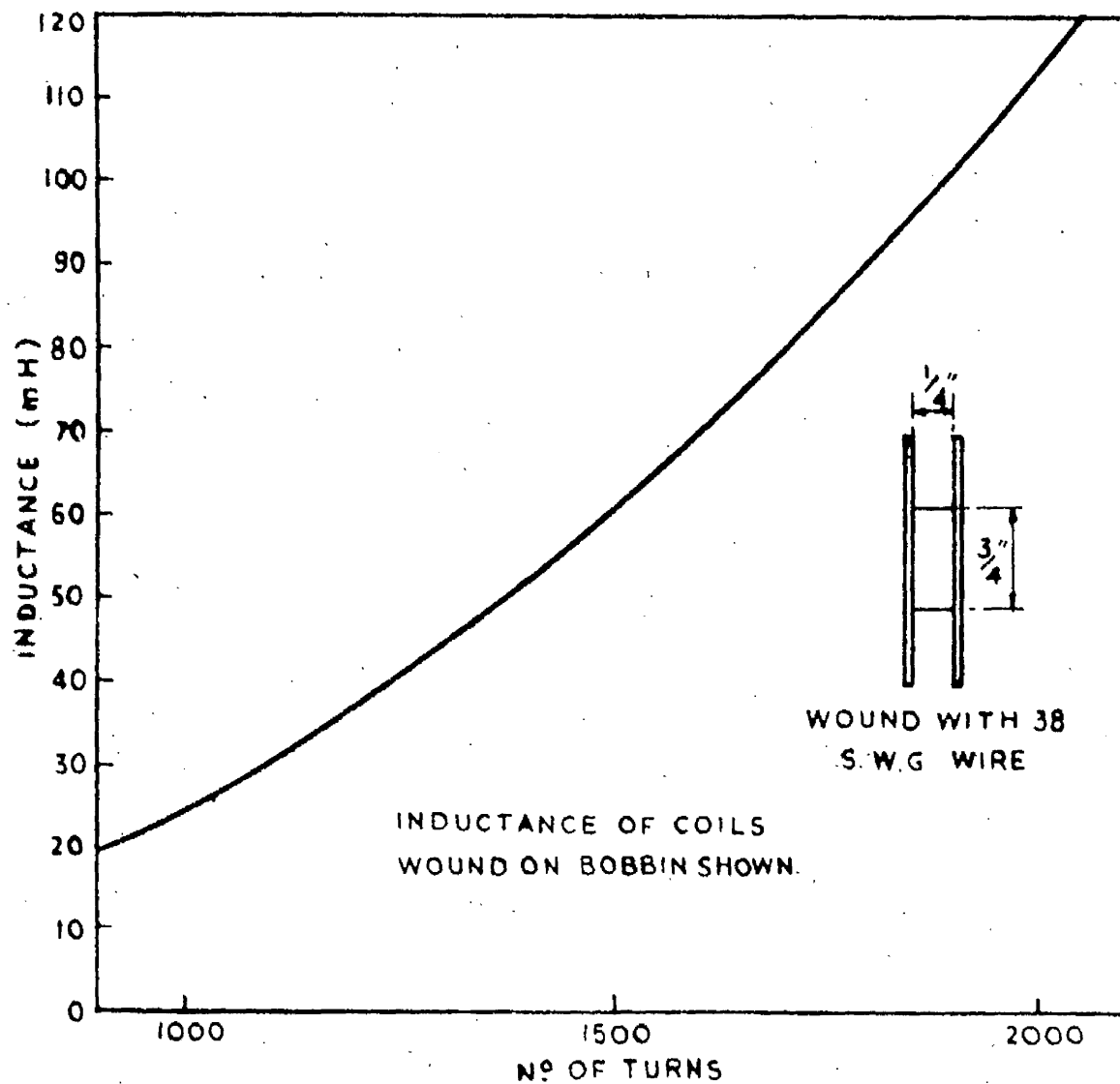
All the artificial line units can be connected in series,

Y-axis: INDUCTANCE (mH) — 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, 120

X-axis: Nº OF TURNS — 1000, 1500, 2000

INDUCTANCE OF COILS
WOUND ON BOBBIN SHOWN.

WOUND WITH 38
S.W.G WIRE

$\frac{1}{4}''$ $\frac{3}{4}''$

FIG. 7.6. LOADING COIL FOR ARTIFICIAL

G.P.O. CIRCUITS — DESIGN DATA.

59·5 mH   118 mH   116·5 mH   60·5 mH
113 Ω   175 Ω   172·5 Ω   116 Ω

53·5 mH   116 mH   116 mH   56·5 mH
110 Ω   173 Ω   177 Ω   116 Ω

$$C = 0·105 \; \mu F.$$
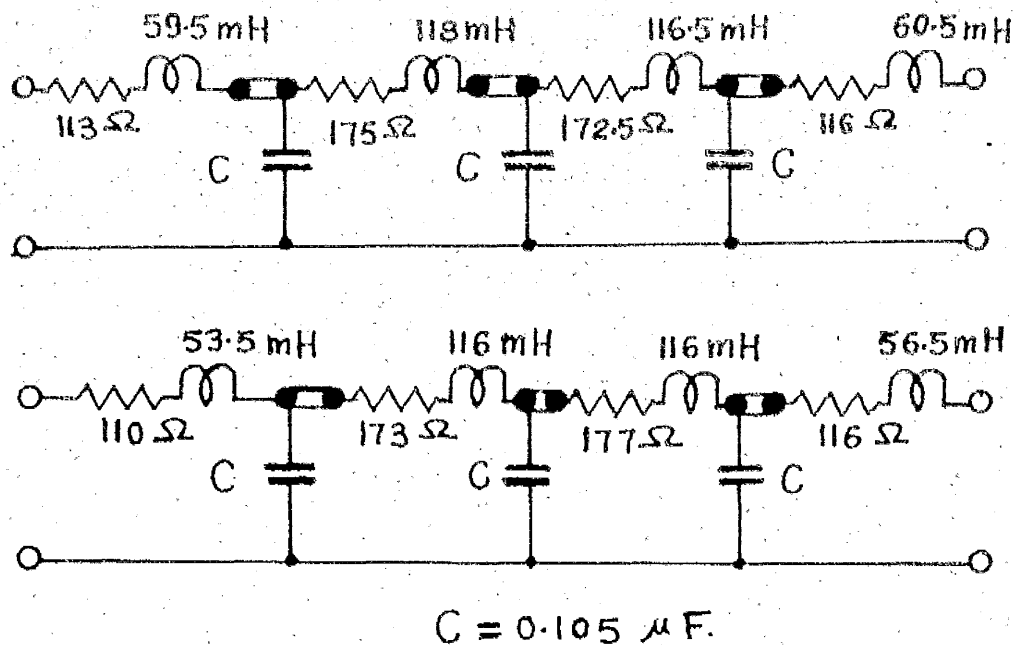
(d) "Two" 5 Miles of 20 lb/Mile Loaded Cable

50 mH   120 mH   120 mH   119 mH   118 mH   118 mH   50 mH
117 Ω   188 Ω   189 Ω   188 Ω   187 Ω   187 Ω   120 Ω

$$C = 0·1 \; \mu F.$$
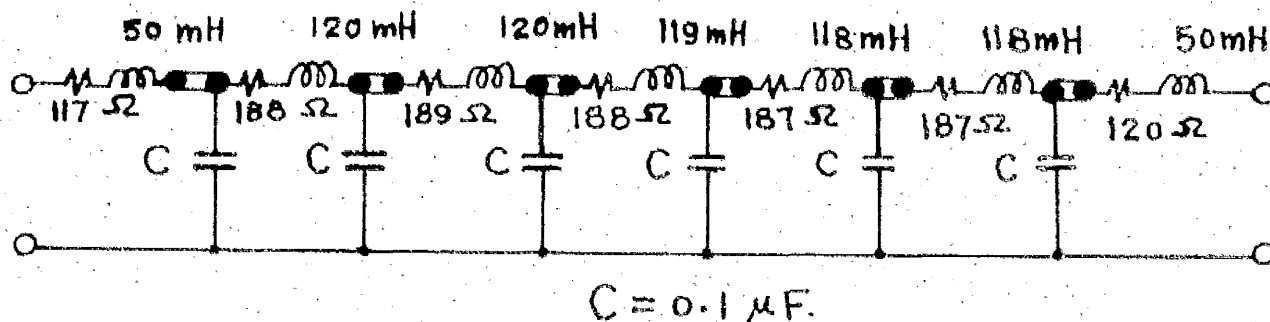
(e) 10 Miles of Loaded 20 lb/Mile Pilot Cable

Fig. (7.7)   ARTIFICIAL PILOT CIRCUITS (LOADED CIRCUITS)

or parallel if necessary, combinations to provide a large and
wide possible limits of length and of asymmetrical pilot circuits.
These artificial circuits are connected together without including
any matching devices to simulate as much as possible present G.P.O.
practice.

7.5.2 Mounting and Assembly

The artificial pilot lines mentioned in the previous section,
were assembled and mounted on two units. Figs. (7.8 and 9) show
complete views of these units. The plug-in arrangement and the
connections of the different sections of one line can be affected
from the front panel, as shown in Fig. (7.8).

The connections for the two terminating ends of a pilot
line are generally carried from the back side of the unit.
Fig. (7.8) shows also the two pilot-line isolating transformers
connected to the two ends of a line. These transformers form a
part of the differential bridge arrangement described in
section (8.8).

Fig. (8.9) shows the artificial line unit which was
designed for the early stages of the investigations.

7.6 Reliability of Pilot Wire Circuits

The reliability of the pilot link is an essential part of
the reliability of any pilot-wire scheme. However, any discussion

FIG. (7.8) ARTIFICIAL PILOT-LINES.

Front, Back and Underneath Views of the
Artificial Pilots Unit.
Pilot Isolating Transformers are also
shown.

FIG. (7.9) ARTIFICIAL PILOTS UNIT
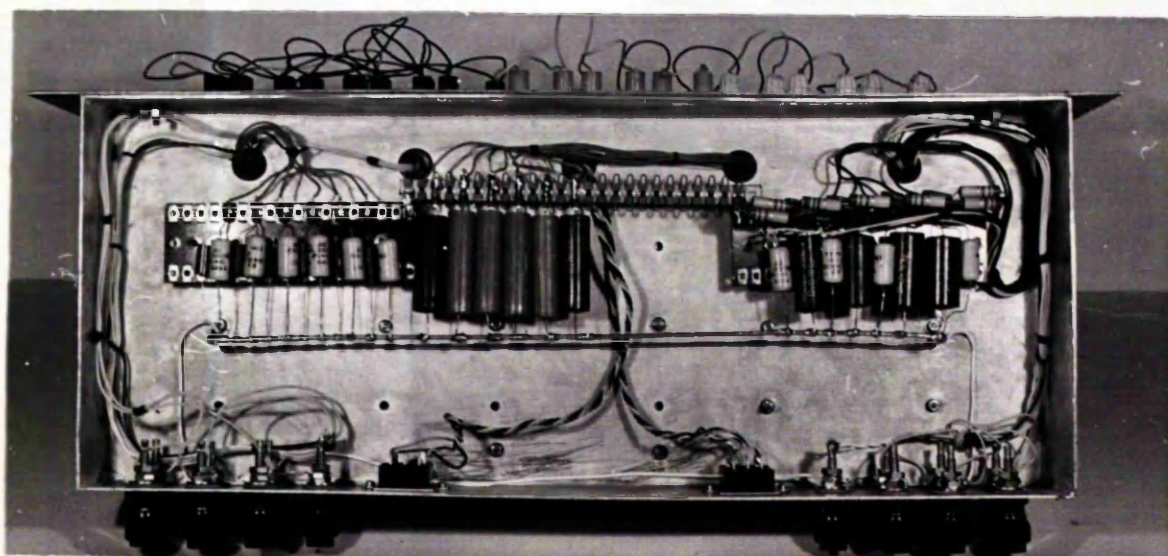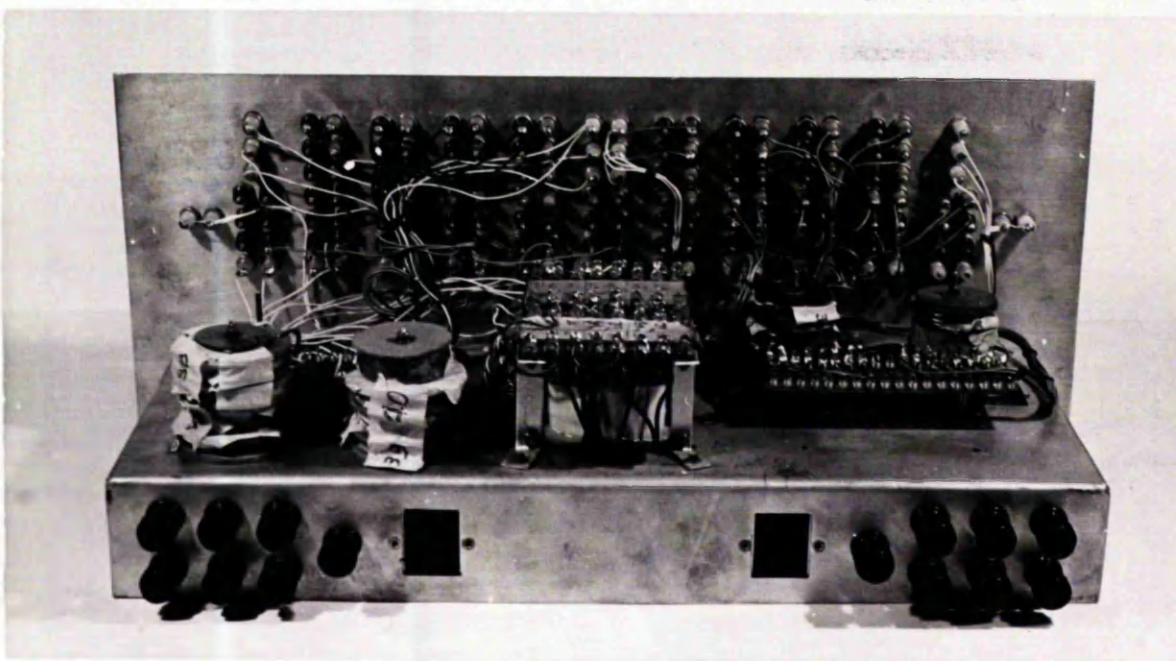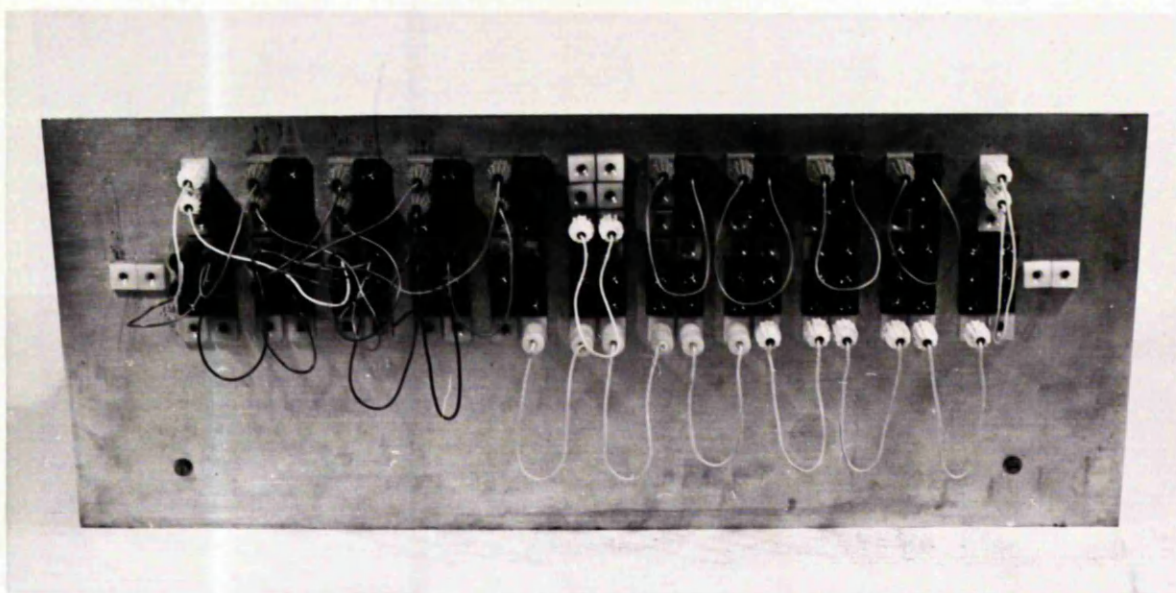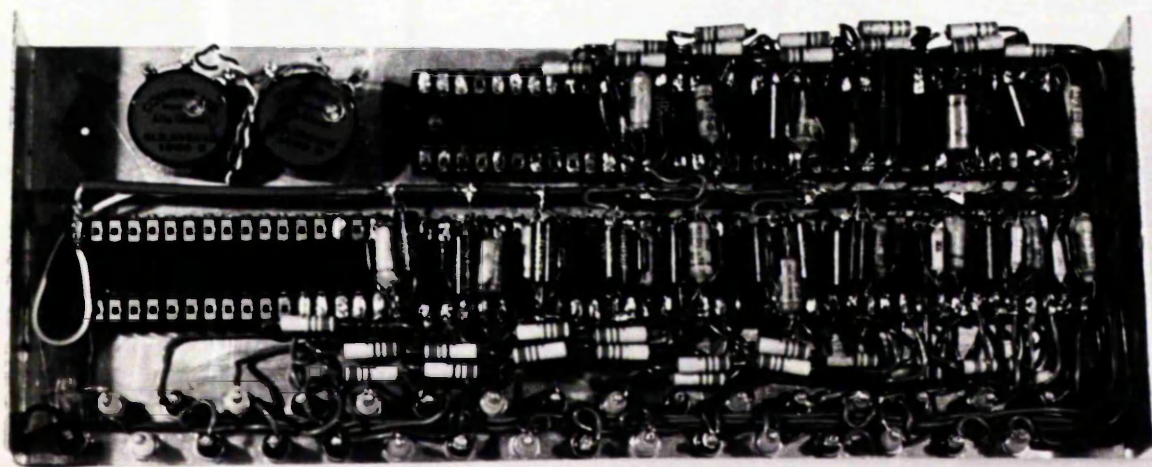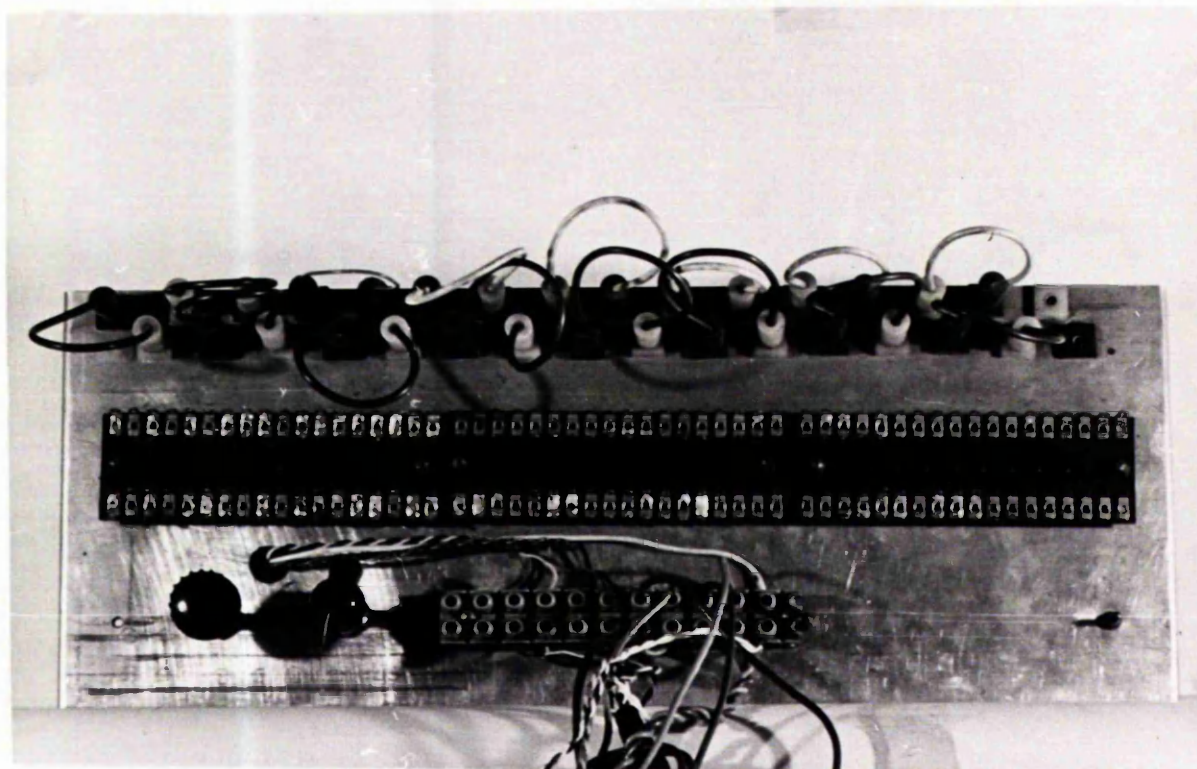FRONT AND REAR VIEWS OF CHASSIS.

FIG. 7.8.

FIG. 7.9.

on pilot wire reliability is closely attached to local circumstances.
In general private pilot circuits proved to be of higher
reliability and they are less exposed to failure due to human
intervention.

The performance of P.O. or leased pilot circuits depends to
a great extent on local conditions, e.g. high fault incidence in
areas subjected to flooding — etc. The reliability of P.O.
circuits depends also on available pilot route where main trunk
circuits give high record of availability than long local tenuous
circuits.

However a penetrating survey study of the problems associated
with pilot-wire relaying was carried out in the U.S.A.[14], based
on the use and experience gained over a large number of years.
The average outage time of leased circuits is quoted as 4.5
hours/circuit/year. However, the number of outages/circuit/year
is 1.37 and therefore the percentage availability is 99.93%.
This percentage availability represents outage time of 6.1 hours/
circuit/year for all outages, planned or otherwise. The
result of the survey indicated that the availability of leased
pilot-wire circuits are very high indeed.

On probability basis, the outage of a pilot circuit would
be expected to add only 0.07 percent incorrect operations to
those due to all other causes.

In the U.K. the figures published for the availability for

G.P.O. circuits is also quite high. The average outage time is about 15 hours/circuit/year, although in some cases an average as high as 22 hours/circuit/year[15] is also recorded and the number of outages/circuit/year is about 2.5 . It seems, however, that no full record, to the Author's knowledge, shows exactly the availability of G.P.O. circuits at time faults, i.e. the coincidence of pilot-circuit failures with the occurrence of faults on the power system which would be a correct measure of this availability. Other figures would be classified under probabilities.

The survey[14] carried out in the States is a thorough study for pilot-wire relaying from the application view point and similar study would be useful to assess the availability of G.P.O. circuits for protection.

CHAPTER 8

DESIGN OF TRANSISTORISED RELAYING CIRCUITS

8.1. Introduction

In the protective scheme developed, all the relaying functions are performed by transitorised circuits which are energised, in the first instant, by signals derived from the fault current. These circuits are connected and cascaded in such a manner, described in Chapter 2, as to produce the overall required performance of the scheme.

Transistorised circuits offer attractive advantages which include small size, small weight and very low power consumption. Static relaying devices, as those employed here, are also not prone to mechanical shocks or vibrations.

A common feature of these transistorised circuitry is the adoption, from the early stages of the investigations, of one common power supply rail at -10 Volts D.C. This is based mainly on economical reasons. Easier circuit designs could have been achieved by adopting power supply rails at (-10 V, 0, and +10V). Bearing in mind, however, the possibility of providing the power supply, in field applications, from station batteries a single voltage level (-10V) is therefore preferable to avoid complications. The possibility of providing separate power supplies for the final tripping stage as well as for the differential bridge circuit, if

required, is also considered.

Transistors in the relaying circuits are used as saturated amplifiers, or as switches, hence minimising instability risks and drift due to temperature and power supply variations.

Simplicity and economy are the two aims to be achieved in the design of the scheme circuitry.
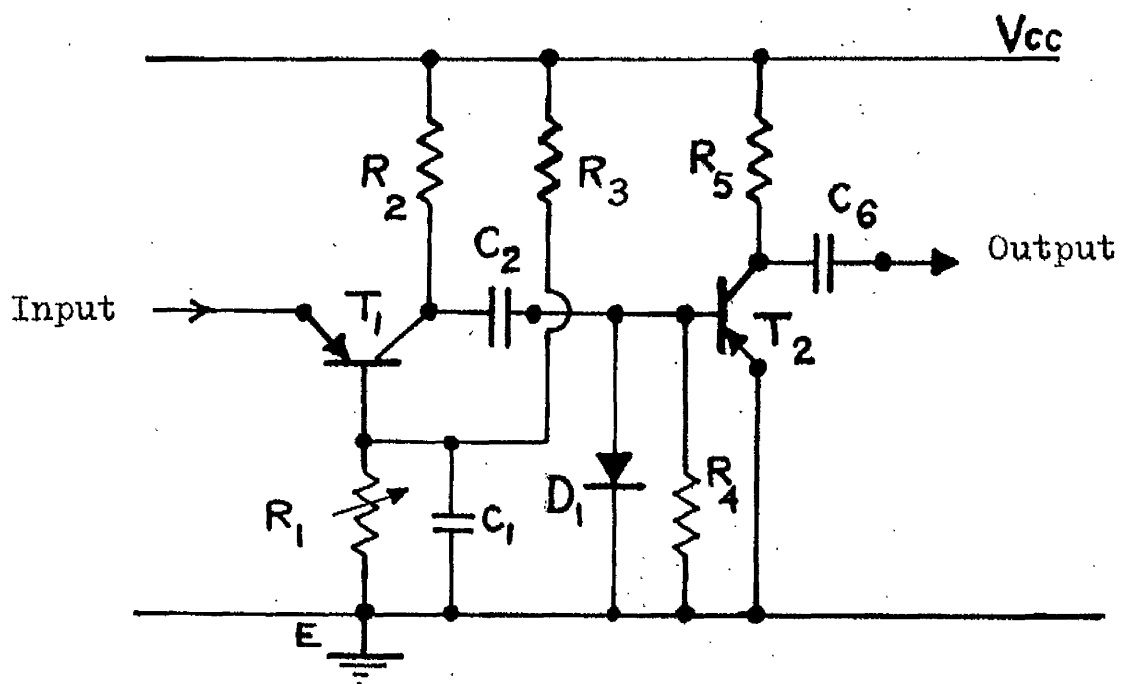
8.2. Squaring Circuit

The function of this circuit has been explained in sec. (2.5.2). It produces square-wave outputs of unity mark to space (M/S), when an A.C. relaying signal, representing the phase angle of the fault current, is applied to its input terminals.

In order to obtain unity "M/S" it is important that the A.C. signal should be free from any unidirectional components. This has been considered in sec. (3.6), and it is concluded that the output voltage of ironless-core C.T.s is almost free, from the practical viewpoint, from unidirectional transients.

The squaring circuit should also have a low input impedance for reasons described earlier in sec. (6.4.4.). An immediate answer would be the use of a transistor circuit T_1, Fig. (8.1), in a common base configuration.

Such a circuit offers the lowest input but highest output impedances. The current gain "α" is a little less than unity, voltage or power gain are therefore due to the output/input impedance ratio. Other advantages for adopting this circuit

(A) Circuit Arrangement

(a) Input Voltage Wave

(b) Collector of T_1

(c) Input Voltage to T_2

(d) Output Wave Shape
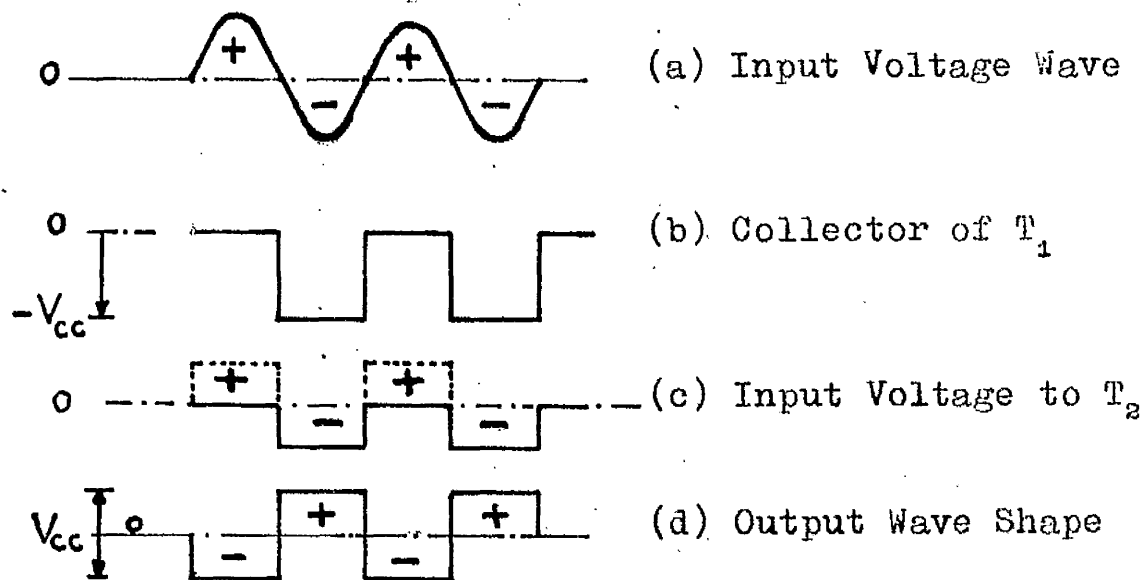
(B) Wave Forms

FIG. (8.1) SQUARING CIRCUIT.

configuration are, its (V_C versus I_C) linear characteristics at very small values of currents and voltages as well as a very small collector leakage current I_{CO}. These characteristics, i.e. very low I_{CO}, and "α" being less than unity, make such a circuit inherently temperature stabilized. Other transistor circuit configurations with compensating elements, could hardly approach such a temperature stability limit.

The input voltage to the emitter of T_1, Fig. (8.1), has to overcome the forward resistance of the emitter to base junction before any collector current starts flowing, (for p-n-p transistor on the positive half cycles of the input voltage), i.e. deriving T_1 to conduction.

The collector of T_1 thus attains a voltage depending on the magnitude of the base potential, neglecting the residual voltage (Vec) of the transistor when bottomed. The collector attains a voltage approx. equal to (-Vcc), if the collector leakage current is neglected, during the negative half cycles of the input voltage waveform. Hence the collector of T_1 will follow almost a square wave having a magnitude (Vcc), Fig. (8.1B), as the input signal passes through its zero points.

To achieve a unity mark to space ratio for the wave shape of T_1 and to eliminate the effect of the forward voltage of its emitter/base junction, the base of T_1 was biased slightly negative through R_1 and R_3. The biasing resistance R_1 is shunted by a

condenser C_1 to reduce its effect in increasing the A.C. input impedance.

The value of R_3 is chosen high enough not to cause any appreciable drain on the power supply. Then the value of R_1 could be easily fixed to give the small amount of negative biasing required. The circuit is also designed that if R_1 is adjusted for the lowest possible setting of input signal to give a unity mark to space ratio, then this value of R_1 will be also suitable for the highest setting to be reached with a departure of not more than 4.0% in the mark/space ratio. The range of the settings over which such an error occurs is about 1:100.

Transistor T_1 is operating as a saturated amplifier with half-sinusoidal voltage input signals. Therefore the square-wave output of its collector would in fact be a part of a very large sine wave, its amplitude is determined approx. by the product of the emitter current and the collector load R_2. At very small input current settings, the change of state of the saturated amplifier is not fast enough and this leads to the introduction of another stage composed of transistor T_2.

This second stage is composed of a transistor T_2 in the common emitter configuration which gives maximum power gain, this being one reason for its use in most switching applications. Another reason is the fact that it requires minimum input power to switch the transistor from cut-off to fully conducting state and vice-versa,

thus eliminating the loading effect on the first transistor T_1.

In sec. (2.5.2.), an arrangement for controlling the unity "M/S" ratio of the square wave by the use of a zero level detector followed by an invertor stage is discussed. The level detector is similar to the type described in sec. (8.3.3.). This procedure has proved to be not essential, as the performance of the squaring circuit, as it stands in Fig. (8.1.) is quite satisfactory with a deviation within ± 4% over the whole range of settings.

Fig. (8.2) shows the input wave shape and the square-wave output of the circuit for different values of input signals, from minimum setting Fig. (8.2A), to a value about 40 times setting in Fig. (8.2F). The variation in the mark/space ratio could hardly be noticed.

This second stage transistor T_2, Fig. (8.1), is driven from the collector of T_1 through C_2 to give the collector full swing. The capacitor C_2 discharges instantly through diode D on the positive half cycles of the collector swing.

It is clear that the output square wave, Fig. (8.1B), is of unity mark/space and has an opposite polarity to the input wave signal.

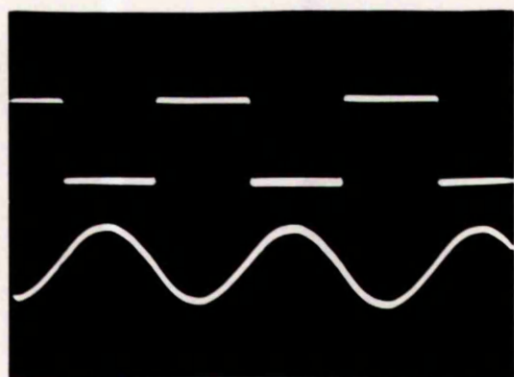## 8.3. Fault Detectors or Starting Circuits

The starting circuits mainly function, as explained in sec. (2.5.1.), in the scheme devoloped, as fault detecting elements.

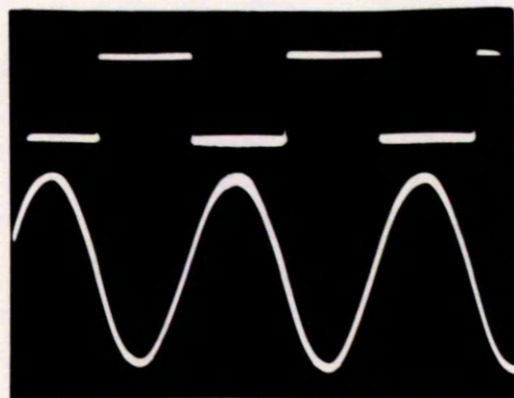## FIG. (8.2) BEHAVIOUR OF THE SQUARING CIRCUIT.

Input and Output Wave Forms
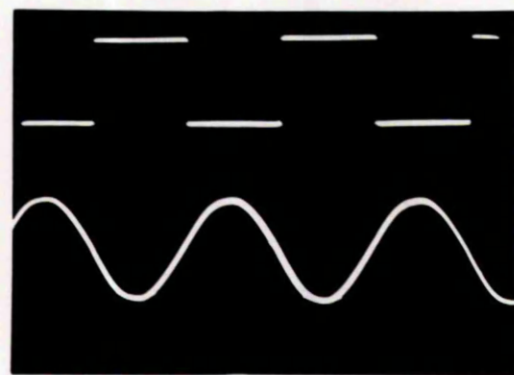
(A)   at minimum setting.
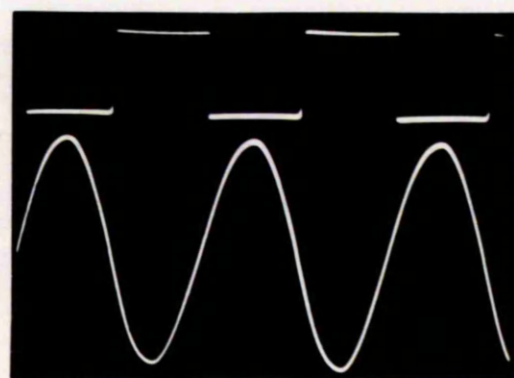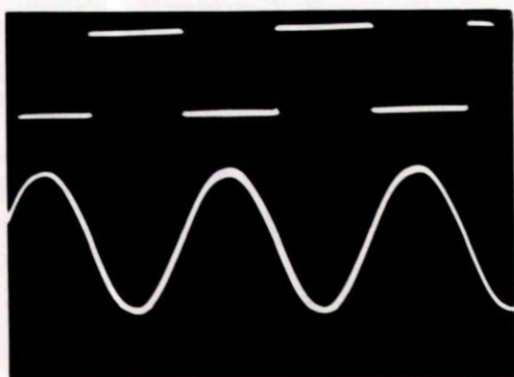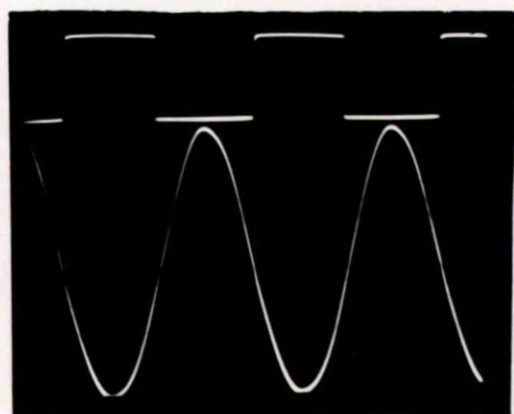
(B)   at about 40 times setting.
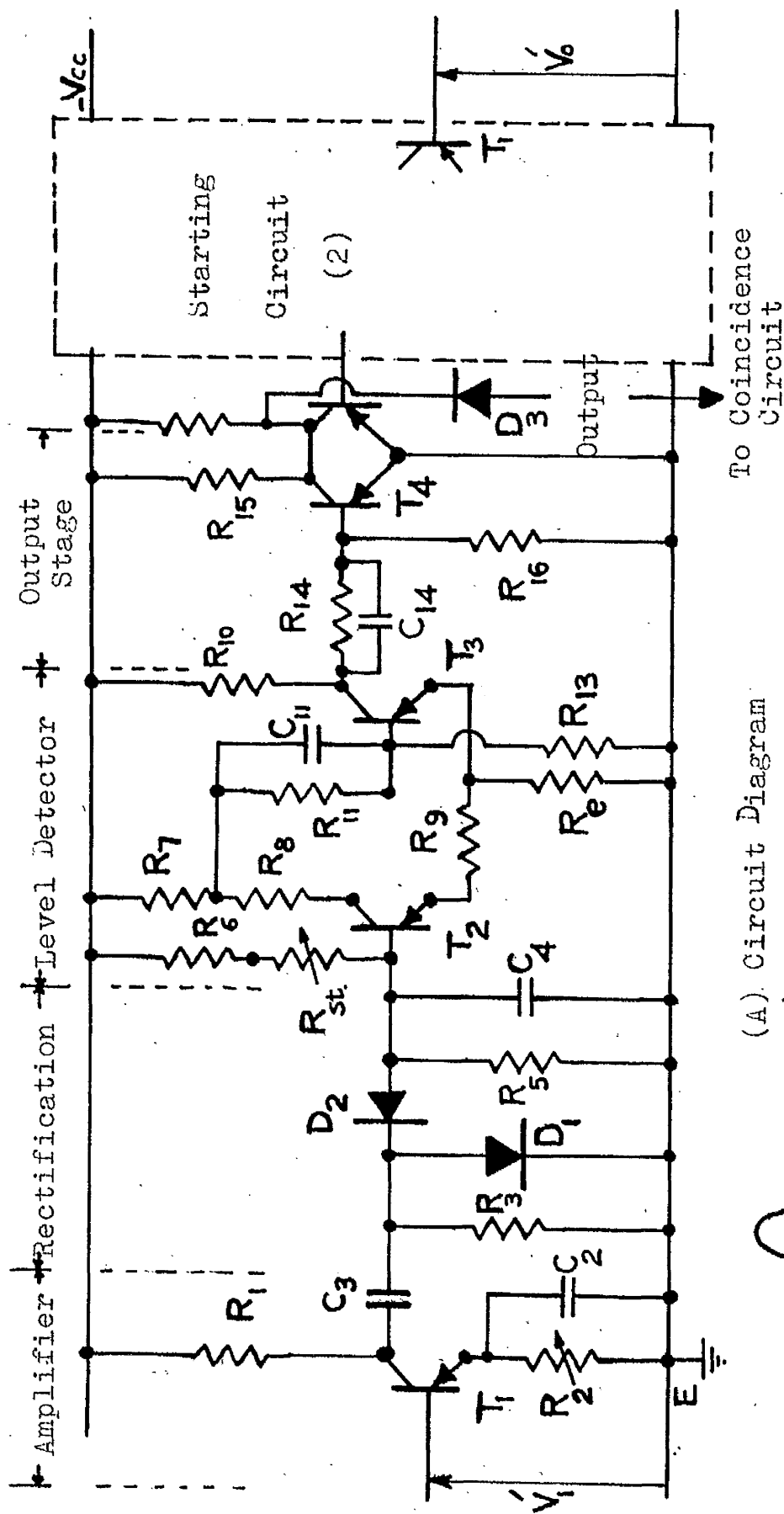
A

B

C

D

E

F

FIG.8.2.

They are designed to respond to the magnitude of the positive-sequence component of the fault current to detect balanced faults, and to the magnitude of the zero-sequence component to detect fault conditions involving earth. They produce starting signals to control the coincidence/phase comparator circuit which in turn controls the tripping circuit. The absence of these starting signals inhibits phase comparison, between the square-waves representing the phase angle of the currents at the two ends of the protected section, from taking place.

The starting circuits arrangement is illustrated in Fig. (8.3). It consists of two identical transistorised circuits. Each circuit is composed of four main parts, namely, an input amplification stage, followed by a half-wave rectifying and smoothing which is followed by a level detector of the emitter coupled type. The final stage is simply an invertor combined with an (OR) gate arrangement for the two starting circuits. The output of the gate is fed through diode D3 to the coincidence gate. The output of the starting circuits is in the form of a voltage step, i.e. a sudden change in voltage level, as soon as the input signal to the circuit reaches a predetermined value.

8.3.1. The Amplifier

The input signals, which are proportional to the positive sequence and the zero-sequence components of the fault current, as explained in sec. (6.4.4.), are applied each to one of the starting circuits.

Amplifier → Rectification → Level Detector → Output Stage

Starting Circuit (2)

$-V_{cc}$

R_1 R_2 C_2 C_3 R_3 D_1 R_5 D_2 $R_{st.}$ C_4 T_1 V_1' E

R_6 R_7 R_8 R_{11} R_9 R_e R_{13} C_{11} T_2 T_3 R_{16}

R_{10} R_{14} C_{14} R_{15} T_4 D_3 Output

To Coincidence Circuit

T_1 V_6'

(A). Circuit Diagram

Input (small)   Ampl. Output   rectified Wave   Level Detect.   Circuit Output

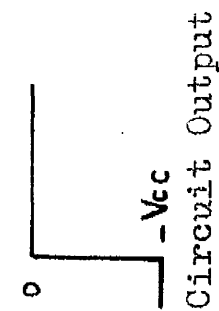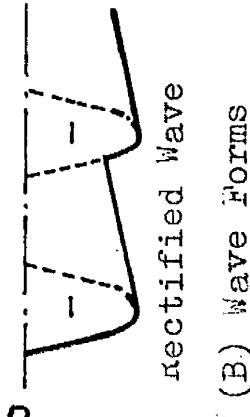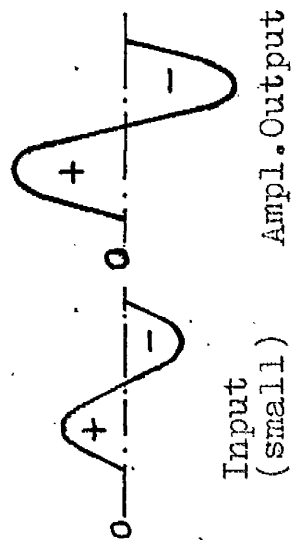+ 0 −   + 0 −   0 −   0   D.O.Level / P.U.Level   0 / $-V_{cc}$

(B) Wave Forms

FIG. 8.3)   STARTING CIRCUIT ARRANGEMENT.

The input signal is applied to the base of transistor T_1, Fig. (8.3), where the signal is amplified in a one stage amplifier of the common emitter type which has a rather high current gain β. The voltage gain of this stage is controlled by the values of R_1 and R_2 or by the value of R_1 provided the emitter circuit resistance R_2 is kept constant.

The amplifier of starting circuit (1) which responds to the magnitude of the positive sequence components, is designed to saturate at high input values corresponding to multi-phase faults. This means that if the fault current reaches a certain level the amplifier operates as a switch and its output is near in form to a square-wave.

On the other hand, the second starting circuit operated from the zero sequence component of the fault current, is adjusted by designing the operating point of the amplifier to cause saturation if the zero-sequence input signal reaches a very low level determined by the harmonics and the errors produced from the segregating networks, sec. (6.4.3).

The output of the amplifier, for either of the two starting circuits, is taken from the collector of T_1, Fig. (8.3), as an amplified sinusoidal wave for small inputs and almost as square-wave at high input levels, through C_3 to the half-rectifier stage.

To reduce the effect of temperature variations on the amplifiers, silicon transistors are used and proved to be satisfactory

without adding complicated temperature compensating circuits.

8.3.2. Rectification Stage

Since the input signal to this stage is an A.C. one and in order to operate a D.C. level detector to determine its amplitude, a rectification stage has been introduced between the amplifier and the level detector.

The input signal to the starting circuit is rectified by D_2, Fig. (8.3A), after being amplified in T_1. This half-wave rectifier allows current to flow on negative half-cycles only.

During positive half-cycles the current flows through diode D_1 thus discharging the coupling capacitor C_3 to a very small positive value equal to the forward residual voltage drop across D_1. Alternatively, during negative half cycles current flows through D_2 and by proper choice of the values of C_4 and R_5, neglecting the shunting effect of $(R_6 + R_{st})$ on R_5, the maximum allowed value of the ripple could be determined. The forward resistance of the rectifier D_2 should be taken into consideration. The criterion for the maximum ripple value, could be demonstrated as follows:-

In order to obtain rapid response, i.e. to minimize delay, the time constant $R_{D2} C_4$ of Fig. (8.4), should be as small as possible; while in order to obtain minimum ripple in the d.c. output $R_5 C_4$ should be as large as possible. In other words, low value of C_4 gives faster response and higher percentage of ripple,
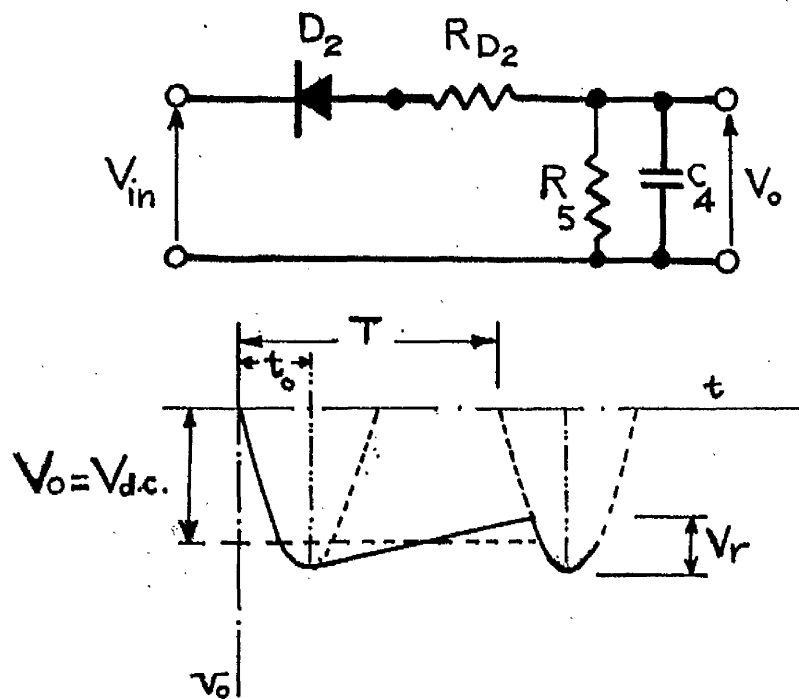
FIG. (8.4)   RECTIFICATION STAGE.
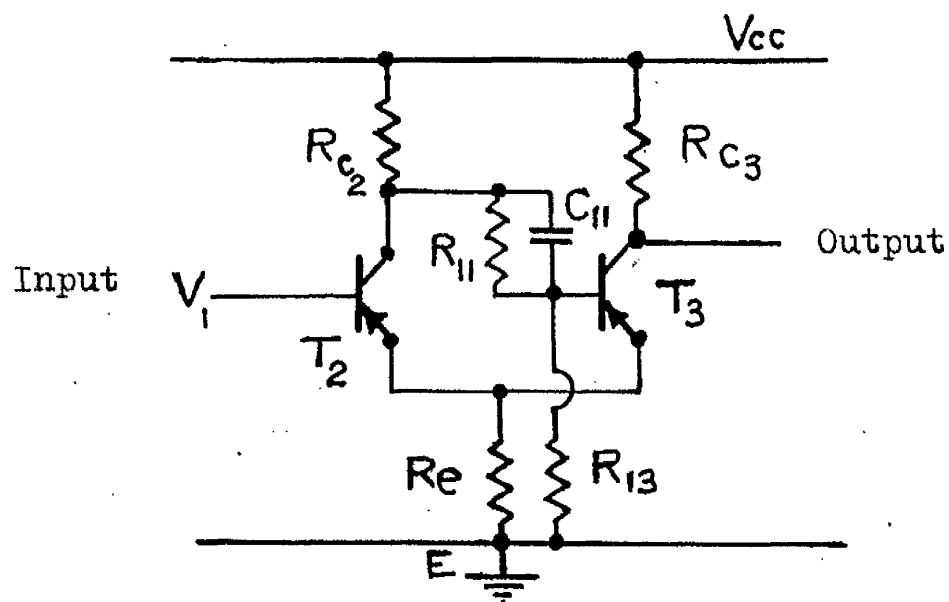
FIG. (8.5)   BASIC EMITTER COUPLED TRIGGER CIRCUIT.

and vice-versa.   In this case, R_{D_2} is, in fact, very small being the forward resistance of the diode D_2.   The time constant $R_{D_2}C_4$ is much smaller than $R_5 C_4$ and therefore the charging time of capacitor C_4 can be neglected

The discharging time through R_5, assuming $(R_6 + R_{at})$ very large w.r.t. R_5, should be equal to a period "T" of one cycle.

The output voltage after time $t_o = T/4$, which is repeated every cycle, is given for the first period by:-

$$v_o = -V_{max.} \cdot e^{-(t-T/4)/R_5 C_4} \qquad \ldots\ldots (8.1)$$

where $T/4 < t < 5T/4$

It can be seen that the output voltage is not therefore composed of a constant D.C., but contains an amount of ripple voltage v_r given by:-

$$v_r = V_{max.} - V_{min.} \qquad \ldots\ldots (8.2)$$

where $V_{max.}$ is the peak value of the A.C. voltage V_{in}, and V_{min} is the instantaneous value of the voltage v_o given by eqn (8.1) when t reaches a value between T and $5T/4$.   From eqn (8.2), and at $t = T$ it follows:-

$$V'_{min.} = -V_{max.} e^{-3T/4 R_5 C_4} \qquad \ldots\ldots (8.3)$$

and for $t = 5T/4$, it gives:-

$$V''_{min.} = -V_{max.} e^{-T/R_5 C_4} \qquad \ldots\ldots (8.4)$$

An average value $V_{min.}$ between $V'_{min.}$ and V''_{min} would represent approx. the actual value:-

Hence $\quad V_{min.} = -V_{max.}\; e^{-7T/8R_5C_4}$ $\qquad$ ..... (8.5)

Since this rectified output is applied as input to the level detector, of the type described in sec. (8.3.3.), it is therefore essential that:-

$$V_p - V_d \geqslant V_{rm} + i_{bm} \cdot R_b \qquad ..... (8.6)$$

where V_p and V_d are the level detector pick-up and drop-off voltages respectively, V_{rm} is the ripple voltage at marginal conditions, i.e. when $V_{max.} = V_p$, i_{bm} is the base current, at min. setting, required to operate transistor T_2 of the level detector and R_b is the equivalent base circuit resistance of T_2.

8.3.3. The Level Detector Circuit Arrangement

This circuit is designed as a trigger circuit to respond to the value of the input signal and to produce a stepped output which is fed, after being inverted, to control the coincidence circuit sec. (8.4). The level detector circuit is of the emitter coupled type, its basic arrangement is shown in Fig. (8.5). The two possible stable states of the circuit are controlled by the input voltage level V_1, i.e. the change from one stable state to the other occurs as the input voltage V_1 passes through a predetermined value. The two transistors T_2 and T_3 are coupled in a non-

symmetrical way. A collector-to-base coupling is used from T_2 to T_3, while a common emitter resistance R_e completes the regenerative loop. The behaviour of the circuit could be easily explained by assuming, in the first instance, that the magnitude of the input voltage V_1 is negative but not enough to cause T_2 to be bottomed, i.e. T_2 is off. In such a condition T_3 is in a state of conduction, it is also assumed that T_3 is not biased into saturation. Neglecting the collector reverse leakage current I_{co} of T_2, a certain voltage level is set across the common emitter resistance R_e due to the conduction of the transistor T_3. If the input voltage V_1 is increased negatively beyond the common emitter level, T_2 starts to conduct. With both transistors conducting, loop re-generation causes T_3 to cut off quickly. With T_3 in a non-conducting state, T_2 would operate at whatever point the input voltage V_1 sets itself according to design. Wherever the operating point of T_2 on its load line may be, the output taken from collector of T_3 will not be affected since T_3 is cut off.

However, if the input voltage reduces its negative value such that the base of T_3 is more negative than the common emitter voltage, T_3 would turn to conduction again and loop regenerative effect leads to drive T_2 into non-conduction state.

The two critical values of the input voltage levels (V_p, pick-up voltage and V_d, drop-off voltage) differ and, therefore, the circuit exhibits an inherent back-lash or hysteresis, and for

input voltage levels between V_p and V_d, the circuit can be in either one of its two stable states.

When T_2 is cut-off the equivalent circuit could be represented as shown in Fig. (8.6A). T_2 will start to conduct when V_1 exceeds V_{e3} negatively.

The pick-up voltage V_p is then equal to V_{e3}. Neglecting I_{co} of T_2 and taking $V_{b_2} = V_p + V_{be3}$, then:-

$$V_p + V_{be3} = \frac{V_{cc} R_{13} - (I_{c3}/\beta_3) R_{13}(R_{c_2} + R_{11})}{(R_{c_2} + R_{11} + R_{13})}$$

$$\dotsc\dotsc (8.7)$$

and

$$V_p = R_e \frac{I_{c3}}{\alpha_3}$$

$$\dotsc\dotsc (8.8)$$

where α_3 and β_3 are the gain of $T3$ in common emitter and common base configurations, respectively.

When transistor $T3$ is cut off and just about to conduct, i.e. when the input voltage V_1 equals the drop-off voltage V_d, as in the equivalent circuit of Fig. (8.6B), it follows therefore that:-

$$V_{cc} - V_{c_2} = (I_{c_2} + I) R_{c_2}$$

$$V_{e3} - V_{c_2} = (I R_{11}), \; V_{e_2} = (I.R_{13}) = (\frac{I_{c_2}}{2})R_e$$

$$\Bigg\} \dotsc (8.9)$$

Hence the input voltage $V_d = V_{e_2} + V_{be_2}$ $\dotsc\dotsc (8.10)$

The difference between the levels of Vp and Vd determines the sensitivity of the circuit as a level detector. In order to reduce this inherent back-lash (i.e. to reduce the difference between Vp and Vd). Either Vp is reduced, (i.e. becoming less negative) to
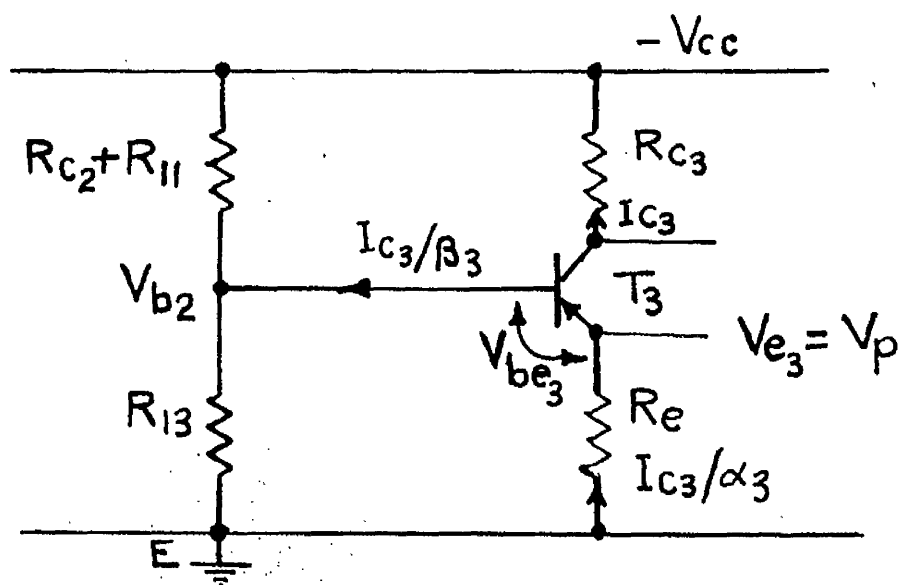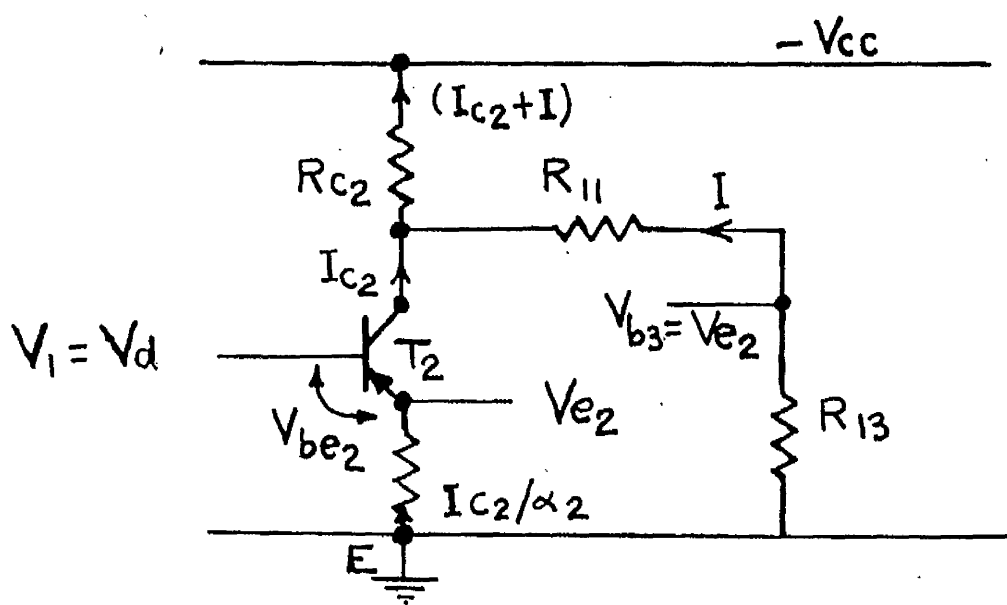
FIG. (8.6) EQUIVALENT CIRCUITS OF EMITTER COUPLED
LEVEL DETECTOR

approach Vd by adding a resistance in the emitter circuit of T_3.
Alternatively, this can be approached by increasing Vd (i.e.
becoming more negative) to approach Vp. This could be achieved by
introducing a resistance in the emitter circuit of T_2. These
methods of introducing resistances in either of the emitter circuits
of T_2 or T_3, in order to reduce the hysteresis, would produce
series negative feedback, and hence a reduction in gain. To restore
partially the gain during transition, these emitter resistances
should be shunted by capacitors. Using such a method to improve
the sensitivity of the detector, care should be taken to ensure
that as the drop-off voltage Vd approaches the pick-up voltage Vp,
no risk of instability should occur.

In the particular application of the level detector as part
of the starting circuit, the pick-up voltage is adjusted slightly
more negative than that of the drop-off. This allows for some
percentage ripple, as described in the previous section, and avoids
instability, "chattering", under marginal conditions. The
difference between Vp and Vd is controlled by inserting resistance
Rg, Fig. (8.3), in the emitter circuit of T_2.

The sensitivity of the circuit with respect to the input
signal is improved by superimposing a negative bias at the base
of T_2. This is provided by a potential divider $R_5/(R_6 + R_{st})$,
Fig. (8.3). The value of this bias, when T_2 is cut-off, is made
variable over a reasonable range by changing R_{st}. The maximum

magnitude of the biasing voltage can be made just equal to Vd, the drop-off voltage of the level detector.

The maximum biasing voltage Vb, when Rst = 0 and T_2 being cut-off, is given by:-

$$Vb = \frac{-Vcc\ (R_5)}{(R_5 + R_6)} \quad Vd \quad \quad \ldots\ldots (8.11)$$

The effect of this biasing on the output of the rectification stage, sec. (8.3.2), would be equivalent to shifting the zero line in a negative sense, or in effect to changing the value of the lowest setting to which the level detector responds, i.e. increasing or decreasing the overall sensitivity of the combined rectifier/detector circuit.

8.3.4. <u>Output Stage/(OR) Gate Arrangement</u>

An output stage has been introduced, following the level detector, to produce a stepped output signal. This voltage signal changes its magnitude , suddenly from -Vcc to almost zero level, as soon as the magnitude of the input signal to the amplifier stage reaches a predetermined threshold level. This output signal is employed as a "let go" signal for the phase comparator circuit. Its absence inhibits phase comparison between the currents at the two ends of the feeder, as mentioned in sec.(2.5.1), and explained in more detail in sec.(8.4).

From the previous section it has been established that the output of the collector of transistor T3, Fig. (8.3), acquires two stable states, namely either at approx. (-Vcc) or at

$-(V_{CC} - I_{c3} R_{c3})$ depending on the input signal magnitude. Both these two levels are, of course, negative and neither of them is at zero level due to the nature of the coupled emitter circuit which has a common emitter voltage $V_{e3} = Re \cdot \dfrac{I_{c3}}{\alpha_3}$. To obtain a step signal having an amplitude of $-V_{CC}$ to 0, another transistor T_4 of the common emitter configuration is introduced as a combined output/(OR) gate stage. This transistor T_4 is operated from the level detector described in the previous section.

The resistance R_{14}, Fig. (8.3), in the base circuit of T_4 is made big enough to make T_4 just cut-off when T_3 is conducting. Any negative increase of the collector voltage of T_3 would cause T_4 to conduct and the voltage of its collector will be the residual voltage across it, which is small enough to be considered at zero level.

As the output voltage of the level detector is in the form of a step, a shunting capacitor C_{14} across R_{14} helps to speed the switching operation of T_4. The resistance R_{16} is also added for temperature variation stability as well as helping to turn T_4 to the cut-off state.

The output of the invertor T_4/(OR) gate circuit is taken from its collector through a diode D_3 which allows current to flow only when the collector voltage is negative, i.e. when T_4 is cut-off.

The protective scheme developed comprises two starting circuits as fault detecting elements.

Hence, it is necessary to provide a gating arrangement for

the two stepped outputs from the starting circuits to control the coincidence/phase comparator circuit. This gating arrangement allows either of the two outputs to reach the coincidence circuit, i.e. in an (OR) gate arrangement.

Advantage is taken of the presence of transistor T_4 as a combined invertor/(OR) gate, thus economising in the number of circuit elements. In this arrangement the two transistors T_4, of the two starting circuits, being in an earthed emitter configuration, are joined to have a common collector connection at R_{15}, Fig. (8.3), where the output is taken.

The output point would attain a zero voltage level if either of the two transistors T_4 is conducting and has a voltage value of approx. $(-Vcc)$ if both are in the cut-off state. This stepped output voltage is used to bias the coincidence circuit or as an inhibiting signal to the phase comparator and in special cases of pilot-link failures is required to initiate tripping as explained in sec. (2.5.4) and in the next section.

8.4. Coincidence/Phase Comparator Arrangement

The coincidence/phase comparator circuit followed by the tripping circuit constitutes the main relaying element of the protective scheme.
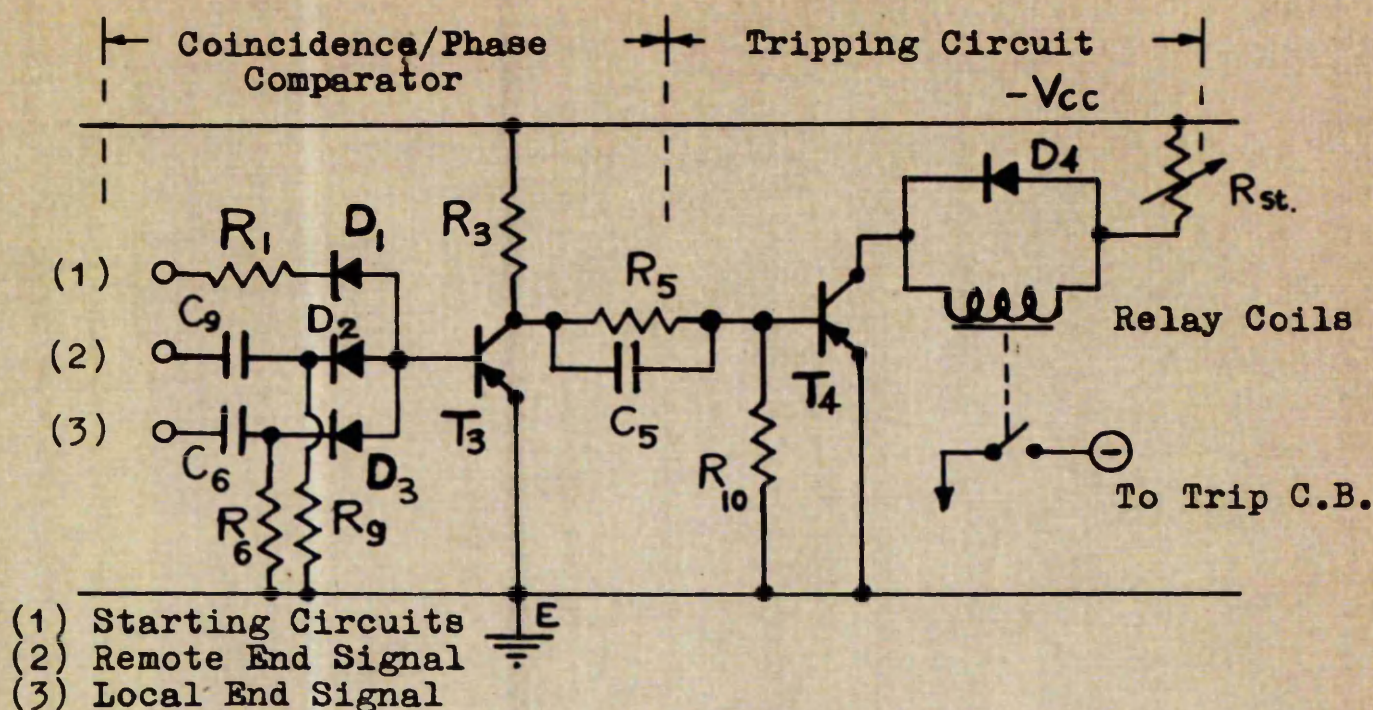
The main functions of this circuit, in the developed scheme, are described in sec. (2.5.4.).

The basic arrangement of the coincidence/phase comparator circuit is shown in Fig. (8.7).
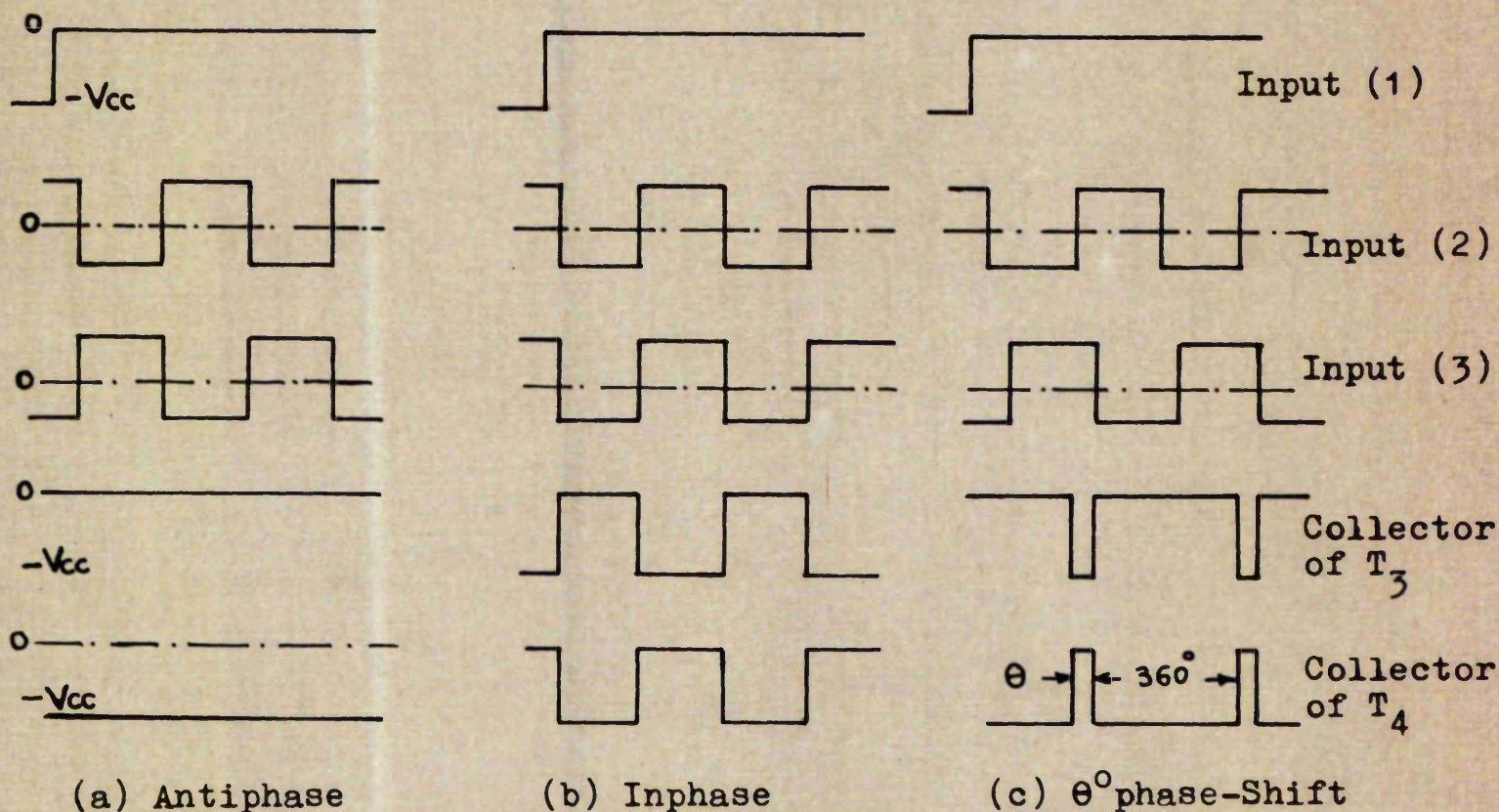
Three inputs (1), (2) and (3) are fed through diodes D_1, D_2 and D_3, respectively, to the base of transistor T_3. Input (1) is fed from either of the outputs of the starting circuits, as explained in the previous section, and is normally having a negative value of approx. (-Vcc). This input, therefore, maintains transistor T_3 in a conducting state, irrespective of the other two inputs (2) and (3).

When the starting circuit changes stage, i.e. picks-up, input (1) attains zero potential, thereby allowing phase comparison to take place between inputs (2) and (3) because of their A.C. coupling nature to T_3. Input (2) is the square-wave derived from the local end current of the feeder, after being appropriately phase shifted. While input (3) is another square-wave received from the remote end of the feeder, after being properly reshaped. When either or both of the two square-wave inputs are negative, transistor T_3 will be in conducting state, provided input (1) is zero. It is clear, of course, that if both inputs (2) and (3) are positive or zero, T_3 will be in cut off state, provided that input (1) is already zero.

This gating arrangement produces an output train of negative pulses, at the collector of T_3, with a pulse duration equal to the overlapping angle θ° between input (2) and (3). The angle "θ" being

(A) Circuit Diagram

(1) Starting Circuits
(2) Remote End Signal
(3) Local End Signal

(a) Antiphase   (b) Inphase   (c) θ^o phase-Shift

(B) Wave Shapes

FIG. (8.7) COINCIDENCE AND TRIPPING RELAY CIRCUITS.

the departure of the 2 square-wave inputs from the anti-phase position, as shown in Fig. (8.7B).

Since the square-wave inputs (2) and (3) have a unity "M/S" ratio, then the output pulses are in the form of a train 360° apart, as shown in Fig. (8.7B and C).

The pulse produced by this circuit at the collector of T_3 has a magnitude of 0 to $(-Vcc)$, i.e. transistor T_3 acts also as a pulse amplifier, which is another advantage gained by the gating arrangement.

Fig. (8.7B) shows an illustration for the collector voltages of T_3 and T_4 under three different conditions. For case (a) where inputs (2) and (3) are in antiphase T_3 is conducting and T_4 is cut-off and for the inphase case (b), T_3 and T_4 follow the same square-waves in antiphase and in phase, respectively.

8.5. The Tripping Relay Circuit

The tripping relay circuit consists of a single stage transistor amplifier T_4 shown in Fig. (8.7A).

The output pulses from the phase comparator are fed to the base of the transistor amplifier T_4 through R_5. The collector of T_4 follows impulses of opposite polarity to those of the comparator output, i.e. current pulses which flow through the relay coils have a duration "Q" as shown in Fig. (7.8 B). A shunting condenser C_5, added across R_5, helps to speed switching of T_4. The resistance R_{10} is added to minimise temperature variation effects

as well as to assist in turning T_4 to cut-off, during the elapsing time of the negative pulse given to its base.

The tripping stage consists of a telephone type relay driven by the amplifier T_4. In order to obtain a minimum overall operating time of the scheme, this telephone relay must be driven at several times its pick up and should have a low inductance ratio circuit.

It would be more suitable for field applications if special power supply different from those of the relaying circuits would be used for the tripping amplifier. Comparatively higher voltage power supply and higher voltage rated transistors can then be used. This power can be supplied from a special station batteries divider.

However, in the scheme developed, the telephone relay used is derived from the same power supply as the relaying circuits. The relay tripping current appears as a train of pulses 360° apart, as explained in the previous section. In the case (b), Fig. (8.7B), where the two inputs (2) and (3) of the comparator are in phase the relay current is in the form of a square-wave, or the duration of the relay current pulse is maximum, i.e. 180°.

The direction of the diode D_4, across the relay coils, is such that current can flow to prevent only the decay of the flux in the relay core, the rise of the flux being unimpeded. This (slugging) diode has the advantage of perpetuating the relay coil current during the dead period or the dead half-cycles in the inphase case.

A variable resistance R_{st} is connected in series with relay coils to provide a control of the minimum relay current pulse width to which the relay responds, i.e. its sensitivity.

For a given power supply voltage, assuming $R_{st} = 0$, the minimum pulse-width (angle) to which the relay responds can be found from the relay pick-up VA and its coil inductance/ resistance ratio. The introduction of sensitivity control R_{st} would increase this minimum angle since the relay operates on the average VA value (inegrated) over the whole cycle. The diode D_4 tends to increase this average by keeping the relay current flowing during the whole or part of the period when transistor T_4 is cut-off. For the scheme developed, and with 10V power supply, a minimum sensitivity angle of about 35° was obtainable by connecting in parallel the two available windings on the relay core.

Since the relay tripping current appears as a train of pulses 360° apart, therefore the rate of tripping of this auxiliary relay is variable according to the instant of appearance of the fault but it will always be less than one cycle from the appearance of the first relay current pulse.

8.6. Phase Shifting Circuit

The function of the phase shifting circuit is to produce an output wave shape lagging behind the input to the circuit (or delayed) by a certain angle corresponding to the phase shift

over the pilot circuit. Fig. (2.1) shows that the input to this circuit is provided from the squaring circuit. In fact, many alternative arrangements can produce the same result, i.e. a lagging signal to the local end one. This was first tried by amplifying the A.C. signal obtained from the output of the segregating networks, and then phase shifting this A.C. signal by conventional phase shifting networks. Two circuits were developed for this purpose.

The first is of the bridge type, shown in Fig. (8.8A). In this bridge circuit arrangement, R_1 was made equal to $R_2 = R$, say, and C_1 has a fixed value. The only variable element in the circuit is R_3. R_3 was made variable over the range $0 - 2R$, in order to obtain a wide range of phase shifts. With a fixed value of C_1 to give an impedance at 50 c/s of about $0.6R$, the phase shift is adjustable over a range about 110°, with no significant change in the amplitude of the output.

Phase shifts over 90° are not likely to occur with pilot circuits, used for protective purposes, for a length between 25 - 40 miles.

However, this circuit, like most phase shifting devices, uses a reactive component C_1. Consequently, the phase of the output voltage from the network will depend on the frequency of the system, i.e. the circuit is frequency sensitive.

Other circuits can be also used, using inductive or capacitive elements in conjunction with resistive branches.
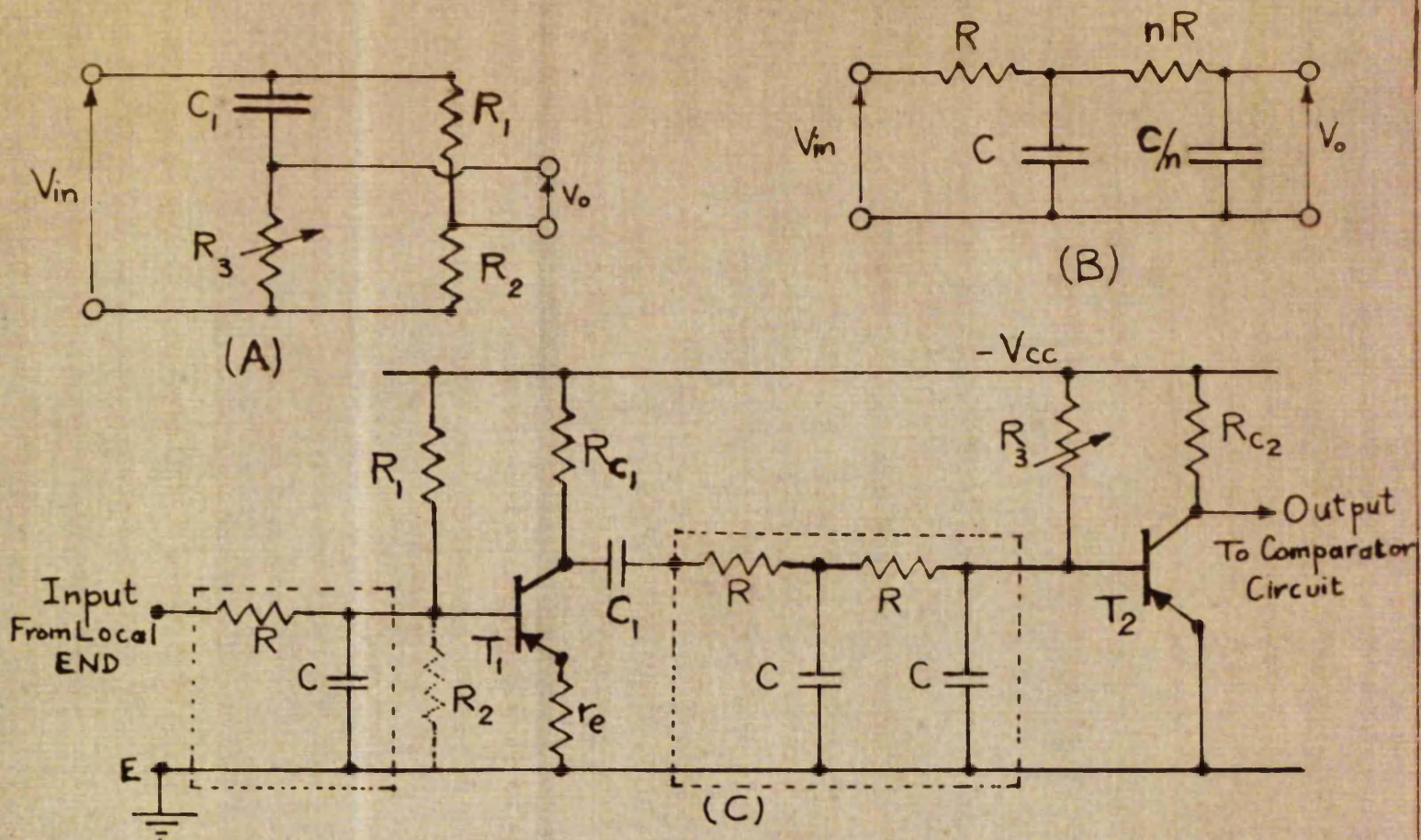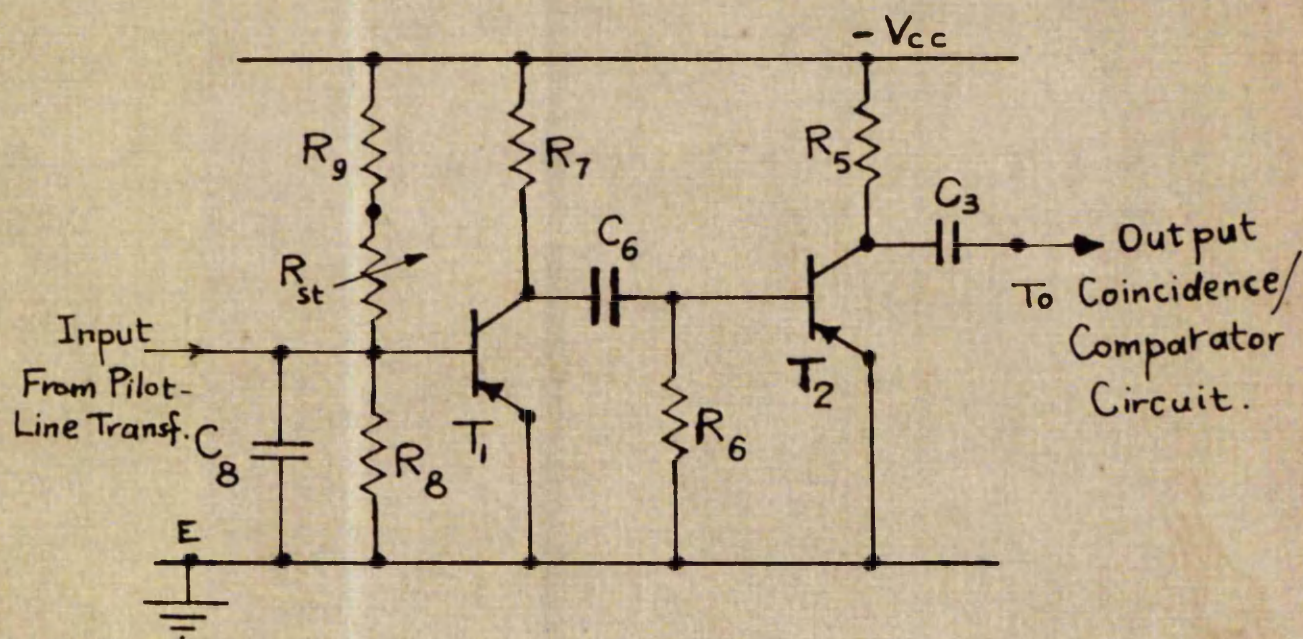
Fig. (8.8)   PHASE SHIFTING CIRCUITS

Fig. (8.9)   RECEIVING/RESHAPING CIRCUIT

However, inductances are generally large and expensive and a resistive/capacitive circuit may prove better and cheaper.

Another circuit of the type described in Chapter 6, sec. (6.3), was designed to produce a voltage output which can be arranged to reach quadrature with its input voltage. This circuit is shown in Fig. (8.8B), where n is a scalar factor $\gg 1$.

It can be proved that the input voltage Vin is related to the output by:-

$$V_{in} = V_0 \left[1 + j\omega CR \left(\frac{2n+1}{n}\right) - \omega^2 C^2 R^2 \right] \quad \ldots\ldots \text{(8.12)}$$

For the case when n = 1, therefore

$$V_{in} = V_0 \left[1 + 3j\omega CR - (\omega CR)^2 \right] \quad \ldots\ldots \text{(8.13)}$$

Taking for example the case of a 90° phase shift, the relationship between R and C would be $\omega CR = 1$, substituting this in eqn (8.13) it follows:-

$$V_{in} = j \, 3V_0 \quad \ldots\ldots \text{(8.14)}$$

Such a type of circuit has been analysed in some detail in sec. (6.3), and for the general case of n > 1 and $\omega CR = 1$, eqn. (8.12) gives:-

$$V_{in} = jV_0 \left(\frac{2n+1}{n}\right) \quad \ldots\ldots \text{(8.15)}$$

Eqn (8.15) shows that the output Vo is lagging behind Vin by 90° and the variation in the value of n affects the magnitude

only. The magnitude varies from $\frac{V_{in}}{3}$ at n = 1 and tends to $\frac{V_{in}}{2}$ as n tends to ∞.

For a fixed value of C and C/n in Fig. (8.8B), a variable twin (concentric) potentiometer operated by the same spindle provides a wide range of values of ωCR ranging from equal to one for a 90° phase shift to $\omega CR' = \sqrt{3}$ for a 60° shift. Since "ωC" is a constant then a gradual change in the value of resistance from R to R' would produce the required shift over the whole range.

As mentioned before, both circuits of Fig. (8.A and B) are frequency sensitive and in the particular application with the developed scheme the input sine wave shape from the segregating was affected by the squaring circuit input impedance, since both are in parallel. The forward resistance of the emitter/base junction in the squaring-circuit affects the positive half-cycle of the input voltage wave. Moreover, since these phase shifting circuits introduce attenuation, amplification was therefore necessary before and after them.

In designing these circuits attention should also be given to the value of the input impedance of the amplifier following the phase shifting circuit. This impedance should be quite high compared to the series branch nR in Fig. (8.8B). If this is not the case, the phase-shift achieved by the network will be less than the simple calculated values given by eqn (8.12).

All these factors present difficulties in using a sinusoidal wave input to the phase shifting circuit.

The alternative of using the local square-wave signal presents a better solution to overcome most of these problems. Moreover, this arrangement is favoured because of the fact that the phase shift produced by the shifting circuit has to be equal to the shift that the remote end square-wave has undergone over the pilot-circuit. Consequently, a phase shifting (delay) circuit for the local square wave has been adopted. This delay was obtained on two stages using RC networks. Each stage is followed by a transistor amplifier of the common emitter type. The total required phase shift is shared between the two stages. The RC circuit used is of the type described in sec. (6.3). These circuits cause attenuation as well as delay to the input wave. The attenuation is compensated for by using high gain saturated amplifiers. In order to produce a signal of the same polarity as the input, an amplifier followed by an invertor or two amplifiers in cascade would be necessary. Advantage was taken of using two amplifiers to produce the total phase shift also in two steps.

Referring to Fig. (8.8C) and assuming a step function to be applied to the input of the RC circuit, a delayed (phase shifted) output is obtained from the collector of T_2.

Assuming that the base of T_1 has a biasing voltage V_b and is about to conduct then:-

$$V_b = \frac{V_{cc}\, R_2}{R_1 + R_2} \qquad \qquad \ldots\ldots (8.16)$$

where R_2 is an equivalent resistance for the input impedance

234.

of T_1 across the shifter output terminals. When the signal is first applied, capacitor C starts charging through R and the voltage across C is given by:-

$$v_C = V_{cc} (1 - e^{-t/CR}) \qquad \ldots \ldots (8.17)$$

The voltage V_b can be made small compared to V_{cc} and therefore transistor T_1 will switch to conduction at a voltage approx. $= V_b$ which is $\ll V_{cc}$. Eqn. (8.17) can then be approximated to:-

$$v_C \simeq V_{cc} \cdot \frac{t}{CR}$$

T_1 starts to conduct and produce an output when v_C across the capaictor C reaches V_b, therefore it follows that:-

$$\frac{V_{cc} \, t}{CR} = \frac{V_{cc} \, R_2}{(R_1 + R_2)} \qquad \ldots \ldots (8.18)$$

$$\text{or} \qquad t = CR \cdot \frac{R_2}{R_1 + R_2} \qquad \ldots \ldots (8.19)$$

The values of the resistances R_1, R_2, and R should be chosen so that the capacitor C would charge through R and discharge through (R_1 and R_2) in parallel, in less than half the period of the square wave input to the RC shifting network. The output of T_1 would then follow the input, and the angle of delay between them will be:-

$$\theta_1^o = \frac{2\pi t}{T} \qquad \ldots \ldots (8.20)$$

where T is the period of the square wave input.

This first amplifier was coupled to an RC composite network, made of two sections in tandem. The output of this circuit is applied in turn to an amplifying stage T_2 similar to T_1.

The signal amplitude, after attenuation in the delaying circuit, is enough to drive T_2 between saturation and cut-off. The biasing resistance R_3 is made adjustable to provide a control over the "M/S" ratio of the square-wave output of T_2.

This arrangement produces a delayed square-wave, with steep edged output delayed, behind its input by Θ_1.

For practical purposes, the change of the delay angle Θ_1^0 is achieved by varying the RC components of the shifter circuit. This provides satisfactory shift for practical pilot circuit lengths within 40 miles.

However, another circuit was investigated for providing a variable square-wave output delay from $(+ \frac{\pi}{2}$ to $- \frac{\pi}{2})$, in order to cover greater pilot lengths, and its output can be calibrated in degrees. The main parts of this circuit and their functions are described in sec. (2.5.5.).

This last mentioned circuit has a complicated design nature and no successful design was obtained using one rail power supply. The monostable and the integrating circuits require at least two power supply rails (negative and positive) as well as a zero rail to provide satisfactory performance. The monostable circuit is not immune from pick-up due to switching operations in its vicinity, and care should be taken for shielding it properly, if

maloperation has to be avoided.

However, although such an arrangement gave reasonable
satisfactory performance, it is considered complicated and
uneconomical compared with the RC shifting circuit of Fig. (8.8C).
This complex circuit causes an error in the mark/space ratio as a
result of any departure in the power system frequency, as well as
variations in power supplies and temperature.

Errors due to temperature and power supply variations
may be partially compensated for, but at the expense of introducing
further complexity in the circuit. The departure of the frequency
of the power system from 50 c/s causes the duration of half a
cycle to be different from 10 m.s. which is the overall time delay
of the monostable. This produces an error in the "M/S" of the
output wave. It is difficult to avoid such errors, but with the
frequency variations likely to occur on the British grid they do
not exceed $\pm 4\%$.

8.7. <u>Receiving/Reshaping Circuit</u>

The function of this circuit, as described in sec. (2.5.6)
is to recover the remote end square-wave transmitted over the
pilot circuit. In other words, the circuit compensates for the
attenuation which the signal has suffered over the pilot circuit.

The circuit shown in Fig. (8.9) comprises two amplifiers, for
receiving/reshaping, of the high gain common emitter configuration.

The input to the first amplifier is fed from the differential bridge circuit, sec. (8.8). This stage is used for amplifying the received signal and eliminating any spikes or sporadic pulses coming through the pilot circuit. The value of the condenser C_8, Fig. (8.9), is made just large enough to eliminate these undesirable pulses. The biasing potential divider $R_8/(R_g + R_{8t})$, provides a very small bias V_b at the base of T_1 and R_8 is made very small to allow a very short discharge time for C_8. This controllable bias feature is to produce an output at the collector of a unity "M/S" ratio. This output is coupled to the second reshaping high gain amplifier T_2. This amplifier restores to the received signal its steep fronts and produce a square-wave output before applying it to the coincidence circuit.

Two cascaded amplifiers (or an amplifier/invertor arrangement) are necessary to produce a wave having the same polarity (phase) as the received signal.

8.8. Differential Bridge Circuit

The function of this circuit is stated in sec. (2.5.3.). Briefly the circuit arrangement directs the local end square-wave towards the pilot-circuit and avoids its return with the received signal which is also guided by the differential bridge to receiving/reshaping circuit.

Fig. (8.10A) illustrates the final arrangement adopted for the bridge differential circuit. It consists of transistors T_1 and

(A) Differential Bridge Arrangement

To Receiving
Circuit

(B) Push-Pull Driving Circuit
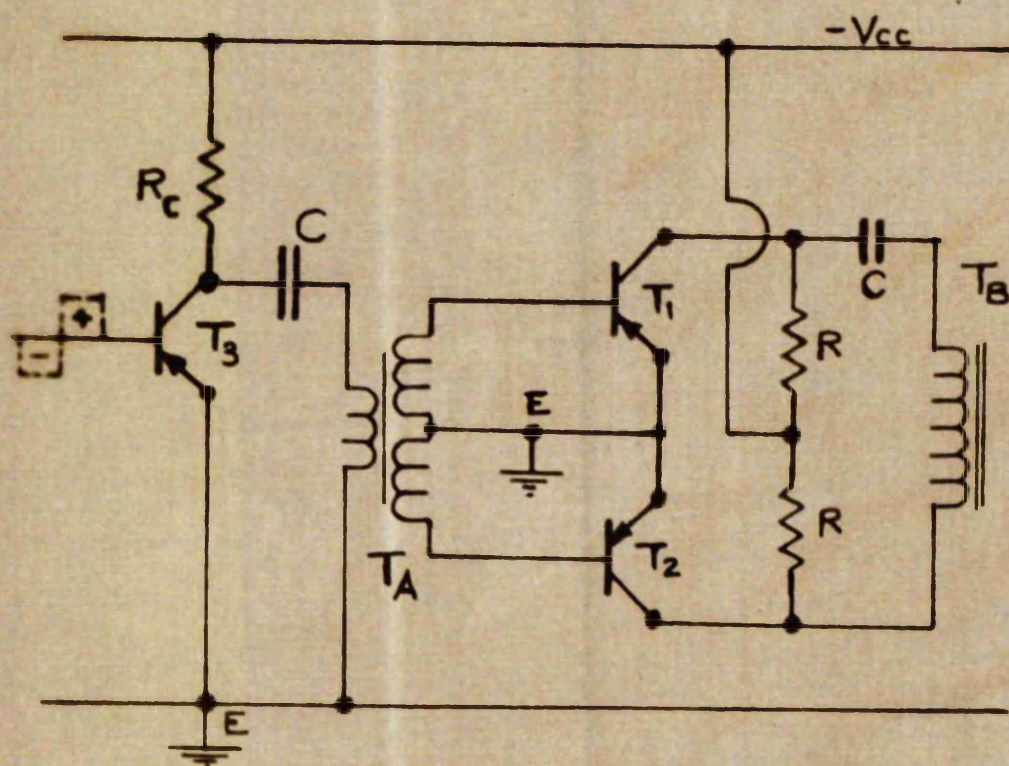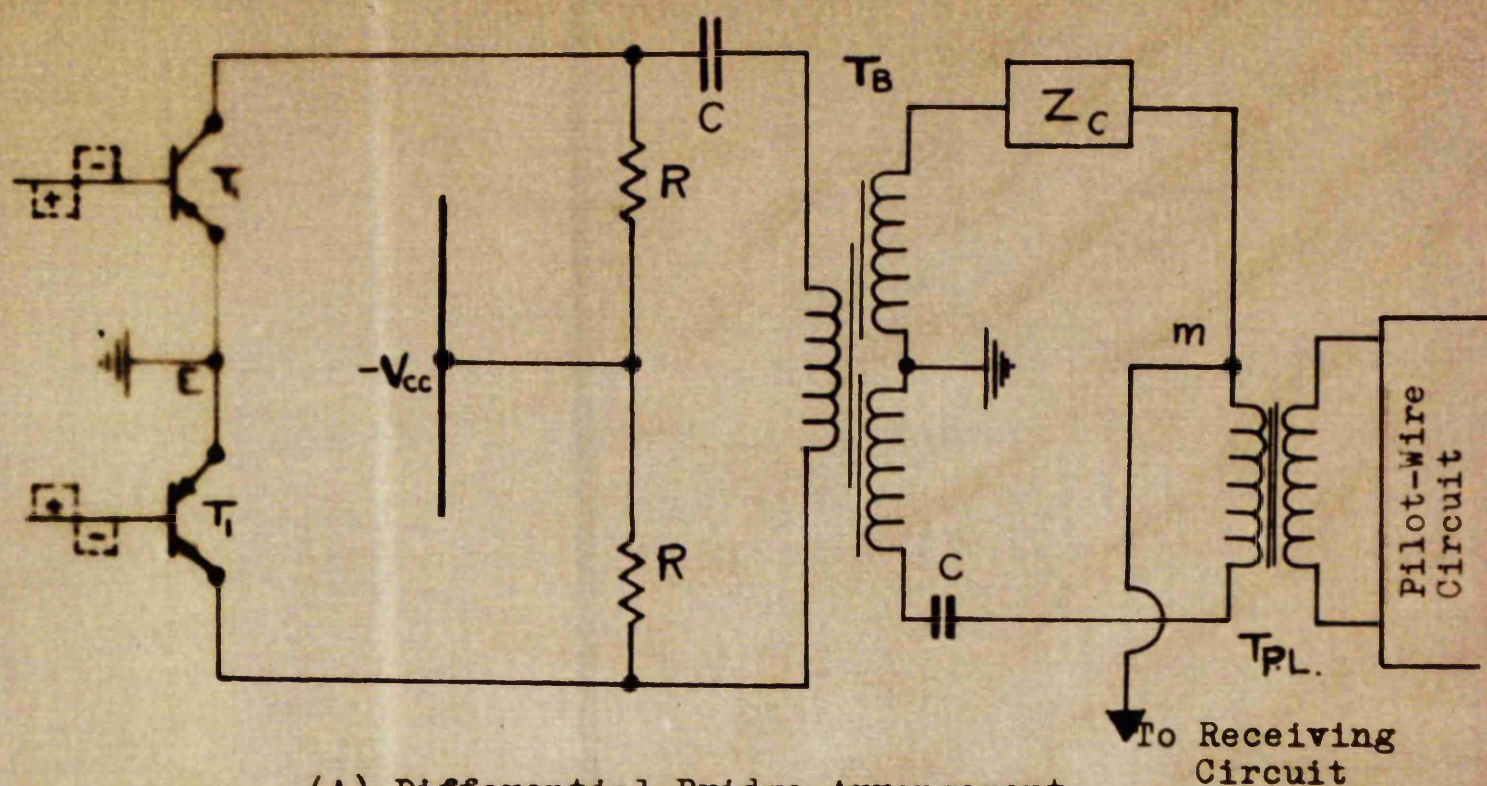
T_B	Bridge Output Transformer
T_A	Pulse Transf.
Z_c	Balancing Impedance
C	D.C. Blocking Condenser
$T_{P.L.}$	Pilot Isolating Transf.

DIFFERENTIAL BRIDGE CIRCUIT

FIG. (8.10)

T_3 in a push-pull arrangement with the bridge transformer T_B.

T_1 and T_3 are driven by two square-wave inputs having opposite polarities. The output of the squaring circuit Fig. (8.1), is taken through transistor T_3, Fig. (8.10B), where transformer T_A is connected across its collector and earth. T_A is a pulse transformer with an earthed centre tapped secondary. The two secondary terminals of T_A are in antiphase connected to drive T_1 and T_2 of the push-pull amplifier.

This arrangement was quite satisfactory, but the pulse transformer T_A is considered rather an expensive item. An alternative way of driving the push-pull amplifier has been used by taking two outputs from an emitter follower at the output stage of the squaring circuit. One of these outputs is applied directly to the base of T_1, Fig. (8.10A), while the other output, after being inverted, is used to drive T_2. The operating points and input signals of the two transistors T_1 and T_2, Fig. (8.10A), are made as similar as possible. Both transistors have equal load R in their collector circuits, this is rather an important part in the design of the differential bridge.

The push-pull stage has the advantage of doubling the swing to twice that of the collector of T_1 or T_2. Each of these transistors has a swing approx. equal to $\pm V_{cc}/2$. The voltage swing across the primary of T_B is therefore, almost equal to V_{cc}. By the appropriate choice of the transformation ratio of T_B the voltage applied to the pilot circuit can then be determined. If a higher

voltage, than that determined by the relaying circuit power supply (Vcc), is desired a separate power supply can be used for the push-pull amplifier. T_B is designed as a pulse transformer to produce faithfully a wave on its secondary circuit of the same shape as that impressed on the primary winding.

Two square-wave outputs, of opposite polarities are obtained from the bridge transformer. One of these square wave outputs is applied to the pilot circuit through a pilot-line isolating transformer $T_{P.L.}$ and the other to a balancing impedance Z_C. The transformer $T_{P.L.}$ is also designed as a pulse transformer and has a unity transformation ratio.

The value of the load R in the collector circuits of T_1 and T_2 of the push-pull stage, determines the shape of the wave applied to the pilot-circuit. These resistances R combine with the apparent resistance and capacitance of the pilot equivalent circuit to form a circuit having a time constant which determines the departure of the wave from a square one.

In practice, the combined circuit of the load R with the pilot circuit will generally be almost that of an RC, even if the pilot is loaded. This time constant defines, in effect, the deforming action of the square-wave. If the collector load resistances R are made small enough, the effect of different pilot circuits would be limited almost to the value of R in the push-pull stage, since R effectively shunts the apparent pilot-resistance.

The balancing impedance Z_C, has to be made equal to the

apparent impedance of the pilot-circuit as seen from the secondary of the bridge transformer T_B. As in many other pilot-wire schemes, the best form for this impedance to balance the pilot-circuit is found to be a series combination of a resistance and a condenser even for loaded circuits. A variable resistor having a max. value of 2500 ohms and a tapped condenser of 11.0 μF adjustable in steps of 0.1 up to 1.0 μF and in steps of 1.0 μF up to 10.0 μF, are adequate to cover most practical pilot circuits for a length up to 40 miles.

8.8.1. Pilot Voltage Wave Shape

It has been mentioned in the previous section that the value of the load resistance R, Fig. (8.10) determines, to a great extent, the shape of the wave to be impressed on the pilot-circuit.

Fig. (8.11) illustrates some of the pilot-circuit voltage wave shapes, under different fault conditions as well as over different complex pilot circuits.

For the external fault case, shown in Fig. (8.11), the pilot-circuit was built up of artificial lines to simulate 45 miles of a 20 lb/mile cable. This is composed of 20 miles of load line and 25 miles of an unloaded cable. The constants of these artificial lines are given in Tables (7.1) (a) and (7.2) (d) and (e), respectively.

The two upper traces (A), represent the local and remote end square-waves, while the (B) traces show the wave shape over the

FIG. (8.11) PILOT VOLTAGE WAVE FORMS.

(A)   End (1) and End (2) Square-Waves.

(B)   Pilot Line Wave Shapes at End
      (1) and End (2).

(C)   Same as (B) on Extended Time Base.

(D)   Local Ends Pilot Voltage and
      Received Signals.

(E)   Pilot Voltage Wave Form on First
      Switching Operation.
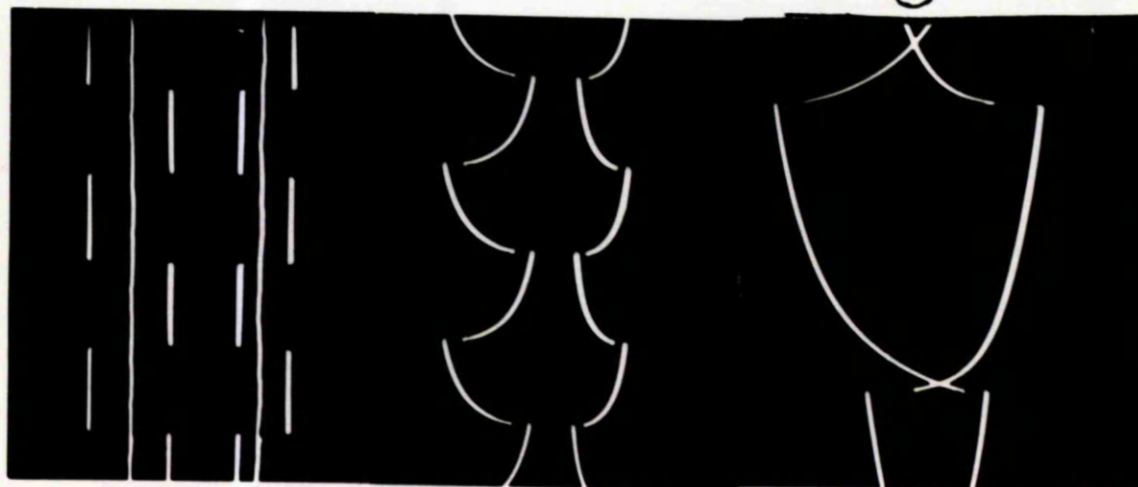
EXT. FAULT INT. FAULT

A

B

C

D

E

FIG. 8. II.
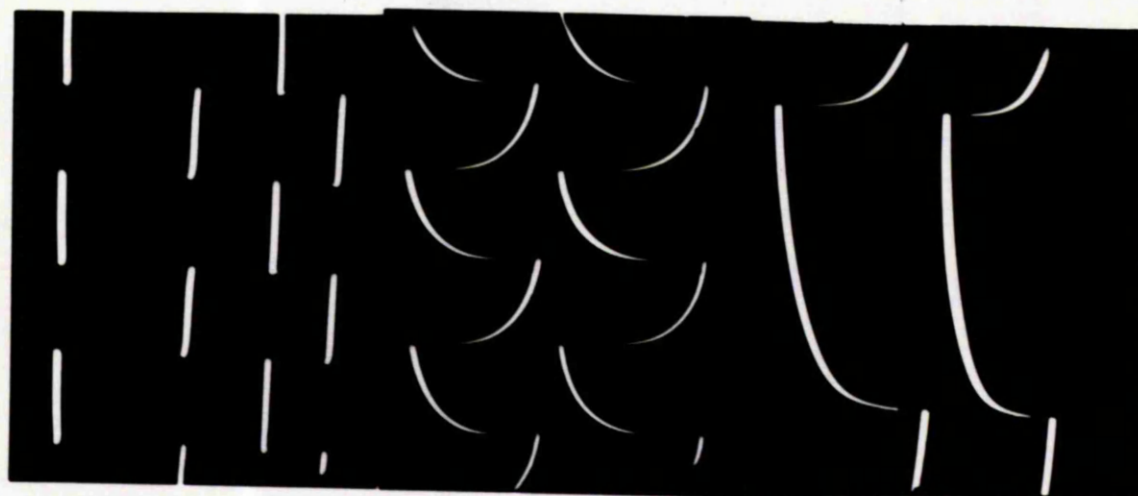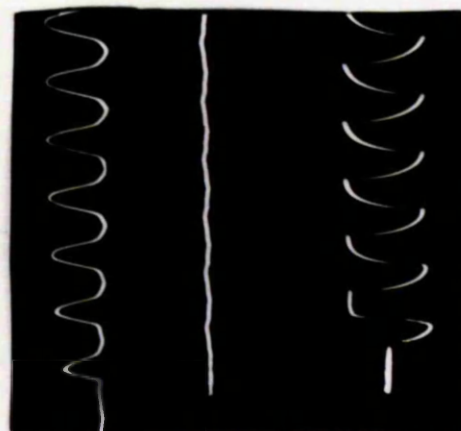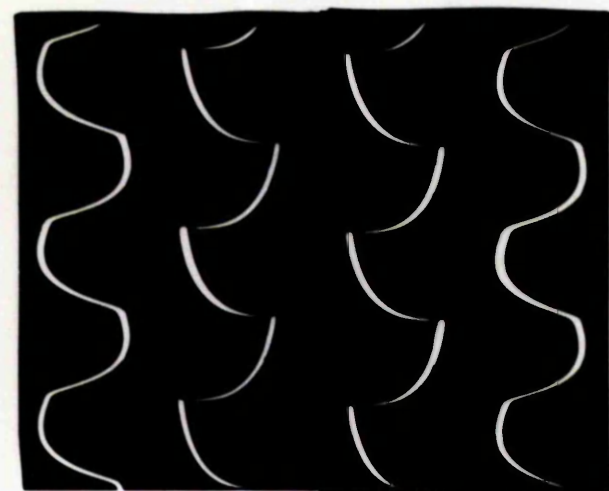
pilot circuit. Traces (C) are the same as those of (B) but for an extended time base.

In the case of an internal fault, shown in Fig. (8.11), the pilot-circuit was composed of a 25 miles of unloaded line, Table (7.1)(a).

Comparing the traces (C) shown in internal and external faults, it can be easily seen that the effect of different pilot-circuits would result in different wave shapes impressed on the pilot-circuit. The departure of the wave shape from being square, i.e. the time constant, depends on the nature of the pilot circuit. However, it is clear that this time constant increases as the pilot length increases. It has also been noticed that loaded pilot circuits would generally tend to give a little larger time constant than unloaded ones.

The middle two traces of Fig. (8.11D) show the pilot voltage wave shapes at the local and remote ends of the protected section, (in enlarged scale). The upper and lower traces of Fig. (8.11D) show the received waves over a 45 miles pilot-circuit. This circuit comprises 25 miles of unloaded 20 lb/mile plus 20 miles of 40 lb/mile cables. The constants of these lines are given in Table (7.1) (a) and (c).

The slight difference in the magnitude of the two received waves, can be noticed, due to the disymmetry of the pilot-circuit.

Fig. (8.11E) shows the pilot voltage wave shape under single infeed (bottom trace), while the upper trace shows the input to

the zero-sequence starting circuit, only as reference. The case represented here is a simulated single phase to earth fault.

However, it can be noticed that the pilot voltage follows its normal pattern after the first one and a half-cycle.

This was traced to be due to capacitive coupling effects between some of the stages of the relaying circuit and due to another factor, not associated with scheme, from the supply transformer where a small transient component was included as can be seen from the top trace. The supply to simulate an earth fault was taken through a phase shifting unit which has an output transformer.

However, this effect would not generally be met when the supply is taken from the linear couplers as their output is transient free, sec. (3.5).

It is also noted that the effect of the capacitive coupling between some stages of the relaying circuitry would diminish on subsequent switching operations and even so it has very little effect on the first switching operation only.

When the scheme is operating under normal (healthy) conditions, the relaying circuits are always energised and continuous comparison is carried-out between the line current at the two ends. Tripping is then controlled by the starting element, as explained in Chapter 2 and sec. (8.2).

The first switching-in operation of the system, under healthy conditions, will, therefore, not cause maloperation since the starting circuit signal will not be present. Any change in the

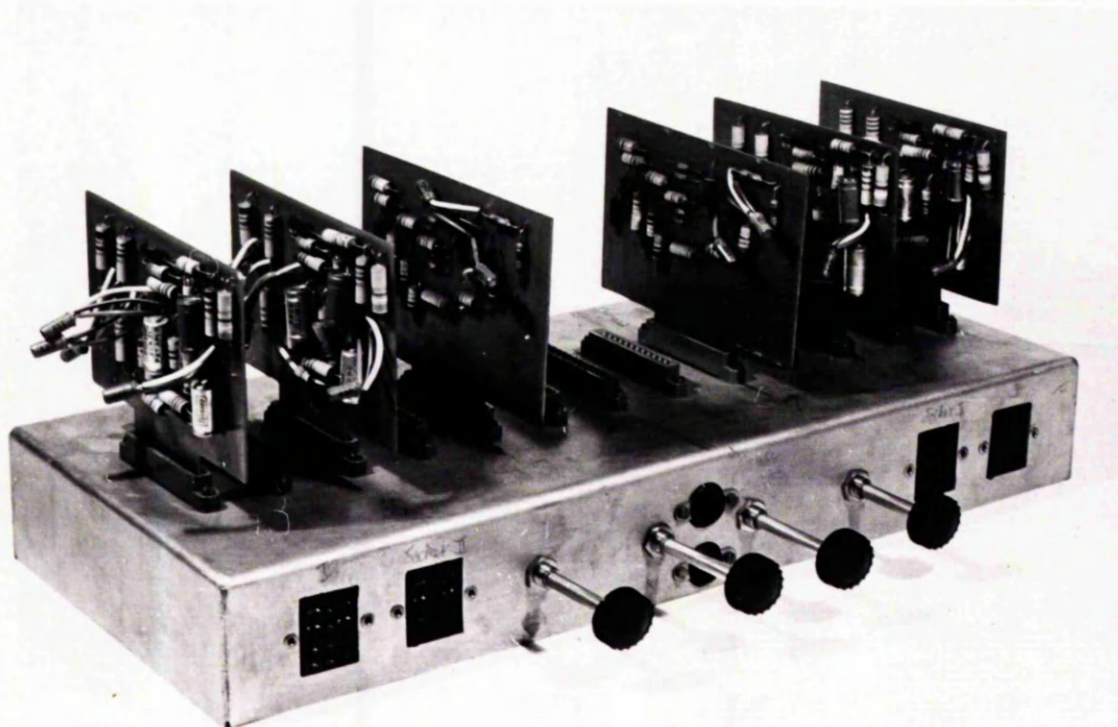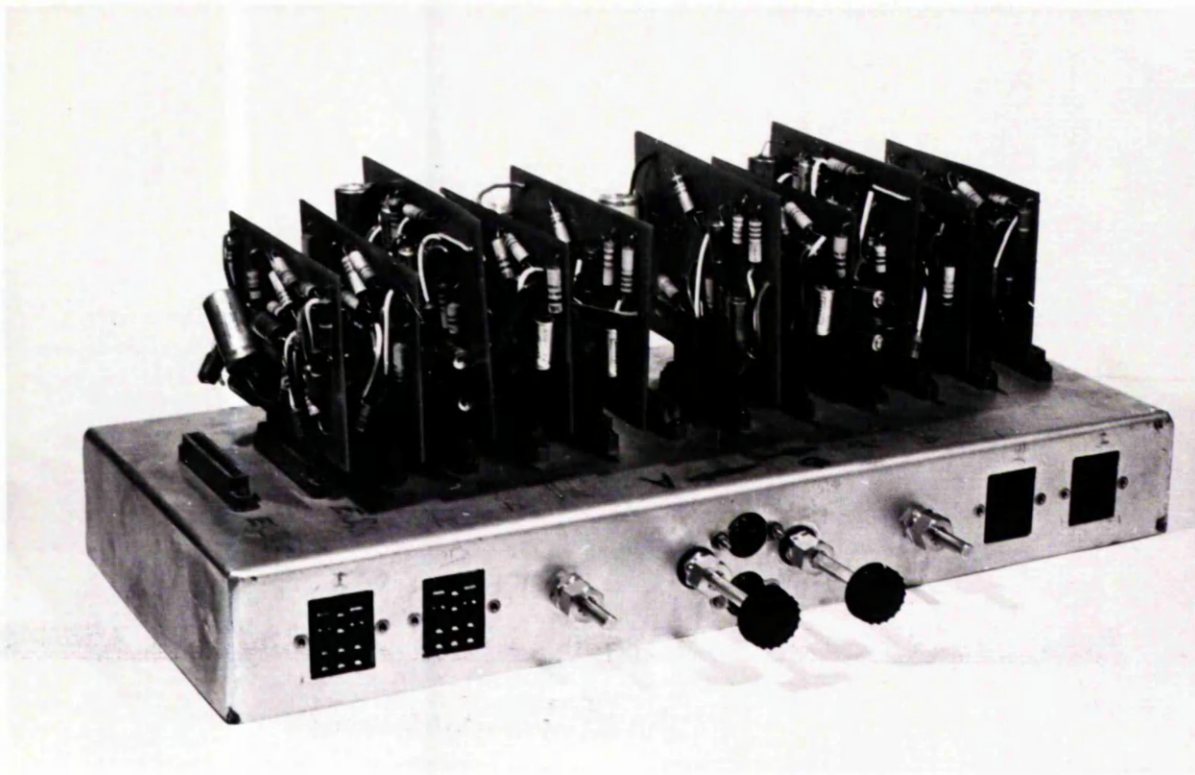FIG. (8.12)   TRANSISTORISED RELAYING CIRCUITS ASSEMBLY.

(PRINTED CIRCUITS)

FIG. 8.12.

mark/space ratio of the local and remote end square-waves, when switching-in, will therefore cause no hazards.

In cases of switching-in on an internal fault, with single or double infeed, tripping should take place within 2 cycles.

The probability of switching-in a system on an external fault, would be the only possible case where this effect may cause some hazards. However, such a case is always considered of a second order risk and is not worth further complications to be included.

8.9. Mounting and Assembly of Relaying Circuits

In order to simplify the wiring of the relaying circuits to the highest degree, printed circuit techniques, which are most suitable for transistor circuits, have been used. The transistorised circuits of the scheme are sectionalized, according to their respective functions into a number of plug-in printed circuits. This makes every unit readily accessible and facilitates reproduction, if desired, as well as reducing maintenance difficulties.

The whole transitorised relaying circuits, for the two ends of the protected section, are mounted on two chassis shown in Fig.(8.12).

The interconnections between the chassis, including the artificial lines unit, are made through plug-in cable sockets mounted on the back side. Some points which may be required for monitoring, testing, adjustment, and maintenance purposes have been brought to the front side.

CHAPTER 9

PERFORMANCE AND TESTING OF THE DEVELOPED SCHEME

9.1. Introduction

A complete equipment for the developed comparison scheme was constructed. This was based on the analysis, design, and information given in the previous chapters. The equipment consists mainly of two identical units, one for each end of the protected section, as well as the artificial pilot-line units described in Chapter 7.

The block diagram of the equipment at each end of the line is shown in Fig. (2.1). The functional diagram of the subdivisions of each unit are also given in Chapter 2 and their design details are given in Chapter 8.

Steady-state tests were carried-out step by step on each individual sub-unit during assembly as well as on the complete assembly. In order to determine the speed of response of the scheme and its rate of tripping, timing tests were performed on the whole scheme after completion.

The performance of the scheme has been investigated over different complex pilot circuits, built up from those mentioned in Chapter 7.

9.2. Steady State Tests

The arrangements for the steady state tests were carried out by disconnecting the segregating circuits at end (1) of the protected line and introducing a phase shifting device instead.

It was arranged that this device would produce an output of adjustable magnitude and phase angle. The output was applied in turn to the starting circuits as well as to the squaring circuits. In order to simulate design conditions as near as possible the output impedance of the phase shifting device was made equal to that of the segregating networks.

A single phase to earth fault was then applied to the segregating networks, at end (2) of the protected section. The relaying quantity "I_m" applied to the squaring circuit of this end equipment was chosen to have a variable $\alpha = (M/N)$, as given in eqns (5.1). The range over which "α" can be varied is from 2 to about 6.

The fault considered is a phase "A"/earth fault, since this phase has the lowest setting, eqn (6.114).

The magnitude of the relaying signal at end (1) is made variable over the range from minimum setting to about 200 times setting. The phase angle of this quantity can be adjusted to have any desired value w.r.t. to end (2) signal.

Several steady state tests were carried out, and numerous oscillograms were recorded for both internal and external fault

246.

conditions. A representative selection is shown in Fig. (9.1)

for the behaviour of the scheme under such steady state conditions.

   (a)   External Fault

        (Healthy conditions, i.e. $\Theta = 0^{\circ}$)

The angle "Θ" is defined as the angle of departure of the

two end signals from the antiphase position.

Oscillograms (A) and (B) give the sinusoidal currents and

the generated square-wave outputs at the two ends of the protected

section. Traces (C) and (D) illustrate the square-wave inputs

to the coincidence circuits, Fig. (8.7), for the local and remote

end, respectively.

Oscillograms (E), Fig. (9.1), show the pulses to the

auxiliary tripping relay at the two ends of the protected section.

It can be noticed that the relays current pulses are of a very

small duration indeed and are 360° apart. Ideally, there should

be zero current flowing under such conditions. These tiny

pulses (spike like) are due to accumulated errors in the mark/space

ratio of the square waves arising from the different relaying

circuitry. They are mainly attributed to the receiving/reshaping

circuit as well as the phase shifting circuits, Figs (8.8 and

8.9), which may have small deviations from unity in the "M/S" ratio

of their square-wave outputs. However, there may also be some

error attributed to the square wave generating circuits,

sec. (8.2). Slight incorrect adjustment in the balancing

FIG. (9.1) STEADY STATE PERFORMANCE OF THE SCHEME.

(A) Local and Remote End Currents.

(B) Local and Remote End Square-Wave.

(C) and (D) Inputs to Coincidence Circuits
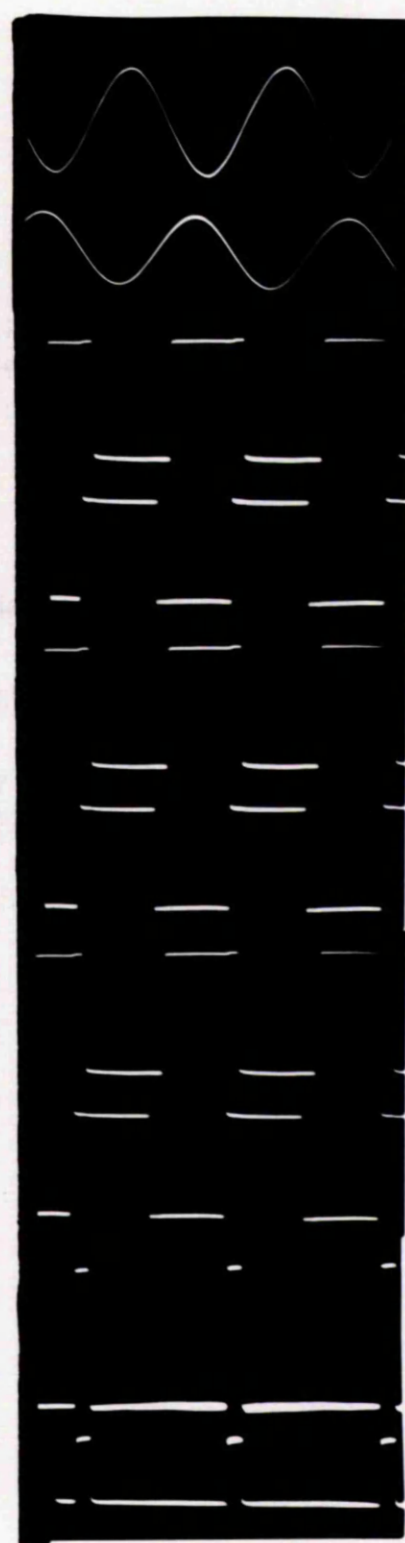   for Both Ends.

(E) Pulses to Tripping Relays.
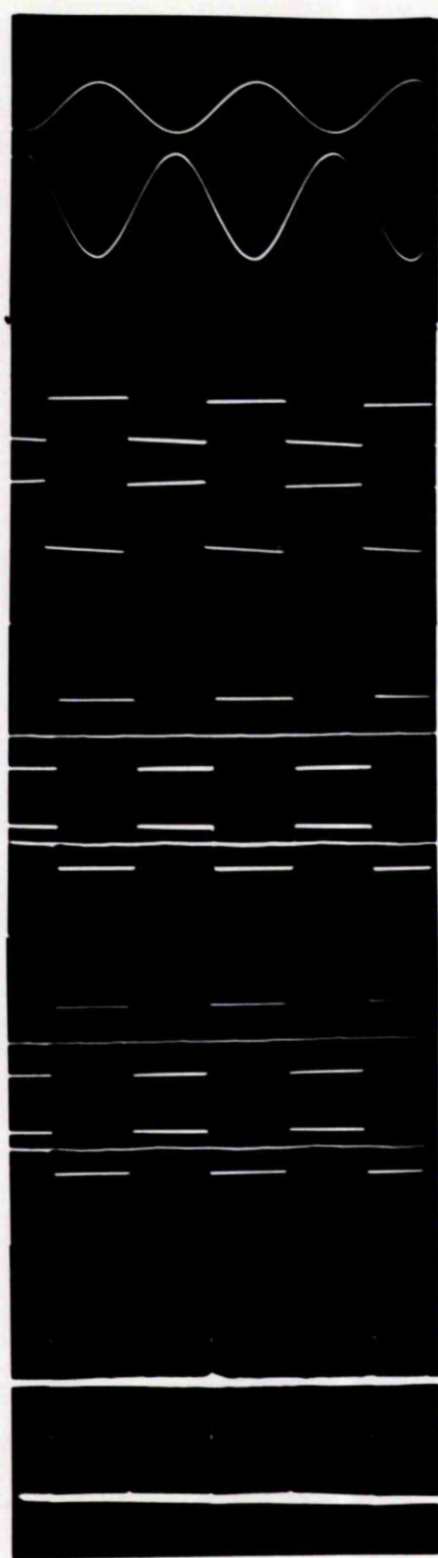
$\Theta = 0°$ $\Theta = 180°$ $\Theta = 40°$
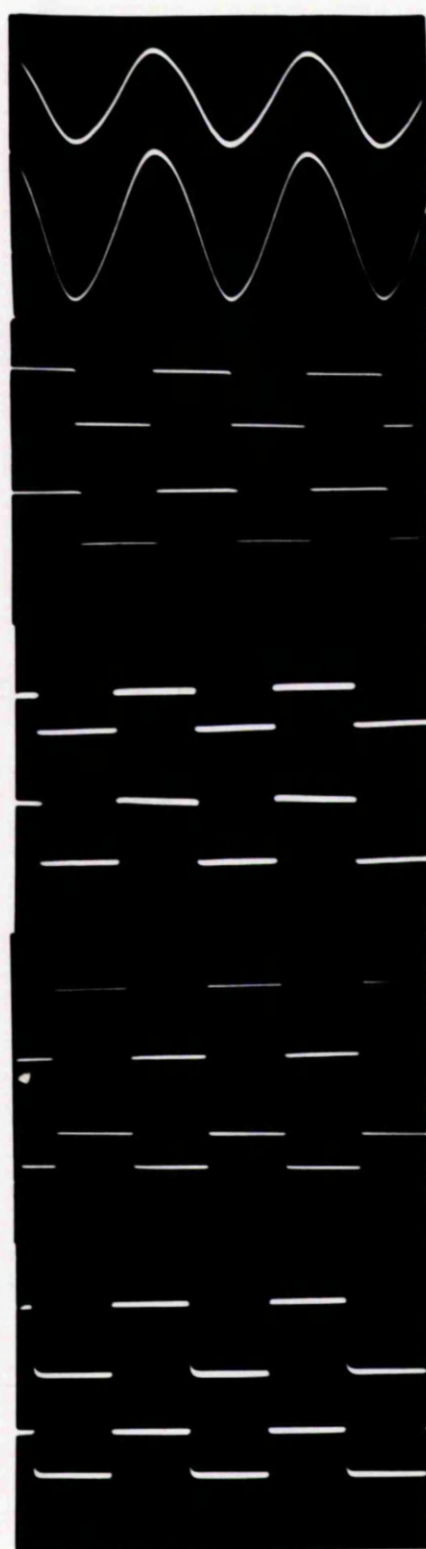
FIG. 9.1.

impedances Z_c of Fig. (8.10) may also contribute to the error.

However, all these accumulated errors in the mark/space
ratio, of the various square-waves, do not exceed 5%. The
maximum pulse width, resulting from the errors, given to the
tripping relay is about 8°.

(b) Internal Fault

"Θ" = 180° in Fig. (9.1)

This case represents an internal fault with double fault
current infeed from both ends of the protected line.

The oscillograms (A), (B), (C) and (D) show, as in the
previous case, the end currents, the local and remote end
square-waves, and the inputs to the coincidence circuits,
respectively.

Traces (E) illustrate the shape of the pulses given to the
two auxiliary relays at the two ends. It can be seen that
these pulses are in the form of a square-wave of unity mark/space
ratio and following the inputs (C) and (D) but having an opposite
polarity (antiphase).

(c) Internal Fault,

Θ = 40°

The case represented here is that of an internal fault
with the remote end current infeed lagging behind the antiphase
position by 40°.

Comparing the square-wave inputs to the coincidence circuits, traces (C) and (D), in Fig. (9.1), with the pulses to the relays shown in trace (E), it can be seen that a relay pulse occurs when the input waves coincide to be positive. The two tripping pulses, each given to the auxiliary relay at one end, differ slightly in width. This difference is, however, within the tolerance range of the tripping angle, i.e. ± 10%.

All the above tests are carried out over a pilot-circuit of 40 miles which comprises 25 miles of 20 lb/mile and 15 miles of 6.5 lb/mile G.P.O. unloaded cables. The total pilot loop resistance was then about 6000 Ω.

9.2.1. Stability Angle

The above tests and a similar variety of tests have been simulated to determine the stability angle "α" of the scheme.

This angle can best be determined from the polar characteristics of the scheme.

For the case of a single phase to earth fault at end (2) of the line, the relaying current at the end (1) was kept constant over a wide range of values up to about 150 times setting.

The phase angle between the two relaying quantities was then varied to show the locus of the current vector at the local end (1) while the current at end (2) was kept constant at a value of 0.5 mA, i.e. at about 10 times minimum setting.

Fig. (9.4A) shows the phase angle characteristics of the scheme for both leading and lagging angles of end (1) current. Fig. (9.4B) gives the α-plane characteristics of the scheme, i.e. for the complex ratio of $I_{(1)}/I_{(2)}$. Fig. (9.4B) represents the case when $I_{(2)}$ was kept at 0.5 mA. The scheme arrangement as a whole, including the ironless-core C.T.s, is a linear one. With higher currents at end (2) and end (1), the characteristics then do not change a great deal as far as the phase angle is concerned.

From the results shown in Fig. (9.4), it can be seen that the scheme has a minimum stability angle of $\theta = \pm\alpha \simeq 40^{\circ}$.

The accuracy of the performance of the scheme, or the tolerance in the angle "α", can be seen to be within $\pm10\%$ of the minimum value given above.

This angle can be increased, if desired, by adjusting the setting resistor Rst of Fig. (8.7A), which controls the width of the tripping pulse to the auxiliary relay, as explained in sec. (8.5).

9.2.2. Sensitivity

The developed scheme is a phase comparison one, and, therefore, its rate of tripping is independent of the amplitude of the primary signals as long as they are in excess of a certain minimum.

The ironless-core C.T.s incorporated in the scheme have a transfer impedance of 10V/kA primary current. The sequence

segregating networks, Fig. (6.16), which are supplied from these linear couplers produce outputs proportional to the sequence components of the fault current, sec. (6.4.4.).

Under a case of a single phase to earth fault on phase "A", where the three sequence components are equal, the input to the starting circuit (2) is given by $v_o' = 3I_o r_o$, Fig. (6.16). With the particulars of Ro = 3.55 kΩ and ro = 56Ω, the minimum setting for this starting circuit was adjusted at $v_o' \simeq 80$ m.v. (r.m.s.). This corresponds to a primary fault current of about 500 A under such fault conditions. The input amplifier for this circuit, T_1 of Fig. (8.3), was made to be driven into the saturation region for higher fault current levels. This setting is limited by the error signals appearing at the output terminals of the segregating circuits, sec. (6.4.3.), due to harmonics, pick-up and frequency deviations under normal load conditions. If higher sensitivity is desired the ironless-core C.T.s can be designed to have higher transfer impedance or alternatively more than one amplifying stages can be used at the input of the starting circuit, Fig. (8.3).

The minimum input to the squaring circuit v_m, Fig. (6.16), at which the square-wave output is generated corresponds to a primary current setting lower than that of the zero sequence starting circuit. This means that phase comparison signals are transmitted over the pilot-circuit before any comparison can take place at either end of the protected line.

Troubles such as high frequency oscillations have been experienced due to high sensitivity of the receiving circuit, Fig. (8.9), when the scheme operated over long pilot circuits in the order of 7000Ω. With a power supply voltage of only 10 volts for the push-pull amplifier arrangement of the differential bridge circuit, Fig. (8.10), and with a pilot isolating transformer having 1:1 turns ratio, higher pilot circuit resistances than 7000Ω caused large attenuation to the signals and in some cases it was difficult to recover the signal without interference from pick-ups, noise, etc.

For practical field applications, the case may be worsened by higher noise levels. In order to avoid such conditions a separate power supply may be used for the push-pull amplifier of the differential bridge circuit and with the proper choice of the transformers turns ratio, a voltage of the order of 50 volts would be suitable, for most practical applications, to be impressed on the pilot-circuit. Using such a voltage level would make it easier to overcome any noise or pick-up levels even for practical pilot-circuits having a resistance up to 10,000Ω.

It is noticed that a square-wave having a magnitude of 50volts would be well within the limits stipulated by the G.P.O., sec. (7.2), and would eliminate any risks of overvoltages reaching the pilot-circuit, unlike the present conventional schemes in case of failures of the voltage limiting devices at the pilot circuit terminals.

FIG. (9.2) TIMING TESTS INTERNAL FAULT ($\theta = 180^{O}$).

(A)   Input and Output to Starting Circuits
      End (1) and End (2).

(B)   Starting Signal Input End (1) and Pulses
      to Auxiliary Relays End (1) and (2).

(C)   Relay Currents and Tripping Contacts
      Supply at Both Ends.

(D)   Zero-Sequence Starting Input Signals and
      Supply to Tripping Contacts of Auxiliary
      Relays (Both Ends).

FIG. (9.3) TIMING TESTS FOR ($\theta = 40^{O}$).

(A), (B), (C), and (D) as for FIG. (9.2)

(E)   Pulse to Tripping Relays and Relay Contacts
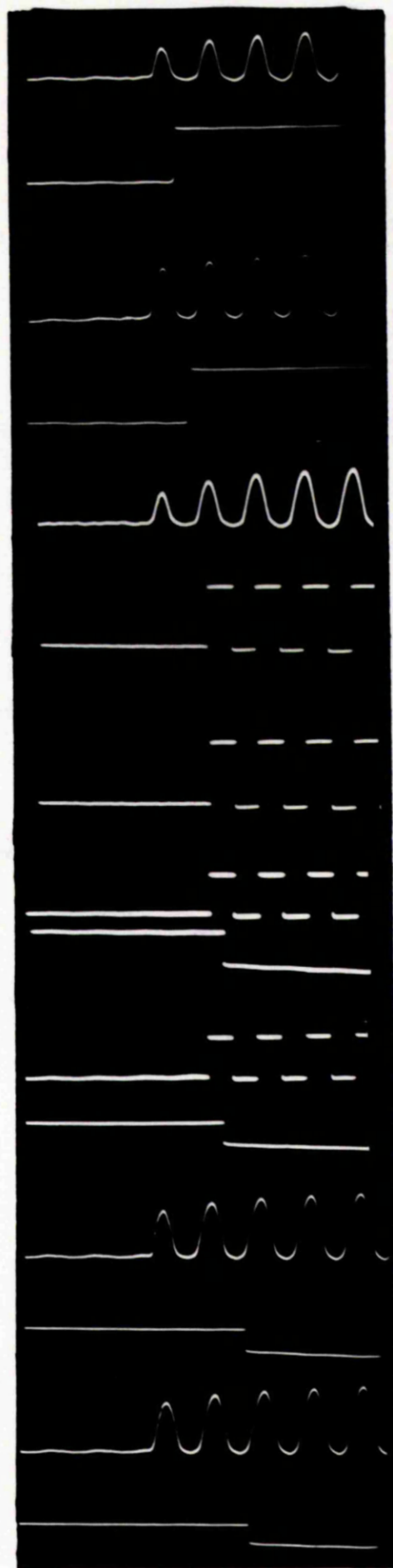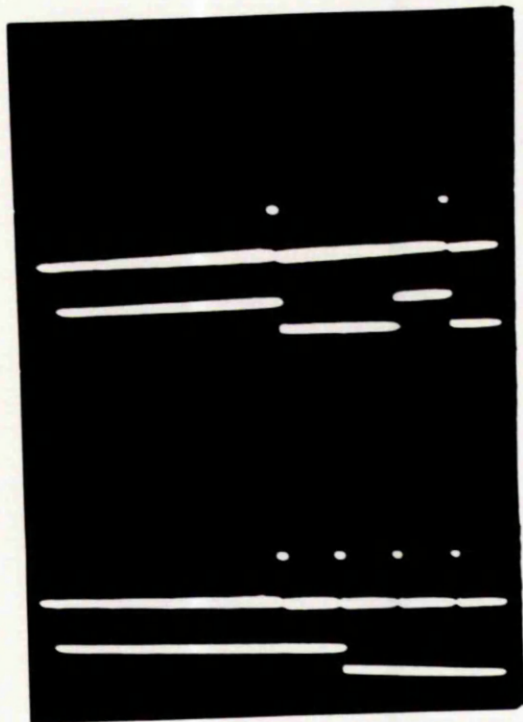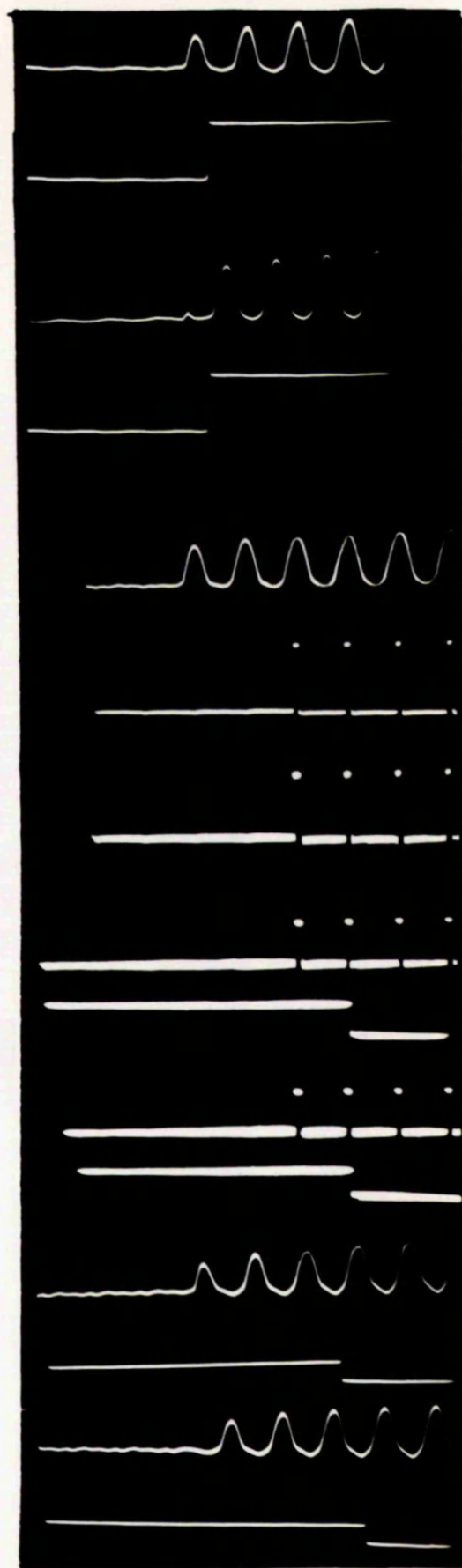   for Ends (1) and (2) under Repetitive Fault.

FIG. 9. 2.

FIG. 9.3.

252.

9.3. Performance and Timing Tests.

Timing tests were carried out on the relaying scheme with different angles between the relaying signals at the two ends of the protected line. These cases simulated internal and external faults. The procedure of these tests can be described briefly as follows:-

The simulated fault case was a single phase to earth fault at each end of the line. The angle between the relaying quantities was adjusted to any desired value, in a manner similar to that described in sec. (9.2). The two relaying quantities as well as the two input signals to zero-sequence starting circuits would then be applied simultaneously to the equipment at both ends of the line. This was carried out through the contacts of a relay incorporated in an electronic unit which also provided a trigger pulse of variable time delay for triggering cathode-ray oscilloscopes. The triggering pulse was adjusted to trigger the oscilloscope a short time before the starting signals were applied.

Since the simulated conditions were of single phase to earth faults, and such conditions are detected by the magnitude of the zero-sequence component of the fault current, these starting signals were used as reference signals in all the timing tests. Under such fault conditions, these starting signals represent also the phase angle of the fault currents.

The performance for different angles "θ" between the two relaying quantities is shown in Fig.s (9.2 and 9.3).

In Fig. (9.2) the angle "Θ", measured from the antiphase position, is 180°. This represents a case of internal fault on the protected feeder.

The four traces (A) in Fig. (9.2), give the starting signal, (the zero sequence current), and the starting circuit step function output voltage for ends (1) and (2), respectively. It is noticed that the two starting circuits, for both ends, operated on the first negative half cycle and the circuit at end (1) gives an output in a period of just over half a cycle while that of end (2), produces an output in about 0.75 of a cycle. Traces (B) give the strating signal for end (1) and the auxiliary relays current at the two ends of the line. It can be seen that both currents start within 1.5 cycles from the moment of incidence of the starting signals. In traces (C), Fig. (9.2), the auxiliary tripping relays current as in (B) are shown together with the tripping supply to their contacts. It is noticed that the contacts of both relays close within the first half cycle from the appearance of the relay tripping pulse.

The last group of traces, (D), show the starting signals /same as first and third traces in (A)_7 and the supply to their tripping contacts. Both ends of the line trips within 40 m.s. from the incidence of the starting signals.

The above tests were performed on a pilot circuit of 25 miles of unloaded 20 lb/mile cable.

254.

Fig. (9.3), (A to D), give exactly the same traces as in
Fig. (9.2), when $Q = 40^\circ$. This represents an internal fault with
the end (2) current leading the antiphase position by 40°.
From (A) it can be seen that the starting circuits at the two ends
of the line picks-up within less than 0.75 of a cycle. From the
three traces shown in (B), it is noticed that the auxiliary
relays current appear as a train of pulses 360° apart. Each pulse
has a width of about 40°. The first relay pulse appears after a
period of almost 2 cycles from the beginning of the starting
signals. Traces (C) show that the auxiliary relays contacts close
at approx. the appearance of the second relay current pulse.
The time taken from the appearance of the relay pulse till contacts
are closed is just over one cycle.

The overall operating time under such conditions can be
known from the traces (D) in Fig. (9.3). This time for end (2)
of the line is about 75 m.s. and approx. 65 m.s. for end (1).

The above test was carried out over a pilot circuit of 40
miles comprising 25 miles of unloaded and 15 miles of loaded
20 lb/mile G.P.O. cable.

The tripping rate of the scheme does, however, vary a little
over different pilot circuits and Fig. (9.5) gives the trend for
the average tripping time of the scheme under different pilot
conditions. The average operating time trends are plotted
against "Q" for cases of leading and lagging angles, as the
difference in operating times between these two cases was quite
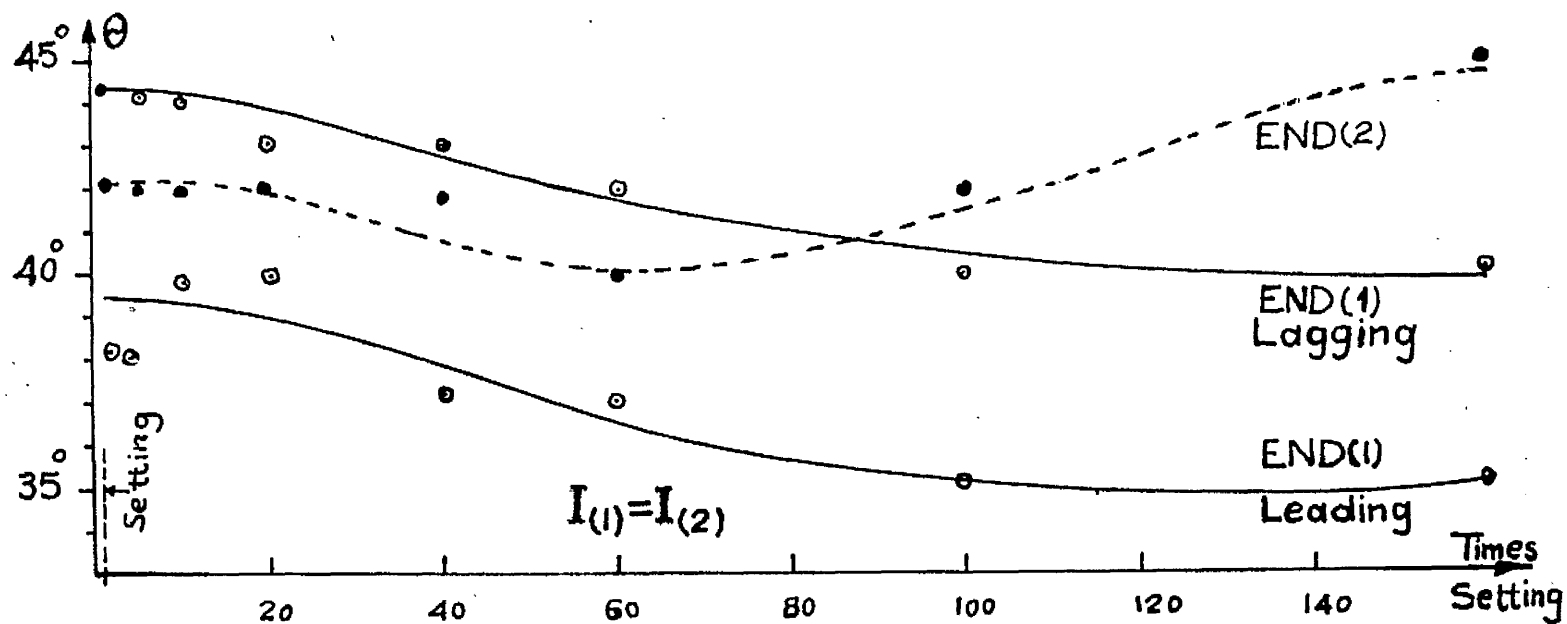
(A) Phase Angle Characteristics
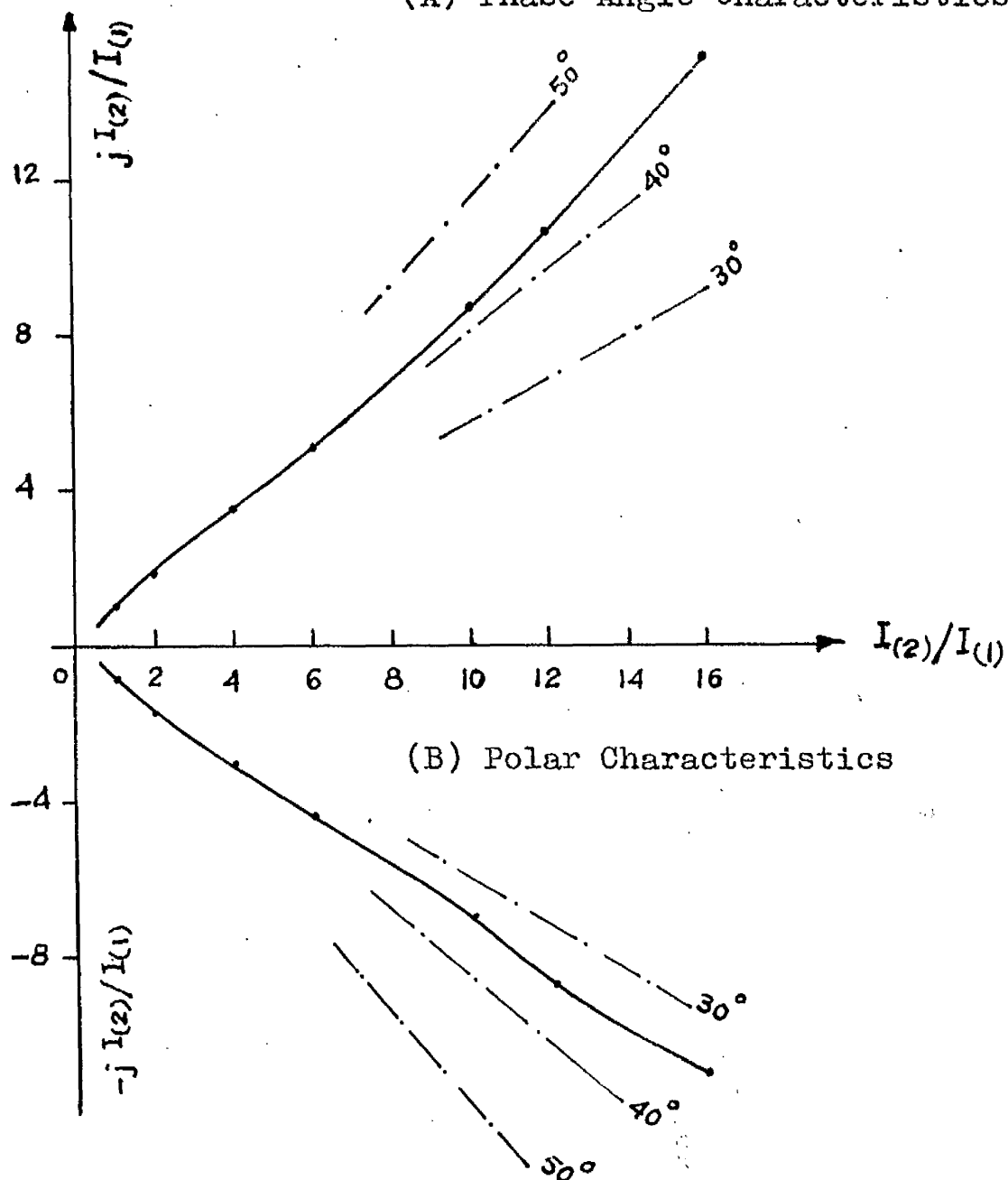
(B) Polar Characteristics

FIG. (9.4)   SCHEME CHARACTERISTICS.

FIG. (9.5) AVERAGE OPERATING TIME OF THE SCHEME.

(1) Loaded Pilot Circuits $>$ 4500 Ω

(2) Unloaded Pilot Circuits $>$ 6000 Ω

(3) Unloaded Pilot Circuits $<$ 4500 Ω

For Pilot Failures
(1) Square Wave from Phase Shifting Circuit
(2) Rectangular Wave

T_D Time Lag Relay
R.S.R. Pilot Supervision Relay
T_R Trip Relay
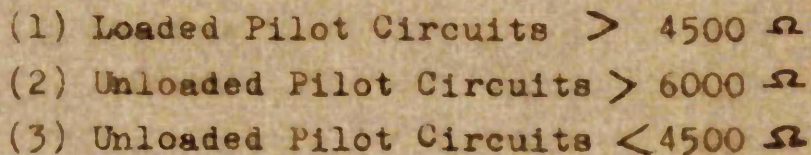
FIG. (9.6) ARRANGEMENT FOR SUPERVISORY ALARM.

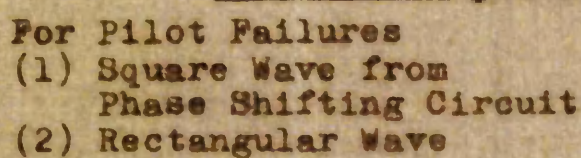small. From Fig. (9.5) it can be seen, however, that the scheme operates within 4 cycles for the most unfavourable conditions. This operating time includes also the auxiliary tripping relay time.

Traces (E) of Fig. (9.3) show a simulated repetitive fault at end (1) of the line. The case represents a fault with an angle $\theta = 40^{\circ}$ between the currents at the two ends of the line. The starting signals were switched on together and then that of end (1) was switched off as soon as the contacts of the relay were closed and reapplied again after a short duration.

It can be seen from the two upper traces in (E) that the contacts of the auxiliary relay at end (1) closed with the appearance of the first relay current pulse and were held closed for approx. 2 cycles, before the relay reset itself.

Meanwhile, the starting signal was reapplied and with the reappearance of the first relay current pulse the relay contacts reclosed.

This test ensures that the scheme is immune from "chattering" risks of the auxiliary relays, once their tripping pulse has reached a predetermined value, as the train of pulses to the relay are 360° apart.

9.4. Effect of Pilot Circuit Failure

It has been mentioned in sec. (1.2.1) that the pilot

supervision equipment is almost incorporated in all present conventional pilot-wire schemes.

Two different arrangements of this supervisory equipment are also shown in Fig. (1.5 A and B). The supervision was carried out by injecting D.C. circulating current around the pilot loop.

In the developed scheme, such an arrangement is neither required nor desirable. The D.C. may interfere with the phase of the relaying signals and may also have some effect on the magnetisation of the pilot isolating transformers.

In the developed scheme arrangement there is a continuous signals received over the pilot link and this can be used as with continuous load supervision schemes. This is preferred to D.C. supervision since it eliminates the inclusion of L.S. and H. set starting features for supervision purposes, as well as the supervising supply equipment itself.

A fault on the pilot circuit, e.g. an open-circuit or a short circuit, would cause unbalance of the differential bridge circuit, Fig. (8.10), with the consequence of a voltage appearing at the point "m" due to the local end signal.

This state of affairs would not cause incorrect tripping since the starting relay signals are not present. Such conditions may cause incorrect tripping only when they coincide with the occurrence of an external fault.

Cases of open-circuit or short-circuit on the pilot link would result, in most cases, in the appearance of a rectangular

wave at the output of the receiving/reshaping circuit, Fig. (8.9).
The case of pilot core reversals would cause no effect on the
scheme performance, unlike conventional differential schemes.

However, advantage can be taken from the appearance, or the
absence, of these rectangular waves at the output of the receiving
circuit to give an alarm feature, if desired, to replace
supervisory equipment.

The arrangement for this suggestion is shown in Fig. (9.6).
Input (1) is a square wave having a unity "M/S" ratio fed from
the output of the phase shifting circuit, Fig. (8.8), while
input (2) is the output of the receiving circuit.

This output under healthy pilot conditions is also a square
wave of unity mark to space, while under pilot failure will be a
rectangular wave or disappear completely as the case may be.

The relay P.S.R. is held closed under healthy system and
pilot conditions due to the input (1) and (2) being in antiphase.
Under system or pilot failures this relay drops and energises the
time lag relay T_D through its normally closed contact P.S.R.

If the fault is due to a pilot failure, the tripping relay
T_R has a normally closed contact in series with the alarm and
once T_D closes it sounds the alarm. In the case of faulty system
conditions, T_R operates before T_D and T.R. contact will be open.
T_D will then operate with no consequences.

9.5. Effects of Temperature and Power Supply Variations

It is well-known that the transistor is a temperature
sensitive device. All the parameters of a transistor vary with
temperature, particularly the d.c. current gain "α", the collector
cut-off current "I_{co}", and the base to emitter voltage drop "V_{be}".

The transistors in the relaying circuitry are designed, as
menitoned in sec. (8.1), to operate as switches or as saturated
amplifiers in order to minimise risks of incorrect operation due
to variations in gain.

The variation in the gain parameter "α" may differ a little
and therefore its tolerance would appear to be of little consequence
in circuits of the common base configurations. This was one of
the main reasons of adopting an amplifier in a common base
configuration at the input of the squaring circuit to control the
mark/space ratio of the generated square-wave output, as
mentioned in sec. (8.2).

A major contribution to instability, for transistors in a
common-emitter configuration, is the term $(1-\alpha)$ in the current
gain "β"; the variations due to this term must be reduced as much
as possible. In designing the input amplifiers of the fault
detecting circuits, sec. (8.3.1), the effect of temperature
variations on their linearity was minimised by using high voltage
rated silicon transistors. Drift due to change of V_{be} or α,
is of the same order for germanium and silicon transistors, but

the silicon type proved to provide better stability due to their extremely low I_{co}. The effect of this leakage current was further reduced by using high voltage rated transistors operating at low collector voltage and high collector current values.

Such an arrangement proved to be satisfactory as far as keeping the sensitivity of the pick-up level of the starting circuits within 10% of the setting, for a temperature rise about $25^{\circ}C$ over the ambient temperature.

For the above mentioned range, of temperature variations, the stability angle of scheme was found to suffer a change of about $\pm 12.5\%$ of its normal value of 40°. This was traced to be due to the change in the unity mark/space ratio of the output square-waves of the phase shifting circuit and the receiving circuit, Figs. (8.8 and 8.9) respectively.

However, the situation could still be improved by using silicon transistors, as mentioned earlier in this section, for these two particular circuits.

The performance of the scheme, as a whole, does not suffer any appreciable change when the power supply voltage was varied between -15 to +10% of its rated value. The change in the stability angle for such a range of variations was less than $\pm$ 10%. This change is small and can be accepted without any need for applying further complicated compensation arrangements in the circuitry.

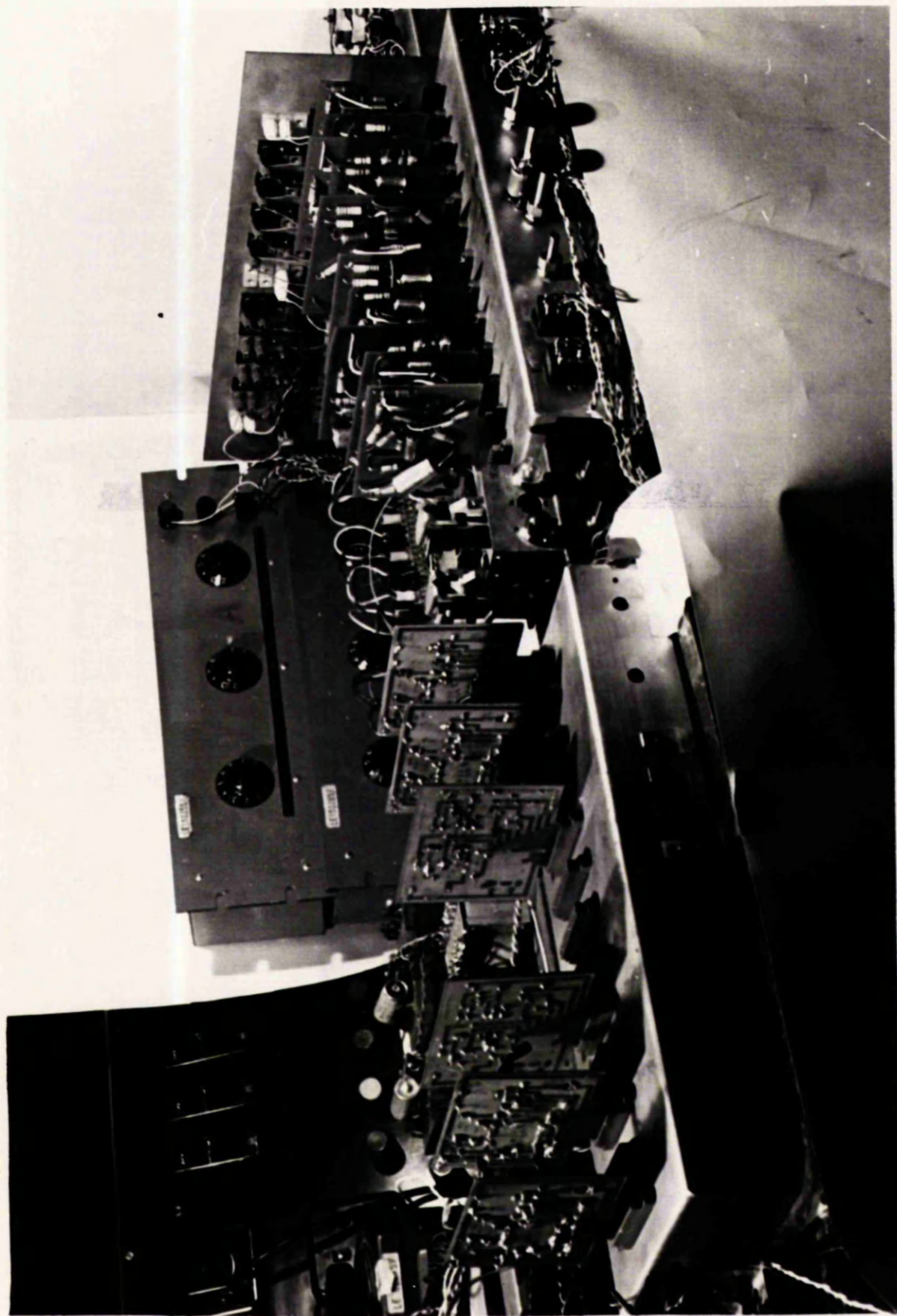FIG. (9.7) VIEW OF THE COMPLETE EQUIPMENT DURING

TESTING.

FIG. 9.7.

Fig. (9.7) shows a view of the complete equipment of the scheme during one of the testing stages.

CHAPTER 10

CONCLUSIONS AND RECOMMENDATIONS

10.1 General Considerations

Due to the nature of the work described in this thesis, conclusions regarding specific problems must be drawn in stages. This has, in fact, been mentioned in most of the previous chapters.

There are, however, some more general points which arise from the work as a whole.

10.2 Selection of Relaying Quantities

A single relaying quantity derived from all the three phases at each end of the protected line, is adopted for the comparison scheme developed in this work.

One quantity representing the phase angle and two quantities indicating the fault were chosen at each end of the line to meet various fault conditions on the primary system as well as to obviate incorrect operation due to pilot-circuit failures.

The summation transformer, as a means of providing this single relaying quantity, has proved to be unsuitable for some resistance earthed systems.

The analysis of the summation current transformer under single phase faults gave a criterion, based on practical conditions, for the S.C.T. turns ratios of $n \geqslant 5$ in an arrangement $(n : n + 1 : n + 2)$ turns ratios. However, the S.C.T. is suitable for directly earthed systems provided its

turns ratios are correctly chosen.

The corresponding arrangement with ironless-core C.T.s. offers more advantages than a summation scheme with conventional S.C.T.

: The adopted sequence currents combination as a phase angle representing quantity was quite satisfactory for the transmission system considered in chapter 5, and for the range of system parameters evaluated in sec. (5.8).

For further work, it is suggested that a more general case for the study of the behaviour of such a relaying quantity would be a double circuit teed feeder having ring generations at its terminals. The effect of mutuals in the case of untransposed lines can be considered. This problem can be best tackled on a digital computer. A moving earth fault on one circuit of the transmission system as well as simultaneous faults would also be envisaged to find any "blind spots" for such a relaying quantity.

The effect of different transformer connections at the line terminals introduces a phase angle error between the relaying quantities at each end of the protected section . Such a topic is worth further analysis in more detail.

However, it is felt that a minimum stability angle of about $\pm 45^{\circ}$ would cover such cases as well as power swing conditions on feeders of 132 kV system, sec. (2.3).

10.3 Performance of Ironless-Core C.T.s (Linear Couplers)

Ironless-core C.T.s (linear couplers) are associated with the developed scheme for the advantages they offer. They have also their limitations, chapter 3. Their advantages can be summarized as follows:

(a) Linearity

They represent in their circuit aspect a linear transfer impedance, i.e. they produce output voltages which are linear functions of the current flowing in their primary circuit.

This linearity is not over a limited range as in the case of D.A.G. current transformers, which were associated previously with pilot-wire protection.

(b) Transient Response

It has been shown in chapter 3 that, when the primary current contains a unidirectional component, the corresponding component in the secondary voltage of a linear coupler is reduced by the "Q" factor of the primary circuit. It can, therefore, be considered, from the practical view-point, that they produce no transient output.

Troubles associated with transient components in phase-angle-comparison schemes have been avoided and saturation problems are completely eliminated.

(c) Stability

The stability of summation schemes with linear couplers depends only on the tolerance within which the toroid coils are wound. A stability

ratio of a single phase summation voltage scheme was found to be about 250, sec. (6.2.7).

The three phase summation scheme, corresponding to the connection of the summation current transformer has an effective stability ratio about half the above mentioned figure, sec. (4.4.1). No biasing arrangements are necessary as in the case of conventional C.T.s.

The main limitation of the ironless-core C.T.s has been in their low power output. In the work described here, this is no longer a limitation since transistorised relaying circuitry were used. The work carried out and described in this thesis demonstrated clearly that such a limitation can be practically annulled using static relaying techniques.

10.4 Sequence Segregating Networks

Sequence components segregating networks of a novel form have been developed and operated satisfactorily when associated with ironless-core C.T.s.

These circuits, chapter 6, are simple, very cheap, and economical. Bulky and expensive iron-inductors were completely avoided on grounds of cost and space economy. Thus avoiding the use of any element which may introduce non-linearities. Extending the application of these segregating network to other fields of protection is obvious. They have great importance when associated with transistorised relaying circuits.

A relaying element, which was also developed by the author[32], operated satisfactorily with the segregating networks described in sec (6.2).

The application of these segregating networks, when associated with linear couplers, in alternator protection as well as in carrier protection, produces obvious advantages. In carrier protection such an arrangement eliminates the use of complicated filter circuits which are generally incorporated to filter-out the unidirectional components of the fault current. Such filter circuits were always a source of subsidence transients and oscillations.

The segregating networks developed in chapter 6 are frequency insensitive, for all practical applications, as the error produced at their output terminals is always less than the order of the deviation in the system frequency itself.

The absence of any non-linear elements from these segregating networks preserves the linearity of their combination with linear couplers with respect to the primary current.

10.5 Transistorised Relaying Circuitry

Transistor and semi-conductor relaying devices offer some very attractive advantages which include small size, light weight, and low power consumption. Other useful properties are their excellent switching characteristics and immunity to mechanical shocks and vibrations.

A further point is the improvement in reliability of circuits using transistors and semi-conductors. This is attributed not only to their relatively long life but also their use causes a significant reduction in the failure rate of other components.

These features of transistors and semi-conductor devices justify the technique followed in developing the scheme circuitry. The advantages obtained can be summarised as follows:-

(a) Low burden

(b) Greater sensitivity

(c) Higher speeds

(d) Freedom from mechanical disturbances

(e) Light weight, compactness, and economy in maintenance.

More complicated techniques for designing the scheme circuitry could have been used but, as mentioned in chapter 8, simplicity and economy without sacrifice in performance, were the two main factors which influenced the design. From the performance of the scheme, chapter 9, and of each individual stage, within their limits, it can be seen that these aims have been achieved. The limits are acceptable for practical applications.

10.5 Reliability

Long term reliability is essential from the practical point of view. If the mean working time before a fault develops is short, maintenance

and inspection will prove to be uneconomical.

During the past two years of the progress of this work, as the different stages of the relaying equipment were constructed, they were operated over long periods, under marginal conditions, without any failure. In fact in most of the 'cases failure was due to human intervention.

The reliability of the different components used is[11]:-

Resistances 0.0001% per thousand hours

Capacitances 0.001% per thousand hours

Transistors 0.01% to 0.1% per thousand hours

Diodes   0.001% per thousand hours

The reliability of transistors could be increased with special technique to 0.001% per K hours.

An equipment developed in the Power Systems Laboratory, having a similar design nature to those employed in the present scheme, containing a large number of components, about 700 (resistors, capacitors, transistors and diodes) was put on long-term[31] continuous test for a year without any component failure.

It is noticed, however, that with the advancement achieved in techniques of manufacture and use of transistors higher reliability will be achieved.

10.6 Scheme Performance

The scheme developed in this work provides a form of pilot-wire protection, employing phase-comparison techniques, which has a characteristics almost independant of the pilot-circuit parameters. This has been possible by using ironless-core C.T.s and transistorised relaying circuits. This scheme would meet the increase in G.P.O. pilot-circuit resistances either to cover longer feeders or due to using smaller conductor sizes by the G.P.O.

The performance of the scheme, as given in chapter 9, is considered satisfactory for pilot circuits of 6000 Ω loop resistance, i.e. in the range of 30 - 45 miles.

The scheme can easily cover longer pilot lengths if the impressed voltage across the pilot-circuit is increased to, say, 50 volts, as suggested in sec. (9.2.2). The limit of the pilot circuit resistance can then be raised to about 10,000 Ω. With such long pilot circuits having a large loop resistance, it is probable that the transmitted signal over the pilots may undergo a shift more than 90°. The phase-shifting circuit, sec. (8.6), using simple R-C networks, to delay the local end signal may not be sufficient to produce shifts over 90°. However, for phase shifts between 90° and 180°, the effective phase shift can be made less than 90°, by reversing the polarity of the local square-wave by means of an inverting stage, i.e. using the supplementary of the phase-shift. (Similarly, phase-shifts between 180° and 270° can be effectively reduced).

However, such large phase-shifts are unlikely to be met in practice on pilot-circuits used for protection purposes.

It can be concluded that the scheme, as it stands, has a stability angle of $\alpha = \pm 40^{\circ}$ and an average operating time of about 3 cycles, including that of the anxiliary relay. This speed of operation can be further improved by eliminating capacitive coupling between some stages of the relaying system and using d.c. coupling instead.

This scheme, unlike present-day ones, for most applications does not need any voltage limiting devices, and therefore eliminating any high voltage risks,which may damage the equipment,to be applied to the pilot circuit inadvertently.

Furthermore, linear couplers can operate on o.c. conditions without giving rise to large voltages as in the case of iron-cored ones.

It is not easy to anticipate the effect of the noise conditions of the power system on the linear couplers. It is suggested in sec. (9.2.2) that the noise from the pilot-circuit side can be swamped by impressing higher voltages on the pilots and thus allowing to decrease the sensitivity of the receiving circuit to avoid any interference from noise, pick-up, etc.

The only means to obtain information on these last points would be by carrying out field tests on a prototype of the developed equipment. This equipment could then be installed in parallel with an existing equipment, i.e. as a duplicate. This will also give, after a certain period, an indication on the reliability of components under practical field conditions.

APPENDIX (1)

EVALUATION OF THE π-EQUIVALENT CIRCUIT FOR A FOUR-TERMINAL NETWORK

It has been mentioned in sec. (7.3.1) that the π or T equivalents of an asymmetrical pilot-circuit can be evaluated from the general constants A, B, C and D of a complex four terminal network.

Fig. (7.1) give the relationship between the elements of the π and T-equivalents and these constants.

Fig. (1.1a) shows a 4-terminal network having complex constants A, B, C, and D. These constants are related by the well-known equations

$$V_s = A. V_R + B.I_R \left. \begin{array}{c} \\ \\ \end{array} \right\} \quad \ldots \ldots (1.1)$$
$$I_s = C. V_R + D.I_R$$

For the π-equivalent circuit shown in Fig. (1.1b), the relationship between the currents and voltages are:-

$$V_s = V_R + (I_R + V_R.Y_R)Z \qquad \ldots \ldots (1.2)$$

and $I_s = V_s.Y_s + (I_R + V_R.Y_R) \qquad \ldots \ldots (1.3)$

Substituting from eqn (1.3) in eqn (1.2) it can be proved that:-

$$V_s = (1 + Y_R Z) V_R + (Z) I_R \left. \begin{array}{c} \\ \\ \end{array} \right\} \ldots (1.4)$$
$$\text{and} \quad I_s = (Y_s + Y_R + Y_R.Y_s.Z)V_R + (1 + Y_sZ)I_R$$

APPENDIX (i)
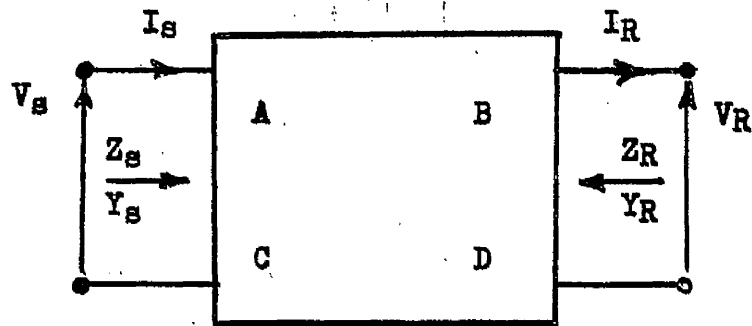
(a) General Four Terminal Network
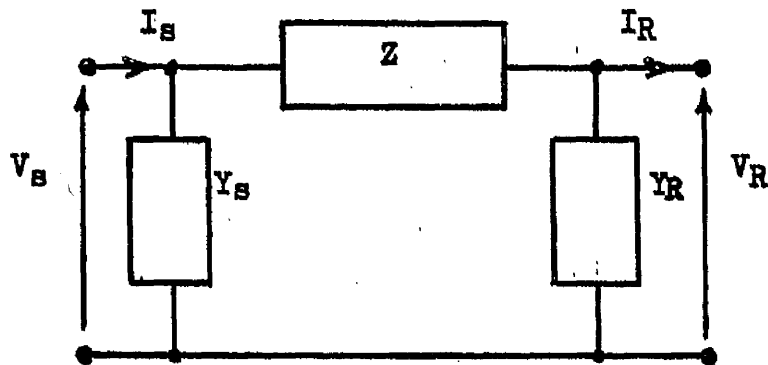
(b) π-Equivalent Circuit

FIG. (i.1). π-EQUIVALENT OF A FOUR-TERMINAL NETWORK.

Comparing eqns (i.1) with eqns (i.4), it can be easily seen that:-

$$A = 1 + Y_R \cdot Z$$
$$B = Z$$
$$C = Y_S + Y_R + Y_R \cdot Y_S \cdot Z$$
$$D = 1 + Y_x \cdot Z$$

$$\ldots\ldots (i.5)$$

If the constants A, B, C, and D are known or found by measurements of the open and short-circuit impedances of the pilot circuit, then the elements of the π-equivalent circuit can be expressed in terms of the general constants, from eqns (i.5), as follows:-

$$Z = B$$
$$Y_S = (D - 1)/B$$
$$Y_R = (A - 1)/B$$

$$\ldots\ldots (i.6)$$

REFERENCES

1. Stubbings, G.W.:

   "Automatic Protection of A.C. Circuits",

   Chapman and Hall Book Co., London.

2. Neher, J.H.:

   "The Use of Communication Facilities in T.L. Relaying",

   Trans. A.I.E.E., 1933, 52, p. 595.

3. Harder, E.L., Bostiwck, M.A.:

   "A Single Element Differential Pilot-Wire Relay System",

   Elect. Journal, 1938, 35, p. 443.

   Also,

   "Protection of Pilot-Wire Circuits",

   Trans. A.I.E.E., 1942, 61, p. 645.

4. Fenwick, W., Marais, C.:

   "The Application of Pilot-Wire to Long 88kV T.L.s.
   including Intertripping",

   Trans. S.A.I.E.E., 1945, 36, p. 60.

5. Casson, W., Last, F.H.:

   "Ultra-High-Speed Relays in the Fields of Protection and
   Measurement",

   Proc. I.E.E., 1947, 96, Part II, p. 667.

6. Halman, T.R., Goldsborough, S.L., Lensner, H.W. & Drompp, A.F.:

   "A New Carrier Relaying System",

   Trans. A.I.E.E., 1944, 63, p. 568.

7. McConnell, M.J. Cramer, T.A., and Seeley, H.T.:

   "Phase-Comparison Carrier Current",
   ibid., 1945, 64, p. 825.

8. Adamson, C., Talkhan, E.A.:

   "The Application of Transistors to Phase-Comparison

   Carrier Protection",

   Proc. I.E.E., 1959, 106, p.51.

9. Adamson, C., Talkhan, E.A.:

   "Selection of Relaying Quantities for Differential

   Feeder Protection",

   Proc. I.E.E., 1960, 107, Part A, p. 37.

10. Rushton, J.:

    "The Fundamental Characteristics of Pilot-Wire

    Differential Protection Systems",

    Proc. I.E.E., 1961, 108, Part A, p. 409.

11. Shop, J.E., Sullivan, H.L.:

    "Semi-Conductor Reliability"

    Engineering Publishers, New Jersey.

    Also,

    Dummer, G.W.A., Griffin, N.:

    Pitman, 1960.

12. Forrest, J.S. and others:

"The 400kV Grid System for England and Wales",

Proc. I.E.E., 1962, <u>109</u>, Part A., p. 493.

13. Mathews, P.:

"Protective Current Transformers and Circuits",

Chapman and Hall, 1956, (Chapters 6 and 7).

14. A.I.E.E. Committee Report:

"Pilot-Wire Circuits for Protective Relaying -

Experience and Practice",

Trans. A.I.E.E., 1953, <u>72</u>, Part III, p.331.

15. Rushton, J.:

"Performance and Design of Pilot-Wire Differential

Protective Systems Using Long Pilot Circuits",

Fellowship Thesis, Manchester College of Science and

Technology, 1961.

16. Hamilton, F.L.:

"The Protection of Feeders by Pilot-Wire Systems",

Reyrolle Review, 1959.

Also,

"Reyrolle H.P.P.W. Feeder Protection".

Reyrolle Pamphlet 1296.

17. Warrington, A.R. van C.:

      "Protective Relays, their Theory and Practice",

      Chapman and Hall, 1962.

18. Hidaka, K., Horigome, T., Ito, No. and Nagamura, G.:

      "Analysis of Zero-Sequence Circulating Current in

      untransposed T.L.s",

      E.T.L., Tech. Report No. 8/2, 1961, Tokyo, Japan.

19. Adamson, C., Wedepohl, L.M.:

      "Power System Protection, with particular reference

      to the Application of Junction Transistors to Distance

      Relays",

      Proc. I.E.E., 1956, 103, Part A, p. 379.

   Also,

      "A Dual-Comparator MHO-Type Distance Relay Utilizing

      Transistors",

      Proc. I.E.E., 1956, 103, Part A, p. 509.

20. Talkhan, E.A.:

      "The Application of Junction Transistors to Phase-

      Comparison Carrier Protection",

      Ph.D. Thesis, University of Manchester, 1958.

21. Mathews, P., Nellist, B.D.:

   "The Design of Air-Cored Torids or Linear Couplers",

   Proc. I.E.E., 1962, 109, Part A, p.229.

   Also,

   "Transients in Distance Protection",

   Proc. I.E.E., 1963, 110, No. 2, p. 407.

22. Donaldson, G.W.:

   "The Application of Phase-Comparison Principles

   to Power Swing Conditions on Long H-V. T.L.s",

   Proc. I.E.E., 1951, 98, Part II, p. 47.

23. Gray, C.B.:

   "The Application of Static Relays to Feeder Protection

   Utilising High Impedance Pilots",

   M.Sc.Tech. Thesis, University of Manchester, 1958.

24. Neher, J.H.:

   "A New Approach to the Pilot-Wire Protection of T.L.s -

   Using Leased Pilots having Relatively Long Electrical

   Characteristics",

   Trans. A.I.E.E., 1960, 79, Part II, p. 245.

25. The Royal Signals:

   "Handbook of Line Communication",

   H.M.S.O., Vol. 1, 1947.

26. Nellist, B.D.:

   "The Application of Air-Cored Mutual Inductors to
   Power System Protection",

   Ph.D. Thesis, University of Manchester, 1961.

27. Morris, W.C., Goff, I.E.:

   "A Negative Phsse Sequence O/C Relay",

   Trans. A.I.E.E., 1953, 72, Part III, p. 615.

28. Wagner, F.C., Evans, R.D.:

   "Symmetrical Components Analysis of Unbalanced
   Electrical Circuits",

   McGraw-Hill, 1933.

   Also,

   Karapetoff, V.:

   "Experimental Electrical Engineering",

   John Wiley & Sons, 1948, New York.

29. Russell, R.L.:

   "An Instrument for Complete Symmetrical Component Analysis",

   Proc. I.E.E., 1950, 97, Part II, p. 29.

30. El-Sharkawi, E.:

   "Three Phase Static Balancer Employing Symmetrical
   Bridges",

   Thesis for Dipl. in Elect. Power Eng., University of
   Durham, 1960.

31. Khalil, N.:

"Telemetering in Power System Control",

Ph.D. Thesis, University of Manchester, 1962.

32. El-Sharkawi, E.:

"Square Law Adder Employing a Thermistor/Transistor

Circuit",

Report, Power Systems Laboratory, Manchester College of

Science and Technology, 1961.